UNIVERSITY OF CALIFORNIA, SAN DIEGO

Digitally Enhanced High Resolution Pipelined Analog-to-Digital Conversion

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy

in

Electrical and Computer Engineering (Electronic Circuits and Systems)

by

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To my family

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PUBLICATIONS

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ABSTRACT OF THE DISSERTATION

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By

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CMOS Analog-to-digital converters (ADCs) are used extensively in modern electronic systems to take advantage of the benefits provided by processing signals digitally. Digital signal processing offers increased programmability, improved noise immunity, simplified automated design and testing, and improved cost and performance from the scaling properties of CMOS integrated-circuit (IC) technologies.

However, when analog functionality is replaced with digital, more stringent requirements are placed on ADCs because less analog pre-processing is performed on the ADC input signal and a larger portion of the IC contains "noisy" digital signals. Pipelined ADCs (PADCs), consisting of a cascade of low-resolution ADC stages, have become a popular ADC architecture due to their ability to achieve medium-to-high speed with medium-to-high resolution. However, performance is sensitive to the inevitable errors due to analog circuit imperfections present in each stage of the PADC, in particular interstage gain errors and digital-to-analog converter (DAC)

element mismatches.

In this dissertation, the performance of PADCs is enhanced using digital signal-processing techniques that correct for inherent analog circuit imperfections. A *gain-error correction (GEC)* technique is introduced that continuously estimates and corrects for errors resulting from interstage gain errors. Chapter 1 presents a 1.8-V 15-bit 40 Msample/s CMOS PADC that achieves 90-dB SFDR and 72-dB peak SNR. The IC is the first silicon implementation of the GEC technique and a *DAC noise cancellation (DNC)* technique, which corrects for errors due to DAC element mismatches. Together these techniques result in a better than 20-dB improvement in SFDR and a better than 12-dB improvement in SNDR. The theoretical basis for the GEC technique is presented in Chapter 2.

An integral component of the DNC technique is a dynamic element matching (DEM) DAC that replaces the conventional DAC present in each stage of the PADC where DNC is used. The size of the digital encoder employed by the DEM DAC dictates the size of the digital logic required to implement the DNC technique, and is doubled with each additional bit of resolution. Chapter 3 addresses this problem by introducing *segmented tree-structured dynamic element matching DACs* that offer reduced DEM encoder complexity.

Chapter 1

A Digitally Enhanced 1.8-V 15-b 40-MSample/s CMOS Pipelined ADC

Eric J. Siragusa and Ian Galton

Abstract—A 1.8-V 15-bit 40-MSPS CMOS pipelined ADC (PADC) with 90-dB SFDR and 72-dB peak SNR over the full Nyquist band is presented. Its performance is enhanced by digital background calibration of DAC noise and interstage gain error. With calibration enabled, a better than 12-dB improvement in SNDR and a better than 20-dB improvement in SFDR is achieved. Differential nonlinearity is 0.25 LSB while integral nonlinearity is 1.5 LSB. The IC is realized in a 0.18-μm mixed-signal CMOS process, consumes 400 mW, and has a die size of 4 mm × 5 mm.

I. INTRODUCTION

The trends toward increased digital signal processing and tighter integration in communications and imaging systems have created a need for high-resolution, low voltage analog-to-digital converters (ADCs) with sample-rates above 20 MHz. Pipelined ADCs (PADCs) are well-suited to such application, but are sensitive to DAC noise from component mismatches, and interstage gain errors. This paper demonstrates two digital background techniques that address these problems: the DAC noise is removed using the DAC noise cancellation technique (DNC) presented in [1], while interstage gain errors are removed using the gain error correction technique (GEC) presented in [2]. Together these techniques enable a 1.8-V 15-bit 40-MSPS CMOS pipelined ADC (PADC) with 90-dB SFDR and 72-dB peak SNR over the full Nyquist

band. The differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.25 LSB and 1.5 LSB, respectively. In addition to improved performance, circuit and layout requirements are relaxed, reducing overall design and layout time.

The PADC is implemented using switched-capacitor techniques and, as a result, capacitor mismatch is the main cause of DAC noise and contributes significantly to interstage gain error. Capacitor matching can be improved with careful layout and larger capacitors [3], but only to a practical limit. C code simulations of the PADC suggest that to achieve 90-dB SFDR (with at least a 2-σ yield) without DNC and GEC using this design and circuit technology would have required more than 25-times larger first-stage capacitors. The resulting impact on circuit area and power would have made such a converter impractical. Due to the calibration techniques, the capacitor sizes in this design were determined by kT/C requirements alone.

In addition to capacitor mismatch, contributors to interstage gain error can include insufficient residue amplifier open-loop gain, incomplete residue amplifier settling, incomplete reference settling, switch charge injection, and switch clock feed-through. These circuit non-idealities are typically reduced to an acceptable level with traditional analog circuit techniques and careful layout at the expense of increased complexity and power consumption. The GEC technique implemented here will correct any linear contributions to the interstage gain error. For example, without GEC better than 100 dB of open-loop gain is required in the first stage residue amplifier, which would necessitate gain boosting. However, GEC relaxes the gain requirement to the point that gain boosting is not necessary. To demonstrate this point, the IC contains gain- boosting circuitry that can be disabled digitally. With GEC enabled, no

significant performance degradation is found with gain boosting disabled.

Analog circuit imperfections such as those discussed above typically dictate the use of some form of calibration or trimming to achieve resolutions better than 12 bits. Other known calibration techniques either operate in the foreground disrupting normal use [4],[5],[6] require additional stages [7],[8], require extra clock phases [9],[10], reduce the input bandwidth [11], only improve DNL [12], or cause a reduction in dynamic range [13],[14]. Component trimming is an alternative to calibration; however this increases costs and is only a one-time correction. Recently a slight extension of the DNC technique was presented to correct for both DAC and interstage gain errors [15]. However the technique is limited in that only errors resulting from capacitor mismatch can be corrected.

A high-level diagram of the implemented PADC is shown in Fig. 1.1. The remainder of the paper will describe details of the various blocks shown in the figure. Section II presents high-level architectural details including the implementation of the DNC and GEC techniques. Section III presents circuit details while Section IV presents measured results.

II. SYSTEM-LEVEL DESIGN DETAILS

Pipeline ADC System Overview

The PADC in Fig. 1.1 consists of seven stages, each coarsely resolving slightly more than 3-bits (9 levels instead of 8). Due to the extra level in each stage, the overall PADC output dynamic range is slightly more than 15 bits and is represented with a 16-

bit two's-complement number. Redundancy is employed to eliminate errors in each stage's flash ADC [16]. The correction algorithms are only applied to the first three stages, as errors in the remaining stages are negligible when referred back to the input. To simplify logic and reduce convergence time of the DNC and GEC algorithms, all error estimations and corrections are performed in parallel. Assuming all of the DAC errors and gain errors are sufficiently small, the effect on overall performance is negligible.

The resolution of the first stage affects many aspects of the system-level design. Advantages of increased resolution can include reduced number of stages, reduced overall power dissipation (since residue amplifier power dissipation for high-resolution designs typically dominates over comparator power dissipation), and reduced sensitivity to remaining stage's mismatches and noise [17]. The DNL of a PADC is also improved [6], [17], [18], as the errors due to DAC capacitor mismatch are lessened. However, DNC corrects for any such errors, removing this issue from consideration and simplifying overall system design. Disadvantages of increased resolution include increased input loading due to the increased size of flash ADC and, as will be shown later, increased DNC digital logic size due to the increased number of DAC elements. Furthermore, since the stage step size is reduced, the immunity to comparator and amplifier offsets, which may not scale with the step size, is decreased. A 3-bit first stage was found to be a good choice taking into consideration all of the factors above. All stages resolve the same number of bits to increase circuit design and layout re-use.

The simplified diagram of a correction stage is shown in Fig. 1.2. It differs

from a conventional PADC stage in three respects:

1. a dynamic element matching (DEM) DAC (needed for DNC) is used in place of a thermometer-encoded DAC,
2. a 1-bit pseudo-random number (PN) sequence, $r_{gec}[n]$, which takes on values of $\pm\Delta/4$ referred to the DAC output, is added to the input of the DAC, where Δ is the step-size of the flash ADC, and
3. the resolution of the DAC is increased to accommodate $r_{gec}[n]$.

The DEM DAC used in this design consists of a partially-segmented DEM digital encoder followed by a bank of 10 1-bit switched-capacitor DACs, 8 with a step-size of Δ and 2 with a step-size of $\Delta/2$ [19]. To minimize latency, the $r_{gec}[n]$ adder and DEM encoder are implemented together, as will be described in Section III.

Basic Converter Operation

Ideally, the output of the first stage residue amplifier is a scaled, inverted, analog representation of the coarse flash ADC's quantization noise. This amplified residue signal is digitized by the remaining stages of the converter, which together constitute an ADC. When this *digitized residue* is added to the digital output of the first stage, complete cancellation of the first stage quantization noise occurs. Except for the last stage, the operation of the remaining stages is identical, yielding a high resolution PADC output equal to the input plus last stage quantization noise. However, in practice there are DAC mismatches in each stage that create noise that is correlated with the input. This noise is digitized by the remaining stages and corrupts the overall converter output. Furthermore, there are gain errors present in the path that each

stage's quantization noise travels. The resulting digitized residues will not completely cancel each stage's digital output and the overall converter output will be corrupted.

Dynamic Element Matching DAC

Each DAC in a conventional PADC consists of a bank of 1-bit DAC elements that are controlled directly by the outputs of a coarse flash ADC. This deterministic control results in tones in the output spectrum when DAC element mismatches are present. If a DEM DAC is used instead, the 1-bit DAC elements are preceded by a DEM encoder that causes the errors arising from static mismatches to be shaped or whitened, depending on the application. Nyquist-rate applications typically employ whitening, as the input signal consumes the entire available spectrum, leaving no portion available for the error power to occupy. The encoder exploits the fact that there are many possible combinations of the one-bit DAC inputs that result in the same nominal (error-free) DAC output, but with a different overall DAC error. If the combinations are chosen properly the resulting output noise spectrum can have the desired spectral properties.

The architecture of the DEM DAC used in the correction stages is shown in Fig. 1.3. It is a partially-segmented tree-structured DEM DAC, consisting of a digital encoder followed by a bank of weighted 1-bit DAC elements [19],[20]. The implementations of the encoder and of the switched-capacitor 1-bit DACs are discussed in Section III. The analog outputs of the 1-bit DACs are summed together via the residue amplifier, not shown in the figure. The encoder consists of nine *switching blocks,* labeled S_{seg} and $S_{k,r}$, where $k \in \{1,2,3\}$ and $r \in \{1,2,3,4,5\}$. Each

switching block generates a corresponding *switching sequence* defined as

$$s_{seg}[n] = \begin{cases} 0 & o_{seg}[n] = 0 \\ +1 & o_{seg}[n] = 1 \quad and \quad q_{seg}[n] = +1 \\ -1 & o_{seg}[n] = 1 \quad and \quad q_{seg}[n] = -1 \end{cases},$$
$$s_{k,r}[n] = \begin{cases} 0 & o_{k,r}[n] = 0 \\ +1 & o_{k,r}[n] = 1 \quad and \quad q_{k,r}[n] = +1 \\ -1 & o_{k,r}[n] = 1 \quad and \quad q_{k,r}[n] = -1 \end{cases} \qquad (1)$$

where $q_{seg}[n]$ and $q_{k,r}[n]$ are random bits coming from the pseudo-random number generator, and $o_{seg}[n]$ and $o_{k,r}[n]$ are the parities of the input to each of the switching blocks. Each pseudo-random sequence is designed to well approximate white, zero mean, random process that is uncorrelated with all other signals in the PADC. These statistical properties are inherited by the $s_{seg}[n]$ and $s_{k,r}[n]$ sequences by virtue of their definition in Eq. (1). Ignoring the $\Delta/2$ LSB factor, the DAC input, $x_{in}[n]$, can be viewed as an integer in the range -8 to 8. At each sample time n, the top and bottom outputs of switching block S_{seg} are set to $(x_{in}[n]+s_{seg}[n])/2$ and $-s_{seg}[n]$, respectively, and the top and bottom outputs of switching block $S_{k,r}$ are set to $(x_{k,r}[n]\pm s_{k,r}[n])/2$, respectively. It can be shown that mismatches cause the DEM DAC to introduce additive *DAC noise* of the form

$$e_{DAC}[n] = \sum_k \sum_r \Delta_{k,r} s_{k,r}[n] + \Delta_{seg} s_{seg}[n], \qquad (2)$$

where the Δ_{seg} and $\Delta_{k,r}$ terms are constants that depend only on the element mismatches. This noise is white due to the aforementioned statistical properties of the $s_{seg}[n]$ and $s_{k,r}[n]$ sequences. The converter's SFDR has been improved, but at the expense of the SNR, as the resulting white DAC noise increases the overall noise

floor. The DNC technique discussed next exploits the statistical properties of the $s_{seg}[n]$ and $s_{k,r}[n]$ sequences to estimate and remove this DAC noise.

DAC Noise Cancellation

As seen in Eq. (2), the DEM encoder imparts a "structure" to the DAC noise, similar to spread spectrum modulation of several dc "message signals": the constant Δ_{seg} and $\Delta_{k,r}$ terms are modulated by their corresponding $s_{seg}[n]$ and $s_{k,r}[n]$ sequences. The DNC logic implements a simple digital spread-spectrum "receiver", or correlator, that estimates the Δ_{seg} and $\Delta_{k,r}$ terms and uses them to cancel the DAC noise at the converter output. The statistical properties of the $s_{k,r}[n]$ sequences – zero mean and uncorrelated with the each other and the input – ensure accurate correlations. Additional details of the DNC theory can be found in [1].

The top-level diagram of the calibration logic for the first stage is shown in Fig. 1.4. The logic for the second and third stages is almost identical to maximize circuit and layout re-use, at the expense of increased circuit area. The input to the logic is the first stage's digitized residue (the combined digital outputs of all the remaining stages). The digitized residue contains the output referred DAC noise, which is an inverted and scaled version of Eq. (2). The DNC logic consists of nine *channels*, one for each switching block in the DEM DAC encoder. The input to each channel comes from the *dithered* requantization block that converts the 14-bit digitized residue into a 7-level digital number. Requantization is performed to reduce the size of the logic in each of the channels. *Dithered* requantization ensures that the resulting requantization noise is white and uncorrelated with the digitized residue – a necessity to avoid

corrupting the correlations [1]. One drawback is that the requantization noise slows down the correlation process, increasing the time required for convergence. Seven-level requantization was found to be a good compromise between logic size and convergence time.

Each DNC channel consists of a simple correlator that produces an output referred estimate of one of the Δ_{seg} or $\Delta_{k,r}$ terms in Eq. (2), followed by logic that effectively multiplies the estimate by the corresponding $s_{seg}[n]$ or $s_{k,r}[n]$ sequence. Therefore, the overall output of the DNC logic, y_{DNC}[n], is an output referred estimate of the total DAC noise of Eq. (2) and is used to cancel the DAC noise at the PADC output.

Gain Error Correction

As discussed earlier, gain error in the path that the quantization noise travels results in leakage of the quantization noise into the PADC output, degrading both the SFDR and SNDR of the converter. In the GEC technique, a random signal, $r_{gec}[n]$, which approximates a white, zero mean sequence that is uncorrelated with all other signals in the PADC, is added to the input of the DAC as shown in Fig. 1.2 [2]. This signal takes on values of $\pm\Delta/4$ referred to the DAC output and travels the same path that the quantization noise travels to the PADC output. The $r_{gec}[n]$ signal incurs any gain along the path and, in a manner similar to DNC, a simple digital correlator is used to estimate the gain. An estimate of the gain error is then found and used to digitally correct the PADC output. The path traveled by the $r_{gec}[n]$ signal must be linear to avoid corrupting the correlation. The whitening of the DAC noise due to DEM ensures

that the DAC is linear and doesn't interfere with the GEC correlation. Although not shown in the figure, the nominal value of the $r_{gec}[n]$ signal is added to the digital output of the stage, $y_{out}[n]$, to ideally cancel with the inverted signal in the stage's digitized residue.

The amplitude of $r_{gec}[n]$ must be sufficiently small to prevent overloading the following stages, as the signal consumes some of the error headroom created by the redundancy used to cancel comparator errors. However, a large signal is desirable to speed up convergence of the estimation. As a compromise, an amplitude of $\Delta/4$ was chosen, leaving approximately one-half of the error headroom available for comparator errors. To create the $\pm\Delta/4$ signal, a +1/2 or 0 signal is added at the FADC output and a $-\Delta/4$ constant offset is introduced at the DAC output (not shown). Thus only 1-bit of extra resolution is required in the DAC (instead of 2).

The GEC logic in Fig. 1.4 consists of a correlator that estimates the gain, followed by logic that creates an estimate of the gain error. The gain-error estimate is then used to form the output correction signal. Ideally, to correct for the gain error the digitized residue should be divided by $1+\tilde{e}_g$, where $\tilde{e}_g$ is the gain error estimate. Under the assumption of a small gain error, the digital complexity is reduced by making a linear Taylor Series approximation of the division. The correction is thus performed by multiplying the digitized residue by $-\tilde{e}_g$ and adding the result to the PADC output. As will be described in more detail Section III, to avoid overloading the DAC, the GEC estimation logic is paused when the FADC output is positive full scale, denoted by the f_z input signal to the GEC correlator in Fig. 1.4. The same issues regarding dithered requantization and the DNC logic previously discussed apply to the GEC logic as well.

III. CIRCUIT-LEVEL DESIGN DETAILS

Overview of Switched Capacitor Implementation

A simplified timing diagram of the chip is shown in Fig. 1.5. Details of the clock phases will be discussed later in this section. Delayed bottom-plate switching is used throughout to reduce charge injection and clock feed-through effects. Separate DAC and input capacitors are used to prevent signal dependent loading of the references at the expense of increased *kT/C* noise (due to the extra capacitors) and increased residue amplifier requirements (feedback factor is reduced).

Input Sampling Network

Signal processing in a switched-capacitor PADC is done in discrete-time, requiring the differential continuous-time inputs to be sampled. The input sampling network must have better performance than the overall converter to avoid performance degradation. This sampling is typically performed either by an input sample and hold amplifier (SHA), or by a passive network feeding a holding amplifier. However in either case the amplifier will limit overall dynamic performance and contribute excessive noise unless significant power is spent. In this design the continuous-time sampling operation is distributed into the main signal path and the flash ADC path [21], as shown in Fig. 1.2. As described in [21], mismatches in the path time constants cause the sampled signal in each path to differ. However, this error can be modeled as flash ADC error and will be corrected along with comparator offsets via redundancy, assuming the available error headroom is not exceeded.

The input sampling network and FADC reference ladder sampling network are comprised of eight of the simplified networks shown in Fig. 1.6(a). Although a single-ended version is shown, all implemented circuits are fully differential. Instead of involving the residue amplifier and comparators in sampling the input as was done in [21], two simple switched-capacitor sampling networks are used. Matching is simplified as path time constants are determined by like elements, and isolation between the continuous-time input and the first stage residue amplifier is increased. The flash ADC input network has the same nominal time constant as the main input network; however half-sized elements are used to reduce area and input loading while still maintaining sufficient matching to limit errors between the sampled signals. Bootstrapped switches (described later) are used for critical switches.

DAC Capacitor Network

Fig. 1.6(b) shows a simplified diagram of the fully-differential DAC switched capacitor network. The network consists of 10 1-bit switched-capacitor DACs, 8 with a step-size of Δ and 2 with a step-size of $\Delta/2$. The references in the DAC capacitor network are double sampled (once each clock phase by each capacitor) to allow half-sized capacitors and to decrease the kT/C noise contribution of the DAC. Without DNC and GEC, the increased DAC mismatch noise and gain error resulting from this structure would not be acceptable. The time constant of the DAC capacitor network is designed to match to the main input capacitor network to avoid residue amplifier slewing. Bootstrapped switches are used to sample the references ease matching and reduce switch sizes. Due to DNC and GEC no special attention was paid to capacitor

matching, greatly simplifying the layout and reducing layout time.

Bootstrapped Switch

To achieve the desired SFDR performance over the entire Nyquist band for the 2.25 Vp-p differential PADC input signal the input switch is *bootstrapped* with the circuitry shown in Fig. 1.7. The circuitry is a modified version of that presented in [22]. The process standard thick-oxide devices with 3.3-V voltage limits are used to replace thin-oxide devices wherever 1.8-V technology limits would be exceeded. The resulting switch is very simple compared to other topologies [23],[24],[25]. Other critical switches in the PADC, such as those connected to a voltage near mid-supply, or those used where time-constant constant matching is important, are also bootstrapped. Switches in Fig. 1.6 that are bootstrapped are driven by a clock labeled with a *_bs* suffix.

Clock Generator

Differential, low-level clocks are brought on chip to reduce disturbances on nearby package pins. An input buffer on-chip generates CMOS output levels and drives the non-overlapping clock generator shown in Fig. 1.8. Each stage of the pipeline contains clock circuitry providing local buffering, inverted phases, and proper reset signals for the comparators and the residue amplifier.

With the distributed input sampling network described previously, proper non-overlapping timing of the switched capacitors requires the comparators and DEM encoder to wait until the beginning of the amplification phase to process the inputs –

the non-overlapping time can no longer be used [21]. Therefore in a normal two-phase clocking scheme, the time required for the comparators and encoder to operate reduces the time available for the residue amplifier to settle. Thus the residue amplifier must be faster and may slew if it operates on unsettled encoder outputs. With the separate input and DAC capacitors scheme used in this design, only the DAC capacitors would be affected by the unsettled encoder outputs, increasing the possibility of slewing.

In the design presented here, a separate clock phase is used for comparator pre-amplification, and another is used for both comparator latching and DAC encoder traversal, as can be seen in the timing diagram of Fig. 1.5. The encoder outputs are now completely settled prior to the amplification phase, reducing the potential for slewing. Normally, the time for these extra phases must be taken from both of the main clock phases, thus reducing the time available for all of the residue amplifiers to settle. The first stage amplifier is the most critical block in the pipeline, usually setting limits on converter speed and consuming a significant portion of the overall power. This is especially true with a multi-bit first stage, as the requirements on the remaining stages are relaxed. To ensure that the amplification time for the first stage amplifier is not affected by these extra clock phases, the standard non-overlapping clock generator is modified with an extra feed-forward path, as shown in Fig. 1.8. All of the time for both pairs of pre-amplifier and latching/encoder periods is now taken from the amplification phase of the second stage. Although reducing the available time for the second stage amplifier to settle dictates less allowable amplifier scaling, increasing the requirements on the second stage to the ease the requirements on the first stage is a desirable tradeoff. The pulse width of the clock used to sample the continuous-time

PADC input, *P1s*, is reduced by only one pair of pre-amplifier and latching/encoder periods, as it is not affected by the modification. This pulse-width reduction may be an issue depending on the application (i.e. depending on the input driving circuitry).

Residue Amplifier

Fig. 1.9 shows a simplified diagram of the two-stage miller-compensated OTA used in the residue amplifier. Better than 100 dB of open-loop gain and better than 15 bits of input referred settling in less than half the clock period is required. A folded cascode input stage was chosen for high gain in the low supply voltage environment. A low input common-mode voltage, permitted by a PMOS input pair, simplified the input switching network as small NMOS switches could be used. A common-source output stage was chosen to accommodate the large required output swing, with NMOS transistors in the signal path providing high drive to control the amplifier's non-dominant pole. The OTA output common-mode voltage is sensed by a simple RC circuit and compared to a common-mode reference by a current-mirror amplifier, not shown in the figure. The inverted output of the current-mirror amplifier, labeled V_{CMFB} in Fig. 1.9, is used to control the common-mode voltage.

To achieve the open-loop gain requirement without calibration, gain boosting is required (not shown in Fig. 1.9). Functionality was added to enable and disable gain boosting from off-chip. Simulations under typical conditions indicate around 130 dB of open-loop gain with gain-boosting enabled, but only 85 dB with gain boosting disabled. However, the open-loop gain with gain boosting disabled is still enough to suppress the non-linearities in the amplifier and switches. As a result, the error is

mainly linear and can be corrected by GEC. As expected, the measured PADC performance with GEC enabled does not significantly degrade when gain-boosting is disabled.

The OTA is held in reset without offset cancellation during the stage's input sampling phase. This simplifies the design as the OTA does not need to be stable during this phase [21]. Although the offset of the PADC is increased, this is typically not a problem in most applications. The amplifier is scaled down once and used in all the remaining stages without further scaling. More aggressive scaling would have reduced power consumption without significantly degrading performance, but was not done in the interest of saving design and layout time.

Comparator

Fig. 1.10 shows the architecture of the comparators used in the flash ADC. Each comparator consists of three simple high-speed pre-amplification stages (differential pairs with resistive loads) and a high-speed latch. The pre-amplifiers contain reset circuitry (not shown) to speed up the recovery time. For reduced complexity, offset cancellation is not performed. The composite preamplifier is designed to have sufficiently low offset to avoid taking up too much of the available error headroom due to redundancy and sufficiently high gain to reduce the effect of latch offset. The same architecture is used for all stages.

DAC Encoder

Previous high speed (low latency) implementations of tree-structured DAC

encoders optimize the delay of the individual switching blocks [26] shown in Fig. 1.3. The resulting encoder circuit, having a tree-like implementation, has a critical path consisting of a series of transmission gates. All of the transmission gates can be pre-set as the state depends only on the $q_{seg}[n]$ and $q_{k,r}[n]$ sequences coming from the PN generator. Modeling the series transmission gates as a transmission line and assuming an equivalent load on each gate yields an approximate signal delay [27] of

$$t_d \cong 0.35RC(N)(N+1) \tag{3}$$

where R and C are the equivalent resistance and capacitance of each switch, and N is the number of bits in the encoder. Therefore the total propagation delay is proportional to the square of the number of bits in the encoder.

A new high-speed implementation for tree-structured DAC encoders is shown in Fig. 1.11 for the 4-bit partially segmented tree-structured encoder of Fig. 1.3. The addition of the GEC PN signal to the DAC input is also done in this block to minimize the total latency. It can be shown that each output of the flash ADC can map to only one encoder output each clock cycle, thus enabling pass-transistor logic to be used. Thus the implementation consists of a Control Logic block that controls a bank of transmission gate switches and a LSB segment switch. The Control Logic block pre-sets the paths (i.e. the switches) from the flash ADC output to the encoder output. The critical path is reduced to a single transmission gate delay, regardless of the number of bits in the encoder.

The Control Logic block effectively performs three tasks to preset the addition when $r_{gec}[n]$ is one, while maintaining thermometer encoding: first it multiplies the flash ADC output by two by just doubling the number of output lines, second it shifts

the lines up, and third it inserts a one in the LSB position. Thus a +1/2 is added at the DAC input, becoming a $+\Delta/4$ after the $-\Delta/4$ offset at the output of the DAC (not shown). The offset is implemented using a switched capacitor. When $r_{gec}[n]$ is zero no shifting occurs, which is equivalent to adding a zero to the DAC input that becomes a $-\Delta/4$ after the offset. When the flash ADC output is full scale positive (denoted by signal f_z in Fig. 1.11) and $r_{gec}[n]$ is one, the Control Logic block operations of shifting all the lines up and forcing the LSB to one has no effect, as this would exceed the available headroom in the DAC. Therefore in this case a zero is added to the DAC input regardless of the value of $r_{gec}[n]$, and the pre-set outputs of the LSB Segment Switch block in Fig. 1.11, c_0 and c_1, must have their values changed. However this only takes approximately two gate delays to occur. The GEC estimation logic of Fig. 1.4 is paused when this occurs to avoid introducing correlation with the flash ADC output.

Although the critical path has been reduced to a single transmission gate, each flash ADC output line will have increased parasitic capacitive loading; however it is small since it comes from switches that are off. For a N-bit unit element tree-structured encoder with $M+1$ levels, where $M=2^N$, the total number of switches is increased to M^2 from $2MN$; however they can be smaller now since they are not in series. There is an increase in digital logic over the previous implementation; however it does not reside in the signal path. Latency has been thus reduced mainly at the expense of increased digital complexity – a desirable tradeoff.

Process, Packaging, and Layout Overview

The IC is fabricated in the TSMC 0.18μ 1P6M mixed-signal CMOS process with MiM capacitors. Separate deep Nwells and multiple voltage supply domains are employed to reduce coupling from digital and analog sections, and to improve isolation within and between the PADC stages. A 56-pin QFN package with an exposed die paddle is used for its good electrical performance and grounding capabilities. Down-bonding of all grounds to the exposed paddle, double-bonding of critical supply pins, and over 5 nF of on-chip decoupling capacitance help reduce power supply bounce. ESD protection circuitry is contained in all pads.

IV. Measurement Results

A printed circuit test board was designed and fabricated and interfaced to a digital data acquisition board to test the PADC. The single-ended output of a low jitter crystal oscillator mounted on the test board is converted to a differential signal via a transformer and used to clock the PADC IC. A high-purity signal generator was used to generate test signals across the 20 MHz Nyquist band of the PADC. For each input frequency, one of a set of five high-quality, custom, discrete-component, bandpass filters was used to further purify the input signal just prior to the test board connection. The test board was designed for two different input signal-path component population options: 1) transformer-based single-to-differential input signal conversion and 2) op-amp based single-to-differential input signal conversion. The transformer option works well for frequencies of 9 MHz and higher, but at lower frequencies the

distortion performance of the transformer is less than that of the PADC. The op-amp option works well for frequencies of 9 MHz and below, but introduces distortion at higher frequencies. Therefore, both options were necessary to measure the performance of the PADC over its full bandwidth.

Fig. 1.12 contains a summary of fabrication and measurement details. Due to a timing error, the digital correction logic needed to be powered from a 2.1-V supply when the chip was operated at 40 MSPS (1.8 V was sufficient at 20 MSPS). The number of samples used in the correlations for the calibration algorithms was 2^{27}. A representative PSD plot from the ADC with and without the calibration techniques enabled for a -1 dBFS 19.03 MHz input signal is shown in Fig. 1.13. Fig. 1.14 shows representative SFDR and THD performance versus input frequency (at -1 dBFS). DNL and INL measurements at 1.01 MHz with calibration disabled and enabled are shown in Fig. 1.15 and Fig. 1.16, respectively. As can be seen from the figures, the calibration techniques result in significant improvements in SNDR, SFDR, DNL and INL. The die photo is shown in Fig. 1.17.

V. CONCLUSION

The first silicon implementation of two new digital background calibration techniques has been presented. The first technique, DNC, compensates for DAC mismatch noise, while the second, GEC, compensates for interstage gain errors. Both techniques operate in the background, transparent to normal converter use, and perform their error estimation and correction completely in the digital domain. Together they drastically reduce analog circuit requirements required to achieve high

performance. They have been shown to be enabling components in a 1.8-V 15-b 40-MSPS PADC.

VI. CHAPTER ACKNOWLEDGEMENTS

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VII. FIGURES

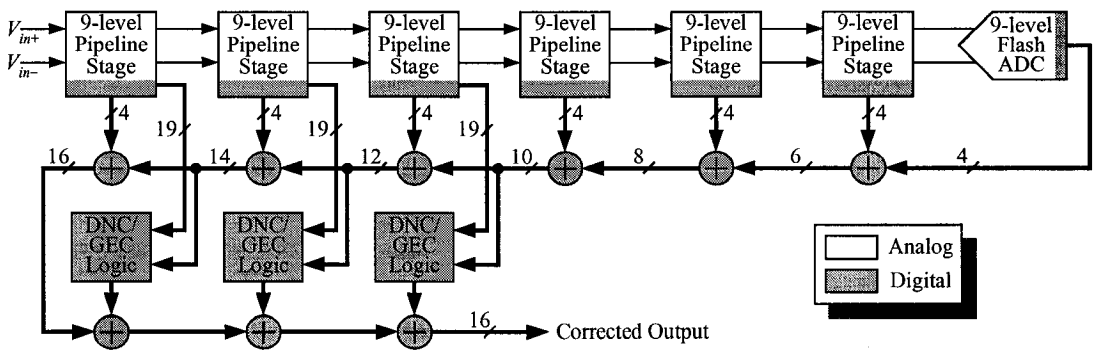

Figure 1.1: Block diagram of the implemented pipelined ADC

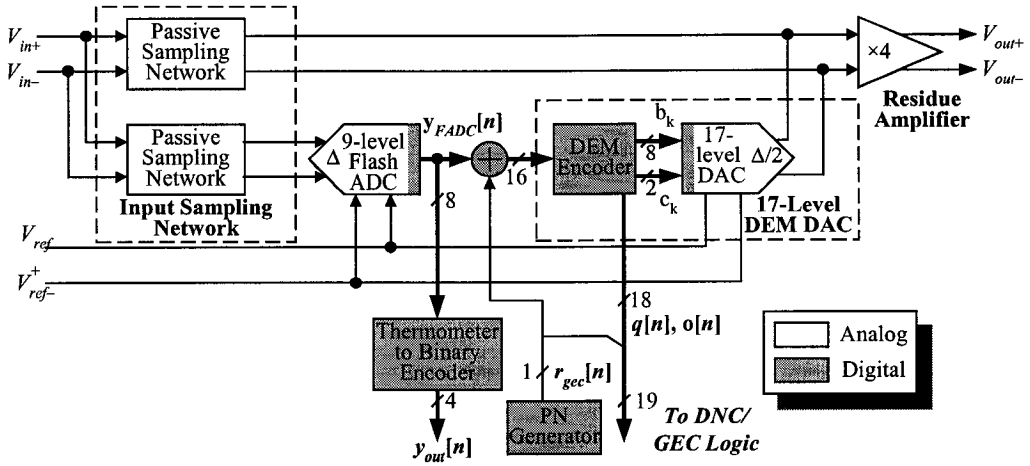

Figure 1.2: Block diagram of a stage employing DNC and GEC

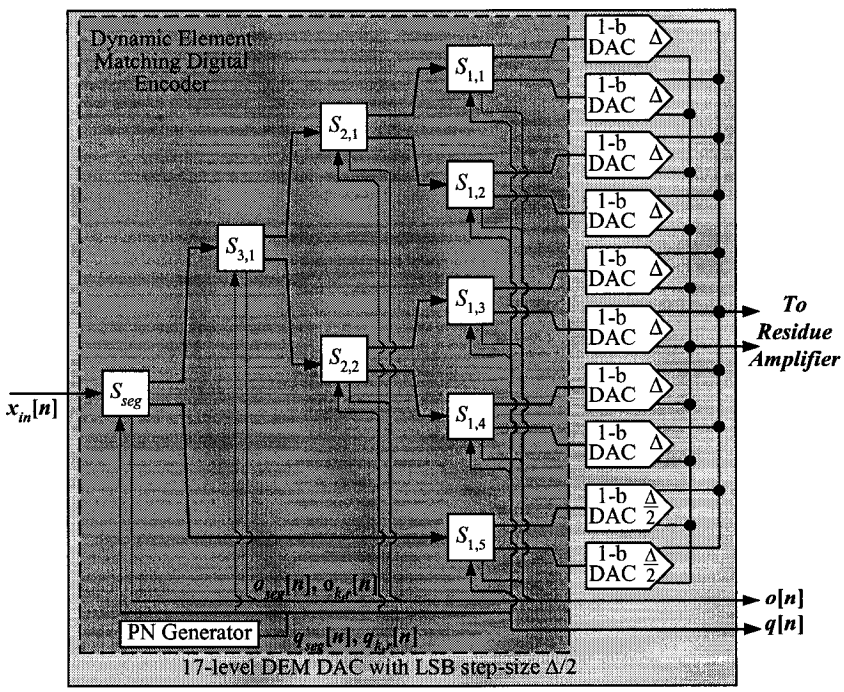

Figure 1.3: Block diagram of the mismatch-scrambling encoder

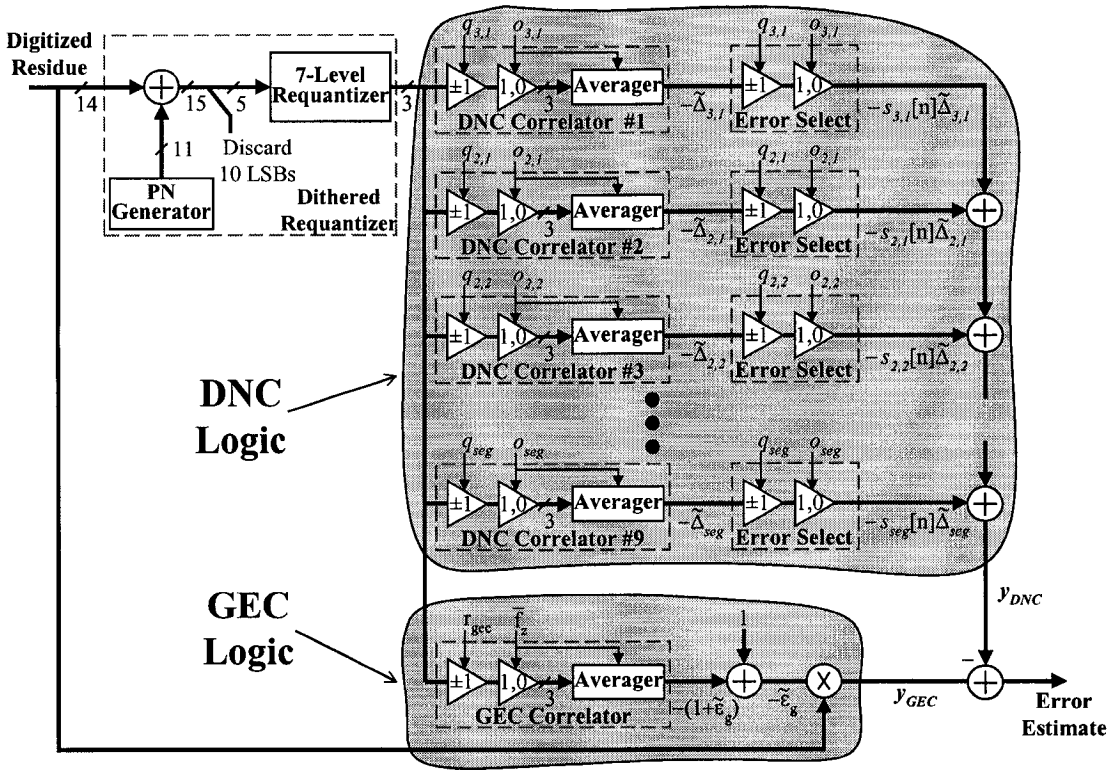

Figure 1.4: High-level diagram of the DNC and GEC estimation and correction logic

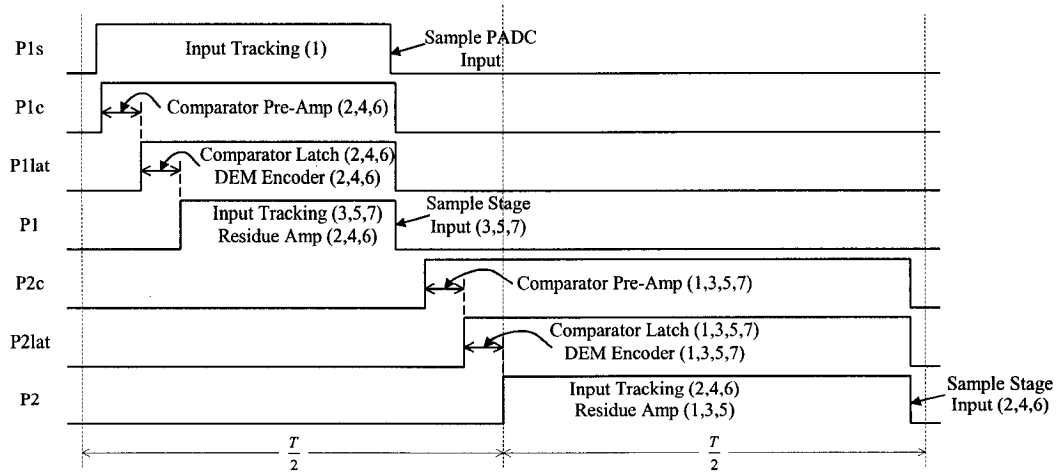

Figure 1.5: Simplified timing diagram of the overall ADC (stage numbers in parenthesis)

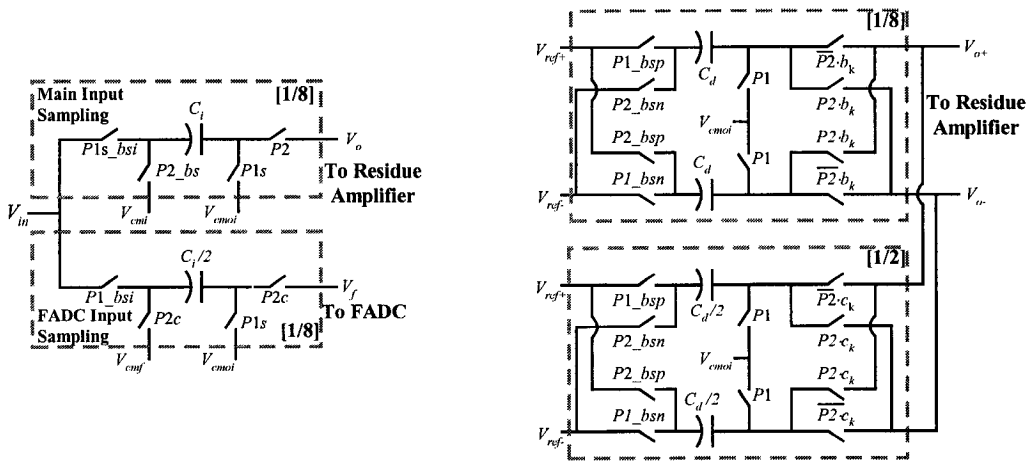

Figure 1.6: Circuit diagram of (a) input and reference sampling network and (b) DAC sampling network

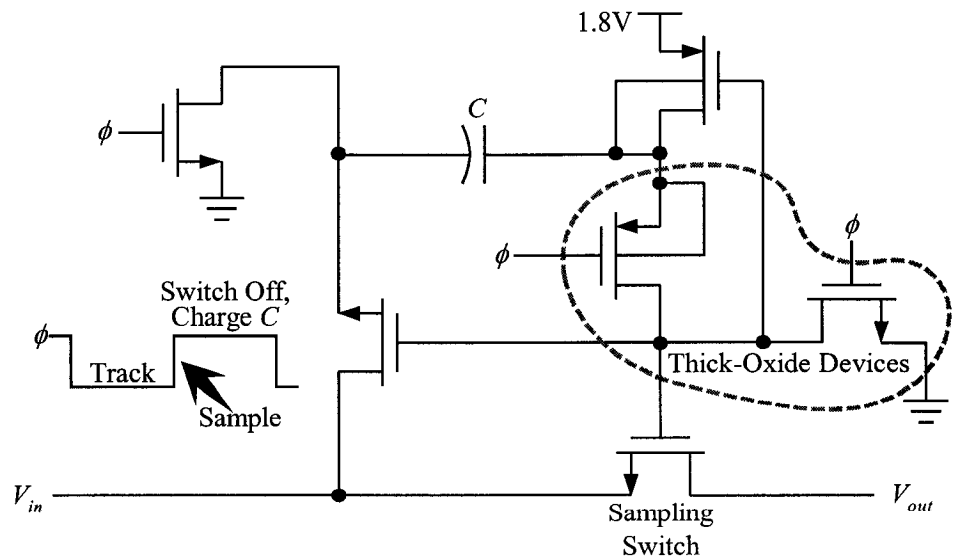

Figure 1.7: Circuit diagram of bootstrapped switch

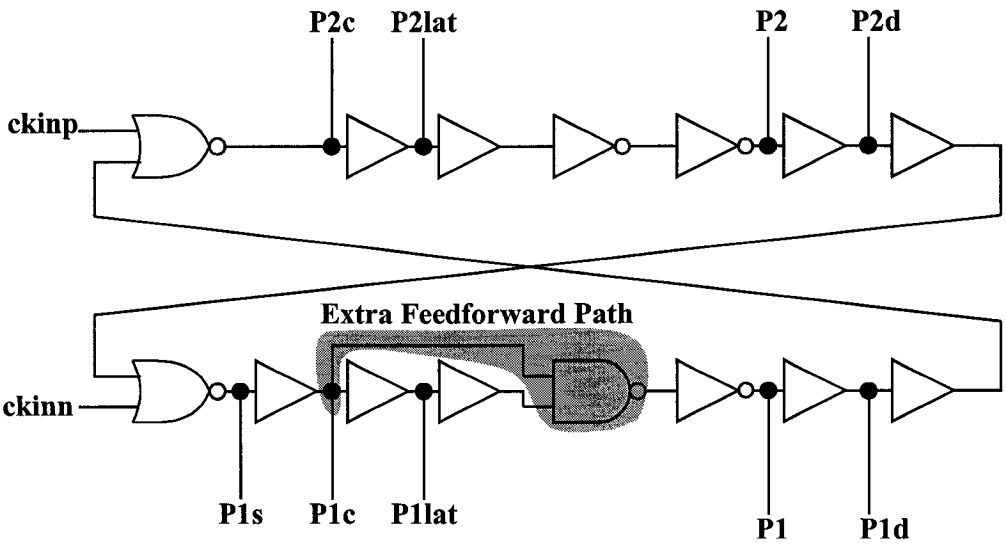

Figure 1.8: Circuit diagram of non-overlapping clock generator

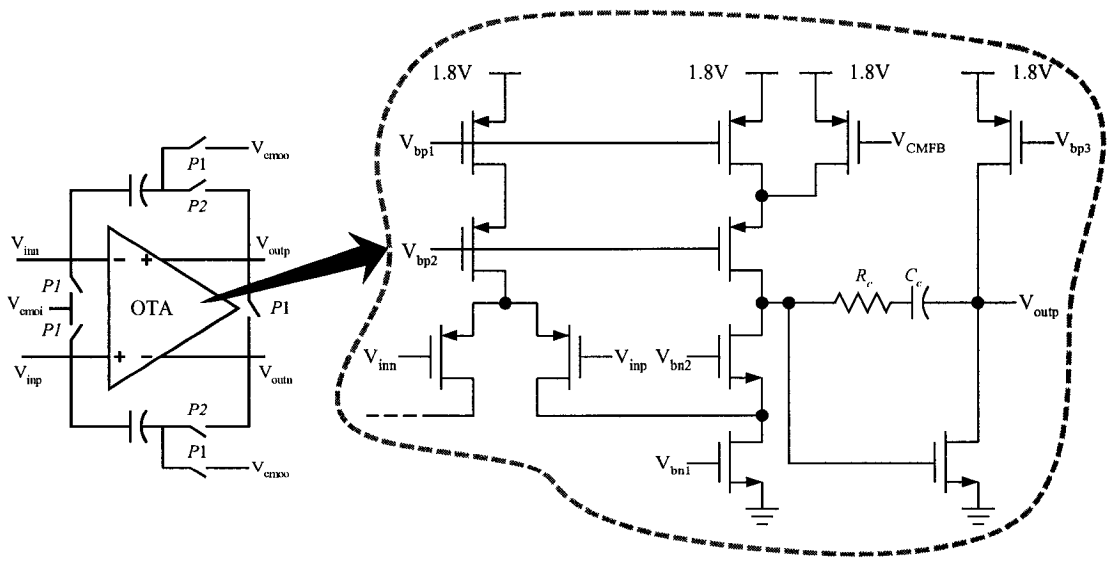

Figure 1.9: Circuit diagram of first stage residue amplifier

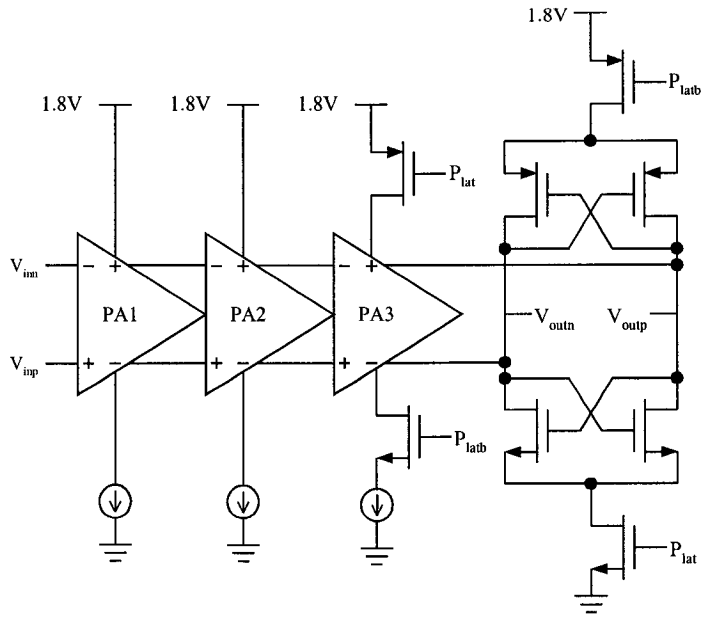

Figure 1.10: Circuit diagram of the comparator

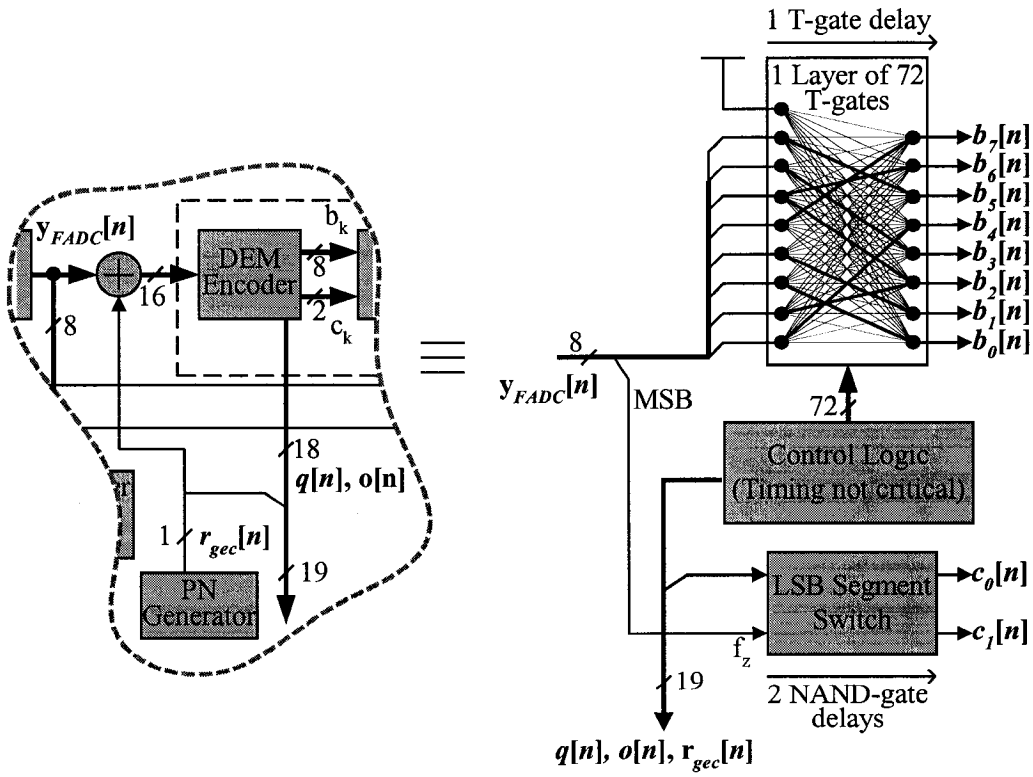

Figure 1.11: Implementation of the DEM DAC digital encoder and $r_{gec}[n]$ insertion

Resolution	15 b
Sample Rate	40 MHz
Input Voltage Range	2.25 Vp-p differential
SFDR	90 dB
THD	88 dB
Peak SNR	72 dB
DNL	0.25 LSB
INL	1.5 LSB
SFDR Improvement With DNC & GEC	> 20 dB
SNDR Improvement With DNC & GEC	> 12 dB
Total Power	400 mW
Analog Power	343 mW
Digital Power	51 mW
Output Drivers	6 mW
Technology	0.18μ 1P6M CMOS
Die Size	4 mm x 5 mm (including pads)
Package	56-Pin QFN with ground downbonding

Figure 1.12: Performance summary table

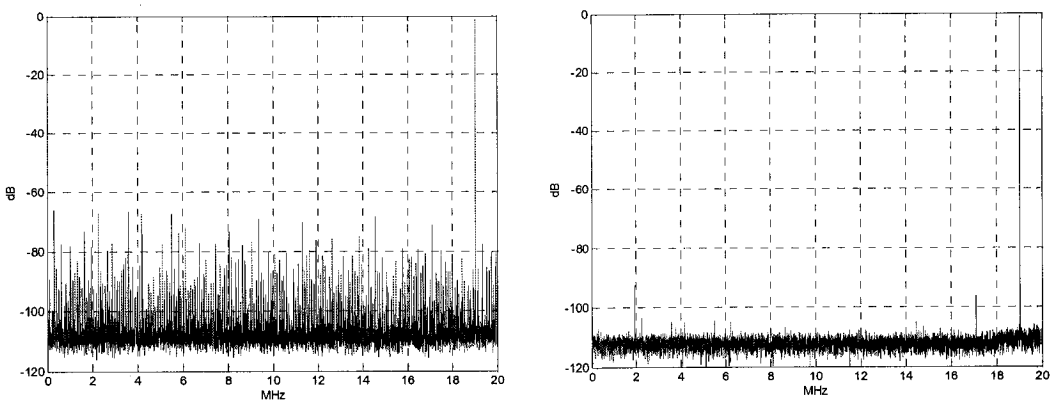

Figure 1.13: Representative measured PSD plot with DNC and GEC (a) disabled and (b) enabled

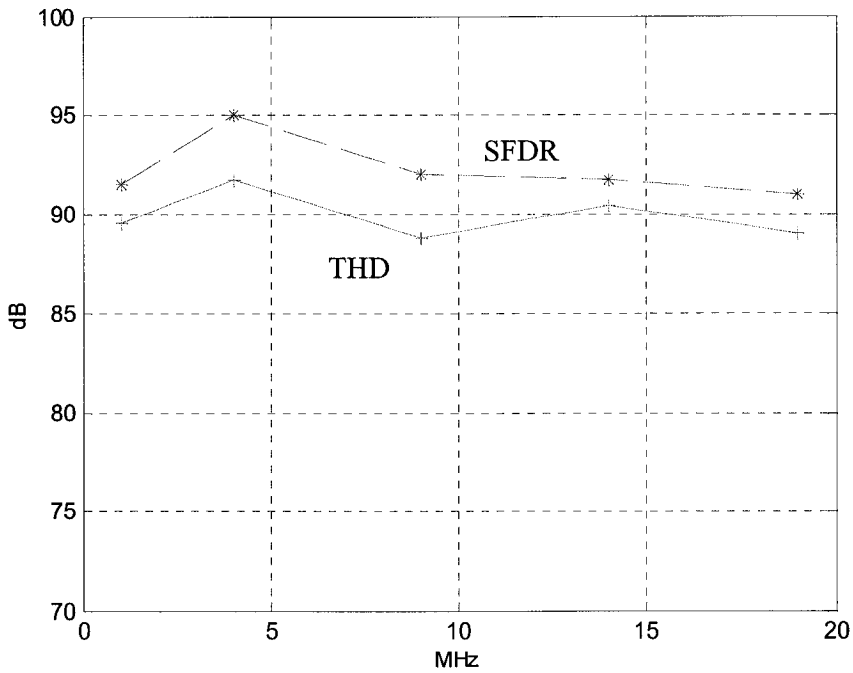

Figure 1.14: Measured SFDR and THD versus input frequency with DNC and GEC enabled

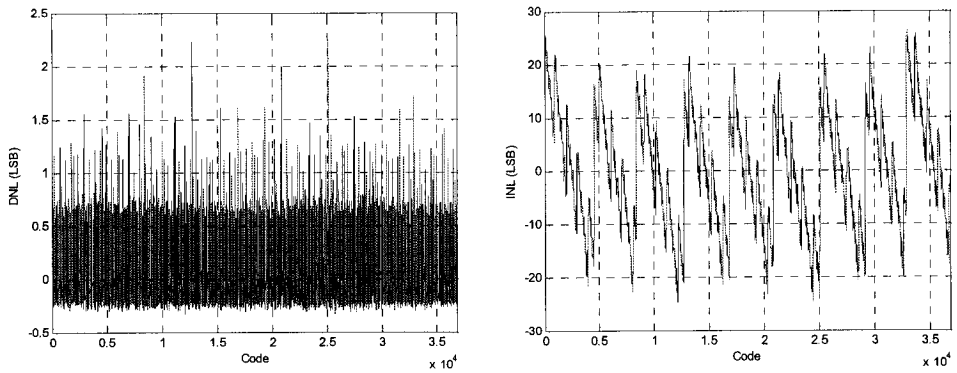

Figure 1.15: Measured DNL and INL with a 1 MHz input with DNC and GEC disabled

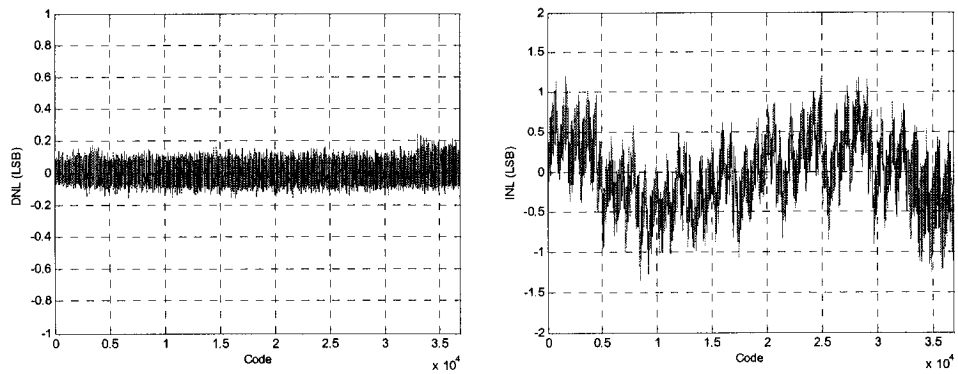

Figure 1.16: Measured DNL and INL with a 1 MHz input with DNC and GEC enabled

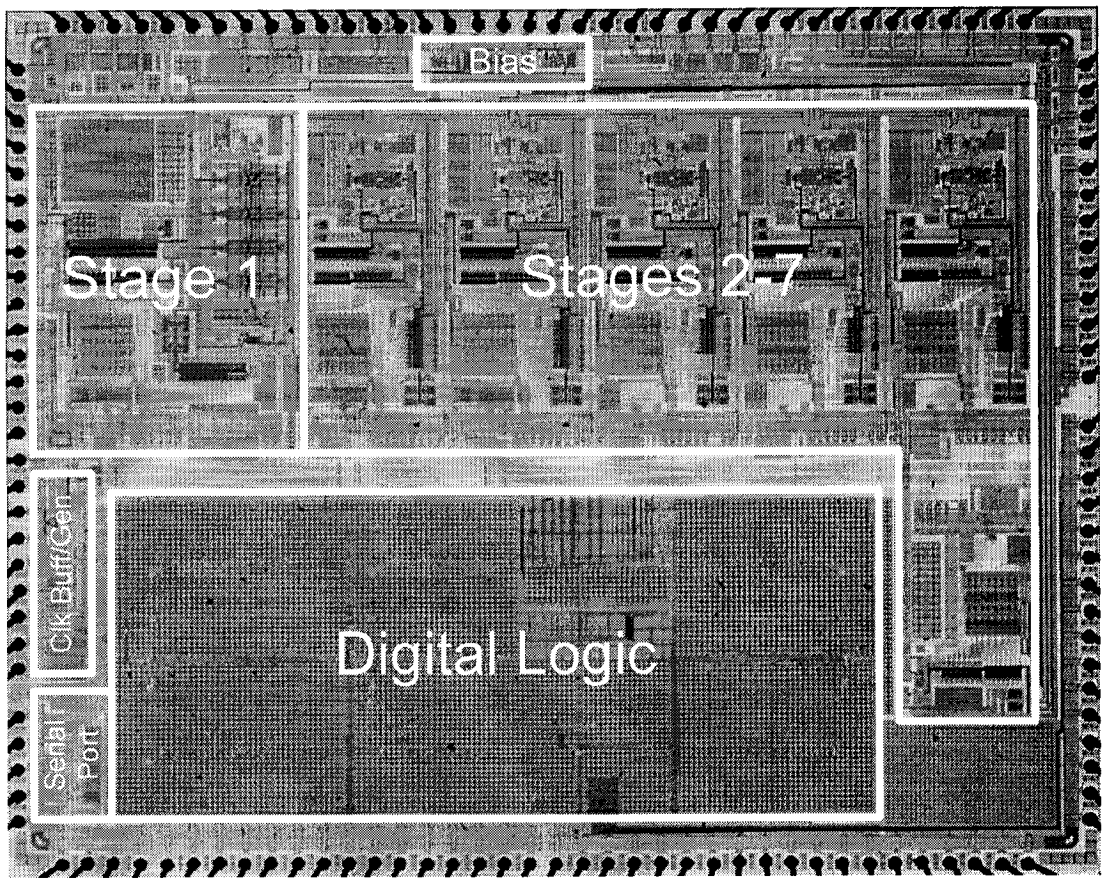

Figure 1.17: Die photograph

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Chapter 2

Gain Error Correction Technique for Pipelined Analog-to-Digital Converters

Eric J. Siragusa and Ian Galton

Abstract—A gain error correction (GEC) technique is presented that continuously measures and digitally compensates for analog gain errors present in each stage of a pipelined analog-to-digital converter (ADC). Simulations with and without the GEC technique indicate that the technique results in a large improvement in the signal-to-noise-and-distortion (SINAD) and spurious-free-dynamic-range (SFDR) of the converter.

I. INTRODUCTION

Throughout the paper, the 4-stage pipelined ADC in Fig. 2.1 is used to demonstrate the GEC technique. Except for the last stage which contains only a 33-level flash ADC, each stage of the pipeline contains a 17-level flash ADC, a 17-level switched-capacitor (SC) digital-to-analog converter (DAC), a summing node, and an interstage gain block. The gains A_i, i = 1, 2, 3, represent the digital scaling necessary to correctly align the digital outputs from each stage. The analog output of a stage, referred to as the residue, is a sign-inverted and amplified version of the stage's ADC quantization noise. Subsequent stages of the pipeline digitize the residue, and the digital outputs of all the stages are combined. Ideally this generates a high precision digital representation of the input signal.

For the purpose of demonstrating the GEC technique it is assumed throughout the paper that gain errors are the dominant contributors to the overall pipelined ADC

error. In particular, it is assumed that the sample-and-hold amplifier (SHA) at the converter input and the op-amps in the switched-capacitor circuits do not limit overall performance. It is also assumed that the DAC signal-dependent errors (which are usually the dominant source of error [1]) have been corrected by another technique such as the one presented in [2]. It can be shown that each stage's ADC errors have virtually no effect on the overall pipelined ADC performance provided they do not cause the input range of the following stage to be exceeded [1]. To leave margin for the flash ADC errors, the interstage gains are chosen such that the maximum swing of the residue, in the absence of flash ADC errors, is half the allowable input range of the next stage.

II. GEC TECHNIQUE

As shown below, gain errors cause incomplete cancellation of the quantization noise from each stage's coarse ADC, which leads to a reduction in the overall converter's SINAD and SFDR. For example, errors in the DAC gain and interstage gain in the first stage, and the error in the overall gain in the remaining stages cause the quantization noise from the first-stage's ADC to not be completely cancelled.

A simplified example wherein the GEC technique is applied only to the first stage is shown in Fig. 2.2. Stages 2-4 constitute a pipelined ADC in their own right and are modeled as a single ADC. To implement GEC a pseudo-random ±1 signal $r_0[n]$ is scaled by 1/4 and added to the output of the first-stage ADC in order to travel the same paths that the first-stage quantization noise travels. Note that the resolution of the DAC must be increased to accommodate the ±1/4 signal, and half the extra input range

of the next stage is consumed.

The details of the block labeled GEC LOGIC are shown in Fig. 2.3. The digitized residue of the first stage, $R_0[n]$, is correlated against $r_0[n]$ and scaled to obtain an estimate of the normalized gain, called $\tilde{\alpha}_q$, in the path traveled by the quantization noise. Thus

$$\tilde{\alpha}_q = \left(\frac{1}{A_0/4}\right)\frac{1}{N}\sum_{n=1}^{N} R_0[n]r_0[n] = 1 + \tilde{\varepsilon}_q \tag{1}$$

where N is the total number of samples in the correlation and $\tilde{\varepsilon}_q$ is the gain error estimate. The digitized residue is then divided by the gain estimate to better eliminate the first-stage quantization noise in the final output. A related idea was presented in [3], however it is not an all-digital solution like the one presented here.

Behavioral C-language simulations of the pipelined ADC were performed using realistic values for non-ideal circuit behavior. The reference voltages for each flash ADC were generated by a simulated resistor ladder wherein each resistor was chosen with a random error of 0.3% standard deviation, and the offset voltage of each comparator in the ADC was chosen randomly with a standard deviation of 10 mV. For the first stage DAC and first-stage interstage gain, fixed errors of +0.5% were chosen to give a worst case condition where the gain errors have the same polarity. The interstage gains for the second and third stages were chosen with a random error of 0.3% standard deviation. Except for the first-stage DAC gain error, the first and second stage DACs were ideal, as it was assumed that another technique was used to correct them if necessary. Mismatches in the third stage 17-level DAC were modeled by selecting the two output voltages corresponding to each one-bit DAC with random

errors of 0.3% standard deviation.

Fig. 2.4 shows the power spectral density (PSD) of the converter output before and after application of the GEC technique. Use of the GEC technique resulted in a 17dB improvement in SINAD and a 28dB improvement in SFDR. The number of samples used in the correlation to produce the gain estimate was 2^{25}. For a 10MHz sample rate converter, this corresponds to a 3.2 second warm-up period, during which the converter can still be operated normally. The PSDs were performed on the converter output data after completion of the warm-up period.

III. THEORY

In the absence of GEC, it can be shown using Fig. 2.2 that the overall pipelined ADC output is

$$y[n] = \alpha_x x[n] + A_0[1-\alpha_q]e_{q0}[n] + \alpha_d e_{d0}[n] + e_{q1}[n] \tag{2}$$

where $x[n]$ is the input to the converter, $e_{q0}[n]$ is the first-stage quantization noise, $e_{d0}[n]$is the first-stage DAC noise error, $e_{q1}[n]$ is the quantization noise from the remaining stages, α_x is the overall pipelined ADC converter gain, α_d is the gain from the DAC output to the overall pipelined ADC converter output, and α_q is the gain from the ADC output to the digitized residue. With GEC, it can be shown that the corrected output is

$$y[n] = \alpha_{x'} x[n] + A_0\left[1-\frac{\alpha_q}{\tilde{\alpha}_q}\right]\left(e_{q0}[n] + \frac{r_0[n]}{4}\right) + \frac{\alpha_d}{\tilde{\alpha}_q} e_{d0}[n] + \frac{e_{q1}[n]}{\tilde{\alpha}_q} \tag{3}$$

where $\alpha_{x'}$ is the new converter gain, which is approximately equal to α_x. Thus for

perfect gain estimation, $e_{q0}[n]$ is completely cancelled. The GEC also causes slight changes to the coefficients of the other signals, which is usually acceptable as it does not significantly degrade the SINAD or SFDR.

Provided $r_0[n]$ is uncorrelated with the other signals present in $R_0[n]$, it can be shown that $\tilde{\alpha}_q$ is an unbiased estimator for α_q, and that the Law of Large Numbers guarantees its convergence with probability 1 as the number of samples taken in the correlation approaches infinity. Therefore, in the limit as $N \to \infty$, $e_{q0}[n]$ is completely cancelled. In practice the number of samples chosen for the length of the correlation depends on the magnitude of $r_0[n]$ relative to the magnitudes of the other signals in $R_0[n]$, and how close $\tilde{\alpha}_q$ is required to be to α_q.

IV. Implementation Issues

Although a specific simplified example has been shown, the GEC technique can be applied to other pipelined ADC architectures, and it can be applied to more than one stage. Other magnitudes of the random signal may also be used, as long as the input range of the next stage is not exceeded. In order to avoid increasing the resolution of the DAC, the random signal can be added to the input of a stage's ADC instead of at its output. However, since gain of the ADC would be in the path of the random signal, an additional correlation would be needed at the stage's digital output in order to determine this gain. This random signal can be created by adding an offset to the ADC that can be toggled. For example, the number of resistors in the reference ladder for the flash ADC can be increased (without changing the total resistance) and the reference inputs of the comparators can be randomly switched up or down the

ladder to produce the offset.

V. CHAPTER ACKNOWLEDGEMENTS

The text of this chapter appeared as a Letter in *Electronics Letters*, vol. 36, no. 7, March 30, 2000. It has been updated to reflect advances in the field since publication. The dissertation author was the primary researcher. Ian Galton supervised the research that forms the basis of the chapter.

VI. FIGURES

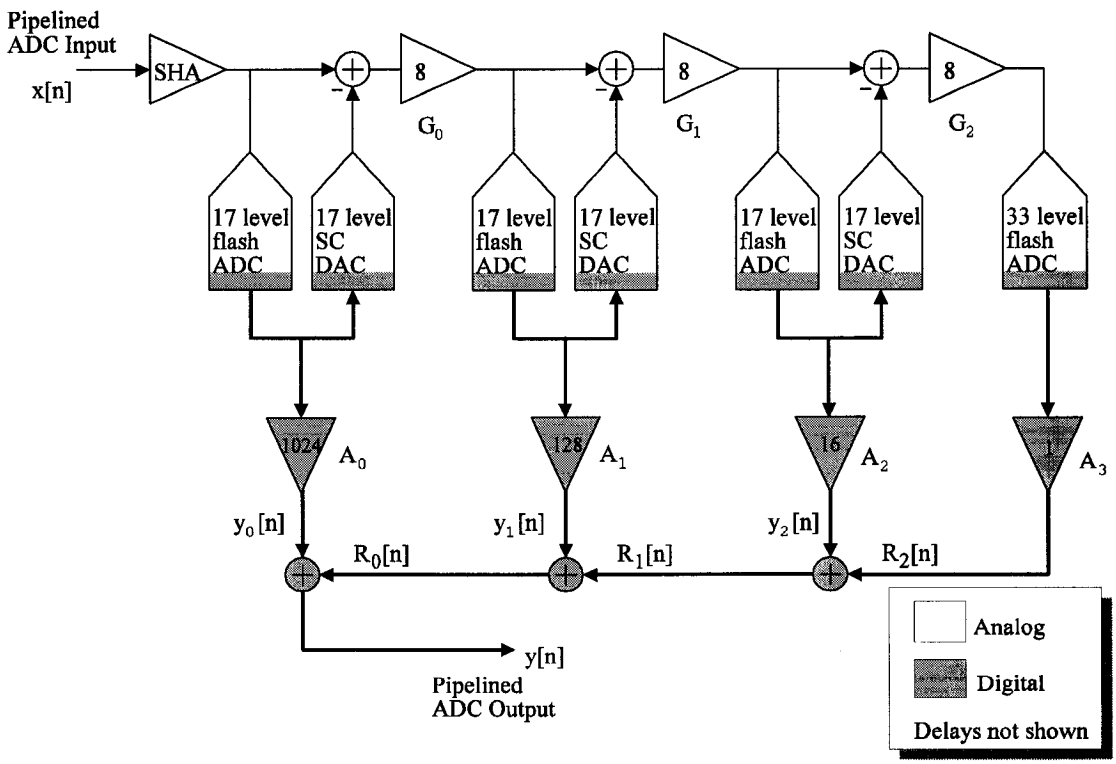

Figure 2.1: An example 4-Stage pipelined ADC

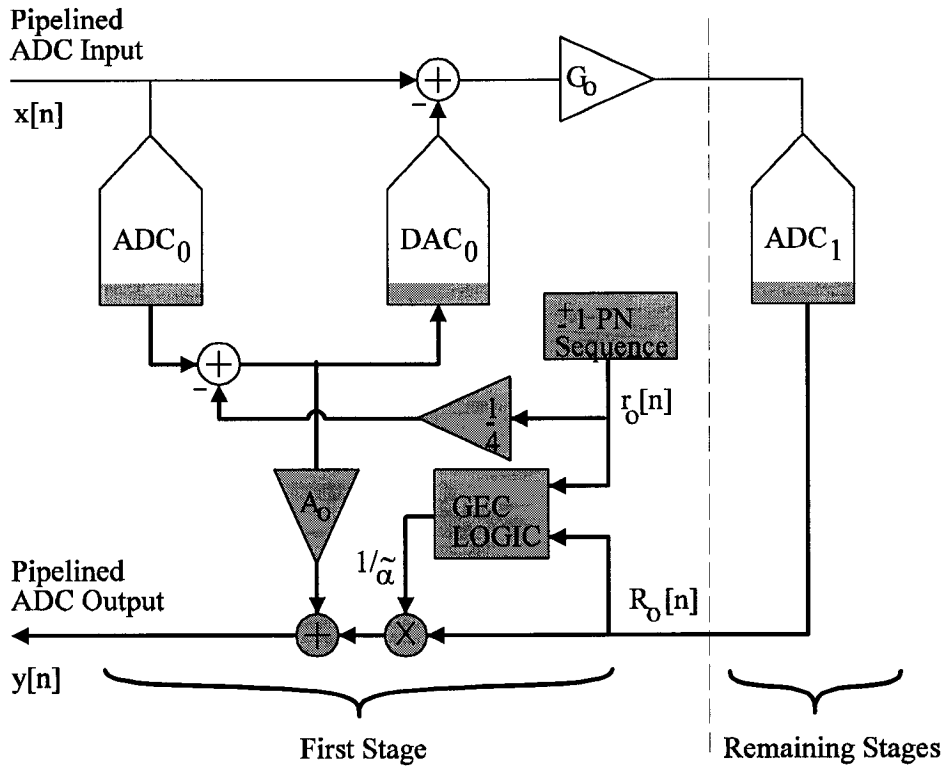

Figure 2.2: Simplified model of the pipelined ADC with GEC

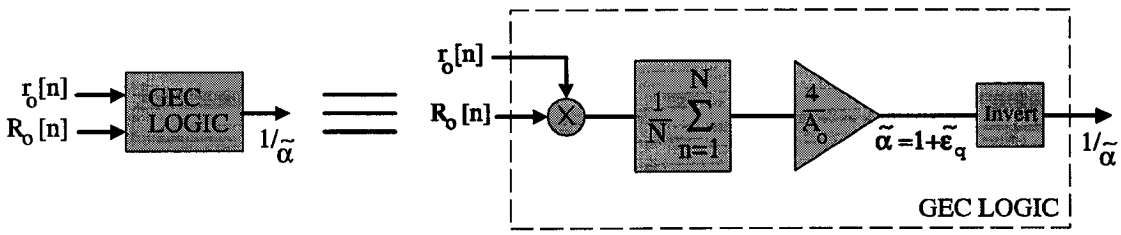

Figure 2.3: GEC logic

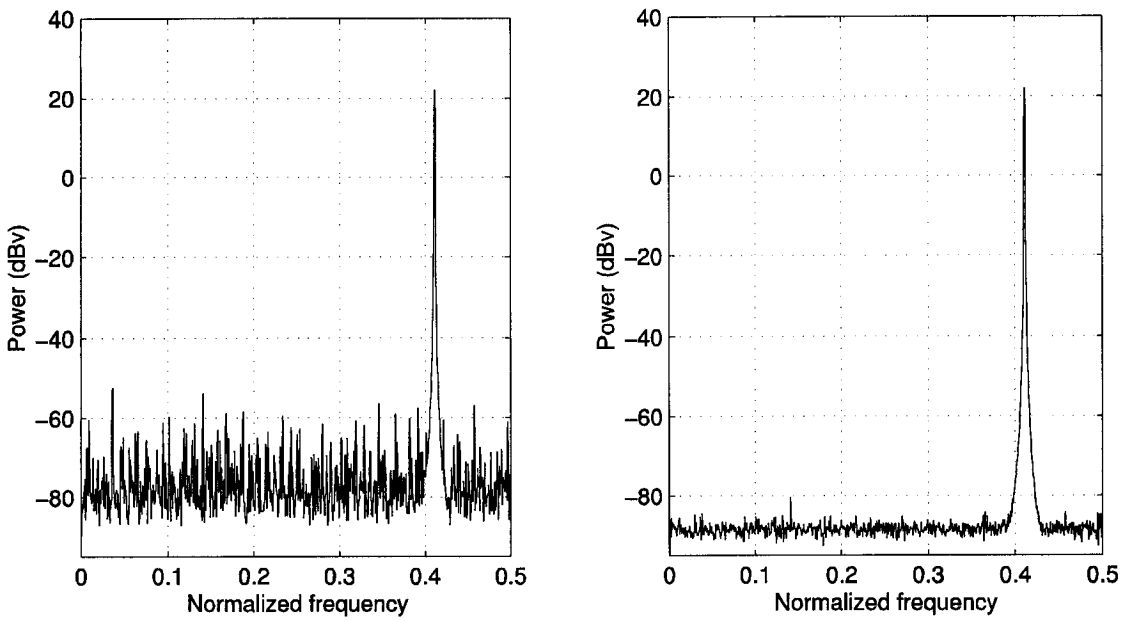

Figure 2.4: Power spectral density plots of the output of the pipelined ADC a) without GEC and b) with GEC

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Chapter 3

Segmented Tree-Structured Dynamic Element Matching DACs

Eric J. Siragusa, Ian Galton, Jared Welz, Eric Fogleman

Abstract— Tree-structured DACs have recently been used as enabling components in state-of-the-art ΔΣADCs and pipelined ADCs to suppress error arising from mismatches among fabricated DAC components. This paper presents a modification to the basic tree-structure that results in a segmented version of the architecture with reduced hardware complexity.

I. INTRODUCTION

Dynamic element matching (DEM) techniques that cause error arising from static component mismatches to be spectrally shaped or whitened are commonly applied to the coarse DACs within delta-sigma (ΔΣ) data converters and pipelined ADCs. Various DEM DAC architectures have been used in these applications, but most belong to a class of DACs that each consist of a digital encoder followed by a bank of unity-weighted one-bit DACs. Tree-structured DACs are the most area-efficient members of this class known to the authors, and have been used as enabling components in state-of-the-art ΔΣ and pipelined ADCs [1], [2], [3]. Nevertheless, as the number of DAC bits, b, increases, the circuit area required by any DAC in this class becomes prohibitive because 2^b one-bit DACs are required. A technique that circumvents this problem has been presented recently that combines two DEM DACs with different weights to create a *segmented* DEM DAC [4],[5]. This paper extends

the technique by showing that the original tree-structured DAC topology can be converted in various ways to form segmented tree-structured DACs that retain the desired DEM properties but have reduced hardware complexity.

II. ORIGINAL TREE-STRUCTURED DAC TOPOLOGY

A 9-level version of the original tree-structured DAC is shown in Fig. 3.1. It consists of a digital encoder followed by a bank of 8 one-bit DACs whose analog outputs are summed to generate the overall output, $y[n]$. For this example, the input sequence, $x[n]$, is restricted to the set $\{-4,-3,\cdots,4\}$. During each sample interval the digital encoder sets $4+x[n]$ of its output bits high and $4-x[n]$ of its output bits low. Each one-bit DAC generates an analog output given by $\Delta/2+e_{h_i}$ if its input bit is high, and $-\Delta/2+e_{l_i}$ if its input bit is low, where Δ is the nominal step-size, and e_{h_i} and e_{l_i} are the high and low one-bit DAC errors, respectively. By convention, throughout this paper the one-bit DAC input value is interpreted to be ½ when the input bit is high and –½ when the input bit is low. As shown in [6], in this case the overall DAC output has the form $y[n]=\alpha x[n]+e[n]+\beta$, where α is a constant gain, β is a constant offset, and $e[n]$ is *DAC noise* that depends upon the input sequence and the one-bit DAC errors in general.

The purpose of the digital encoder is to cause $e[n]$ to be white or spectrally shaped as required by the application. The digital encoder consists of *switching blocks*, labeled $S_{k,r}$, with $1\le k\le 3, 1\le r\le 4$ in Fig. 3.1, and arranged in a tree-like formation. Each switching block generates a top output and a bottom output given by

$$x_{k-1,2r-1}[n] = \frac{1}{2}\left(x_{k,r}[n] + s_{k,r}[n]\right), \text{ and}$$
$$x_{k-1,2r}[n] = \frac{1}{2}\left(x_{k,r}[n] - s_{k,r}[n]\right), \tag{1}$$

respectively, where $x_{k,r}[n]$ is the switching block input, and $s_{k,r}[n]$ is a *switching sequence* generated within the switching block. If $s_{k,r}[n]$ is such that the switching block outputs are in the set $\{-2^{k-2}, -2^{k-2}+1, \cdots, 2^{k-2}\}$ then the switching block is said to satisfy the *number conservation rule*. As shown in [6], provided the number conservation rule is satisfied by all the switching blocks, the DAC noise is given by

$$e[n] = \sum_{k=1}^{3} \sum_{r=1}^{2^{3-k}} s_{k,r}[n] \Delta_{k,r} \tag{2}$$

where the $\Delta_{k,r}$ are constants that depend only on the one-bit DAC errors. Thus, to cause the DAC noise to have a specific spectral property (*e.g.*, to be white noise), all the switching sequences must be chosen to satisfy the number conservation rule *and* have the desired spectral property.

III. SEGMENTED TREE-STRUCTURED DAC TOPOLOGY

A 33-level segmented tree-structured DAC is shown in Fig. 3.2. The segmented structure is obtained from an original tree structure by choosing certain switching sequences to reduce hardware complexity while maintaining the desired DEM properties. Note that only 9 switching blocks and 10 one-bit DACs (weighted) are needed in the segmented topology of Fig. 3.2, as compared to the 31 switching blocks and 32 one-bit DACs that would be needed for a 33-level version of the original

topology. This yields a potentially large savings in the circuit area required by the DAC.

To demonstrate how a segmented tree-structured DAC is obtained from an original tree-structured DAC, a simpler 5-level segmented structure will be generated. Although the 5-level segmented structure does not provide a reduction in hardware complexity over a 5-level original tree structure, it does provide a simple vehicle with which to explain the conversion process. The conversion process can then be used on structures with larger numbers of levels to achieve large savings in complexity. A 9-level original tree structured DAC with its input sequence restricted to 5 levels is used as the starting point.

Suppose that the $S_{3,1}$ switching block in Fig. 3.1 is such that its top output is quantized to be an even number. In this case, $x_{2,1}[n] = x[n] + \varepsilon[n]$ and $x_{2,2}[n] = -\varepsilon[n]$, where $\varepsilon[n]$ is quantization error in the range $\{-1,0,1\}$. It follows from (1) that this is achieved if the switching sequence is chosen to be $s_{3,1}[n] = x[n] + 2\varepsilon[n]$. In practice, a digital dithered quantizer or digital delta-sigma modulator can be used to generate a white or spectrally shaped version of $\varepsilon[n]$ such that the number conservation rule is still satisfied by the switching block. Either way, it follows from (2) that the DAC noise, $e[n]$, contains scaled versions of both $x[n]$ and $\varepsilon[n]$. The presence of the $x[n]$ term just affects the gain of the overall DAC, and, by design, the $\varepsilon[n]$ term has the spectral properties desired of the DAC noise. Therefore, this choice of switching sequence is both practical and acceptable from the point of view of maintaining the desired DEM behavior of the tree-structured DAC.

With the above $S_{3,1}$ switching sequence choice, the input to the top sub-DAC and thus to the $S_{2,1}$ switching block is always an even number. This makes it possible to fix the $S_{2,1}$ switching sequence to be zero without violating the number conservation rule, which, as follows from (1), causes the two outputs of the $S_{2,1}$ switching block to always be equal. The same switching sequence can be used in both switching blocks $S_{1,1}$ and $S_{1,2}$ without violating the number conservation rule because both switching blocks share a common input sequence. Since, in this case, the switching blocks are identical with identical input sequences, both sets of two one-bit DACs in the top sub-DAC can share the same switching block logic. Moreover, since both sets of two one-bit DACs share a common set of one-bit input sequences, they can be combined into a single set of two one-bit DACs each with a step-size of 2Δ instead of Δ.

The above choice of $s_{3,1}[n]$ also allows the hardware complexity of the bottom sub-DAC of Fig. 3.1 to be reduced. As shown above, $x_{2,2}[n]$, the input to switching block $S_{2,2}$, is restricted to the range $\{-1,0,1\}$. This implies that $x_{2,2}[n]$ could be applied directly to a switching block in the final layer (*e.g.* $S_{1,3}$) without violating the number conversion rule along the way. Explicitly, if switching sequence $s_{2,2}[n]$ is chosen such that $s_{2,2}[n] = x_{2,2}[n] = -\varepsilon[n]$, the top output of $S_{2,2}$, which drives switching block $S_{1,3}$, is equal to $x_{2,2}[n]$. Furthermore, the bottom output $x_{1,4}[n]$ is zero for all n, which implies that switching block $S_{1,4}$ and its corresponding DACs need not be used. The final 5-level segmented tree-structured DAC is shown in Fig.

3.3.

The process illustrated above is one of many possible ways that the original tree structured DAC topology can be converted into a segmented structure. For appropriately sized original tree-structured DACs, a switching sequence can be chosen to force the top output of a switching block to a multiple of a number such as 4, instead of 2 as was done in the example above. As in the example above, the signal $x[n]$ is completely contained in the top output, while the quantization error $\varepsilon[n]$ is contained in both outputs. Other choices of switching sequences can result in varying amounts of the signal and error in both outputs. Although not necessary in the simple example above, these techniques can be recursively applied to sub-DACs in larger original tree-structured DACs. Furthermore, it is not necessary to convert the entire DAC into a segmented structure. If the switching sequences are chosen properly, all the various segmented structures can retain the desired DEM properties of the original but have reduced hardware complexity.

IV. CHAPTER ACKNOWLEDGEMENTS

The material of this chapter appeared as a part of the Conference Paper "Segmented mismatch-shaping D/A conversion," *Proceedings of the IEEE International Symposium on Circuits and Systems,* vol. 4, pp. 26-29 May 2002. The dissertation author was the primary researcher of the material in this chapter and the co-authors listed in this chapter directed and supervised the research that forms the basis of the chapter.

V. FIGURES

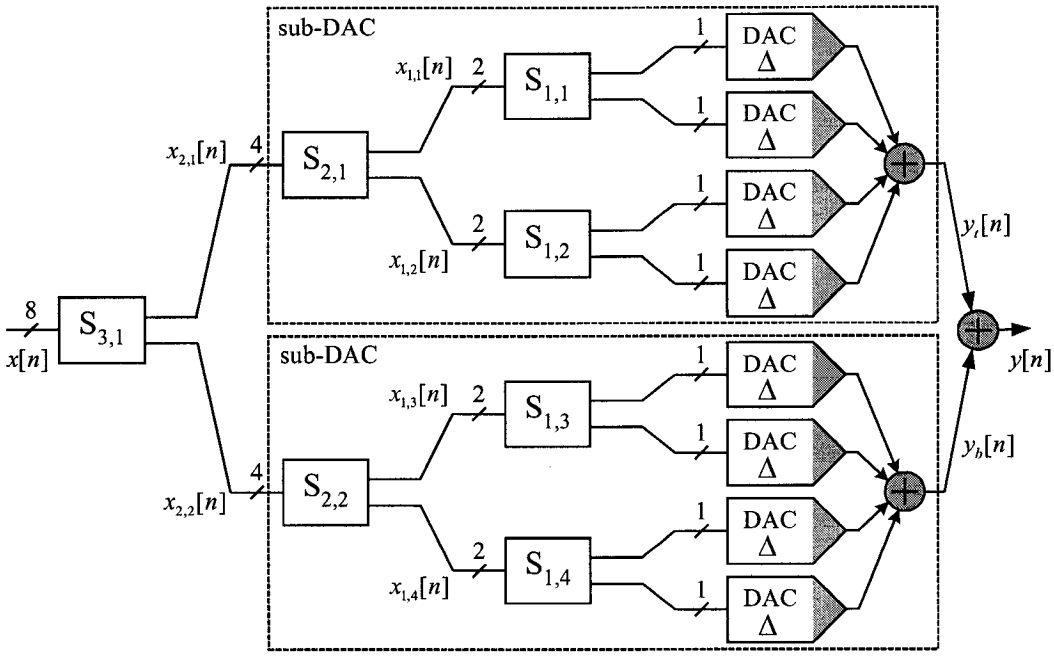

Figure 3.1: 9-Level Original Tree-Structured DEM DAC

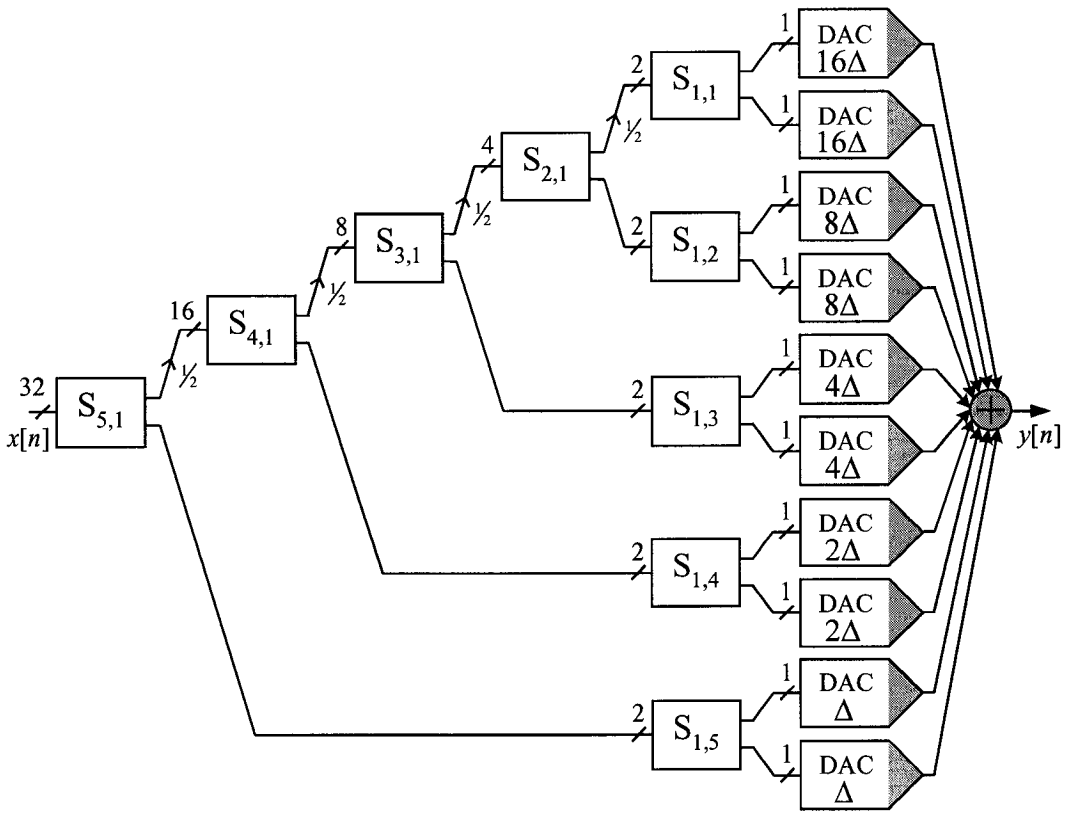

Figure 3.2: 33-Level Segmented DEM DAC

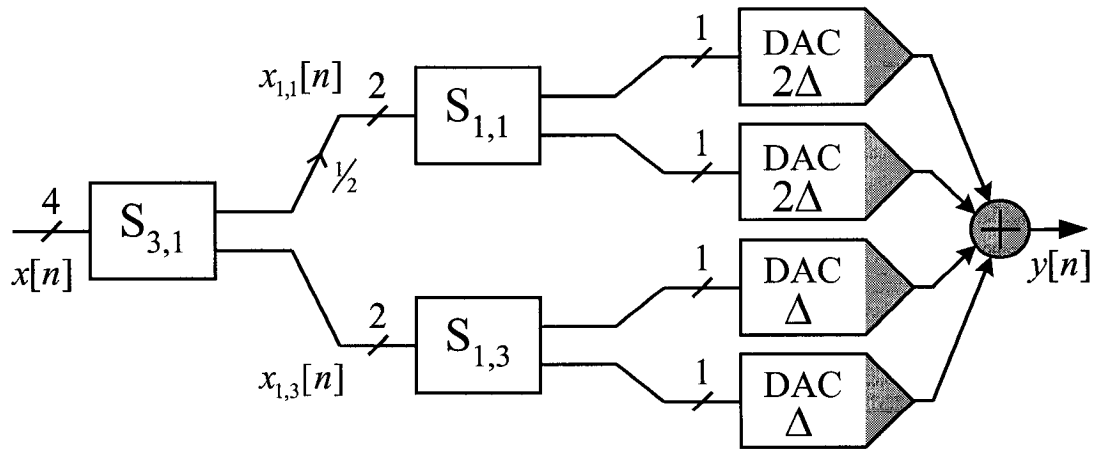

Figure 3.3: 5-Level Segmented DEM DAC

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