Techniques for Phase Noise Suppression in Recirculating DLLs

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***Abstract*—This paper presents two techniques for reducing phase noise in recirculating delay-locked loops (DLLs) and extends recently developed theoretical results to optimize the performance of a recirculating DLL prototype CMOS IC incorporating the techniques. One of the techniques reduces $1/f$ noise in both the voltage-controlled oscillator (VCO) and bias circuitry through hard periodic switching of key transistors. The other technique maximizes the phase noise suppression achieved by periodically switching in a clean reference pulse to reset the VCO phase noise memory. Theoretical results are used to optimize the loop filter and establish several general design guidelines for recirculating DLLs. Measured performance data from the fabricated IC with and without the techniques enabled closely support the theoretical predictions.**

***Index Terms*—Delay-locked loop (DLL), frequency synthesizers, phase noise, phase-locked loop (PLL).**

I. Introduction

FREQUENCY synthesizers are critical building blocks in communication systems. Ring-oscillator-based voltage-controlled oscillators (VCOs) are widely used in low-performance frequency synthesizer applications such as clock multiplication for digital systems because of their simplicity, wide tuning range, and ease of integration. However, they are less commonly used in applications which are sensitive to phase noise such as communication systems, because they tend to introduce excessive close-in phase noise. In a conventional phase-locked loop (PLL) frequency synthesizer, the loop bandwidth is usually constrained to less than 5% of the reference frequency to maintain stability across process and temperature extremes, so the PLL only provides limited attenuation of the VCO phase noise.

To overcome this conventional barrier, the VCO output can be aligned periodically to a clean reference pulse so as to reset the phase error and thereby suppress the noise memory caused by the jitter accumulation effect in the VCO. The result is significant attenuation of the in-band phase noise. Precisely speaking, the term "in-band" refers to the frequency within the loop bandwidth in most applications. In this paper, however, it refers to the close-in frequency because even for the same reference frequency, the effective loop bandwidth of a PLL and a recirculating delay-locked loop (DLL) are significantly different. The noise reduction technique, referred to as *phase realignment* in the remainder of this paper, can be implemented in various ways. In a DLL-based clock multiplier, the delay of a voltage-controlled delay line (VCDL) is locked to the reference period [1]. Multiple delayed versions of the reference clock from the VCDL are then combined to produce the final clock signal, as shown in Fig. 1(a). The delayed reference is discarded at the end of the VCDL, so the phase realignment is performed naturally by design. Another type of DLL, referred to as a *recirculating DLL* in the remainder of the paper, is implemented using a ring VCO with the phase realignment performed by periodically opening the ring to discard the noisy VCO edge and replacing it with a clean reference edge, as shown in Fig. 1(b) [2]. Alternatively, in a *realigned PLL* (RPLL), shown in Fig. 1(c), the phase realignment is performed by directly coupling a strongly buffered version of a clean reference source into one of the inverters in the VCO [3]. The strong buffer overpowers the VCO inverter so that the VCO phase is "dragged" toward the correct position.

Ideally, the phase realignment completely suppresses the noise memory. However, as demonstrated in [3], in both recirculating DLLs and RPLLs, parasitic coupling among the delay cells in the VCO tends to degrade the phase realignment and leads to incomplete noise memory suppression. Therefore, the choice of VCO topology is critical in effectively implementing the phase realignment technique.

At the device level, flicker noise, also known as $1/f$ noise, tends to severely degrade the in-band phase noise performance of the VCO. As will be explained in detail in Section III, $1/f$ noise can be suppressed by periodically switching the associated transistors on and off so as to suppress the long-term noise correlation, as reported in [4]–[6].

This paper presents, analyzes, and experimentally demonstrates a recirculating DLL IC with techniques applied to the VCO and bias circuits that reduce $1/f$ noise and result in nearly ideal phase realignment [7]. The theoretical results presented in [3] are extended to the DLL topology and used to establish several general design guidelines applicable to recirculating DLLs that, to the knowledge of the authors, are not well known.

The remainder of this paper consists of four main sections. The phase realignment theory from [3] is applied to provide design guidelines and optimize the loop parameters in Section II. The underlying physics of the switched biasing technique is reviewed and compared with the phase realignment in Section III. The circuit details of the DLL are presented, and the techniques used to suppress $1/f$ noise and improve the phase realignment are described in Section IV. Measurement results from the fabricated IC are presented and compared to theoretical predictions in Section V.

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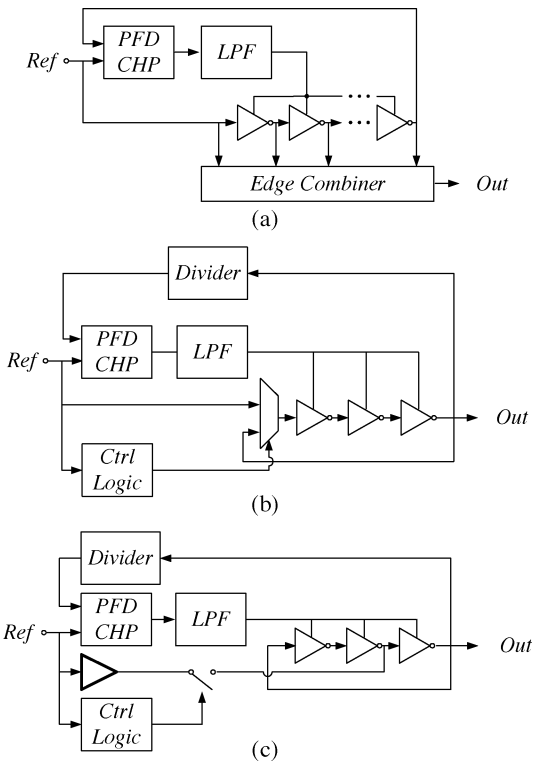

Fig. 1. Frequency synthesizers with phase realignment capability. (a) VCDL-based DLL. (b) Recirculating DLL. (c) Phase realigned PLL.

II. Application of the RPLL Theory to Recirculating DLLs

A. Brief Review of the RPLL Theory

The RPLL theory presented in [3] characterizes the phase noise performance of both DLLs and RPLLs. It is applied to the analysis of recirculating DLLs in this section. For completeness, the highlights of this model are first briefly reviewed.

The theory is based on the physical observations that the phase of the VCO is shifted almost instantaneously when the phase realignment occurs and that the phase shift is nearly linear with respect to the instantaneous phase difference between the VCO and the reference. The ratio between the phase shift and the phase difference just before realignment is defined as β and referred to as the *realigning factor*. The value of β ranges from 0 to 1 and is a measure of how completely the phase error is suppressed.

Fig. 2 shows the resulting linearized model derived in [3] for noise analysis of the RPLL, where $K_{\rm chp}$ and $K_{\rm vco}$ are the charge pump and VCO gains, respectively, N is the divider ratio, and $H_{\rm lp}(s)$ is the transfer function of the loop filter. The terms $\theta_{\rm ref}(s), \theta_{\rm chp}(s), \theta_{\rm div}(s), \theta_{\rm vco}(s)$ and $\theta_{\rm out}(s)$ represent the reference noise, charge pump noise, divider noise, VCO phase noise, and the final output phase noise, respectively. The effect of the phase realignment is represented by the two transfer functions $H_{\rm up}(s)$ and $H_{\rm rl}(s)$, shown as gray blocks in the figure, where

$$H_{\rm rl}(j\omega) = 1 - \frac{\beta}{1+(\beta-1)e^{-j\omega T_r}} e^{-\frac{j\omega T_r}{2}} \frac{\sin\left(\frac{\omega T_r}{2}\right)}{\frac{\omega T_r}{2}}$$

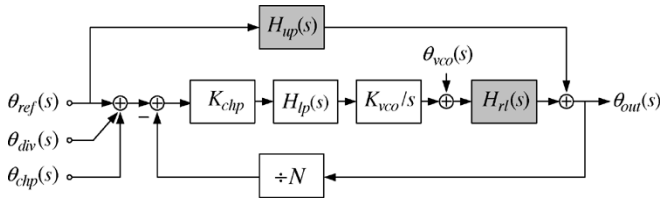

Fig. 2. Linearized model for the RPLL and DLL.

in which T_r is the reference clock period, and

$$H_{\rm up}(j\omega) = \frac{N\beta}{1+(\beta-1)e^{-j\omega T_r}} e^{-\frac{j\omega T_r}{2}} \frac{\sin\left(\frac{\omega T_r}{2}\right)}{\frac{\omega T_r}{2}}.$$

When there is no phase realignment, i.e., when $\beta = 0$, the model reduces to the well-known linearized model for a conventional PLL [8]. The attenuation of the VCO phase noise as well as the charge pump and divider noise increases as β increases. Meanwhile, the reference noise attenuation is reduced as β increases. Therefore, a large β is desirable when a noisy VCO is used along with a clean reference.

B. Application of the RPLL Theory to Recirculating DLLs

Although commonly used to analyze the noise performance of PLLs, few frequency domain noise analysis techniques have been published for DLLs. Most of the published frequency domain analyses of DLLs focus on the stability and settling of the loop, as in [9] and [10]. Noise analyses of conventional DLLs are usually done in the time domain, as in [11] and [12], because DLLs have been most commonly used in digital applications where jitter performance is of interest. In such cases, the metric of interest is usually the standard deviation of the jitter sequence, so it does not provide spectral information. Moreover, correlated noise is usually neglected in the time domain analyses for simplicity so the effect of the $1/f$ noise is usually neglected. Recent findings on jitter transfer characteristics mainly focus on the jitter peaking from the reference to the DLL output so the interaction between the VCO noise and the DLL loop dynamic is not considered [13].

Although the jitter standard deviation is a popular figure of merit, its lack of information regarding the frequency dependence of the circuit noise makes it difficult to separate the contribution to the jitter from individual noise sources in the circuit. Moreover, it is not an appropriate figure of merit for applications such as communication systems whose sensitivity to phase noise tends to be frequency dependent.

To circumvent these problems and provide a tool with which to optimize loop parameters in recirculating DLLs, the RPLL theory outlined above is used to obtain the various transfer functions applied to the different noise sources within the DLL. As demonstrated below, the results indicate that when the VCO noise is dominant and a clean reference source is used, a second-order filter offers no benefit over a first-order filter, and increasing the loop bandwidth improves the attenuation of in-band VCO phase noise. Moreover, while the choice of loop bandwidth significantly affects the attenuation of the VCO phase noise and input noise, i.e., the charge pump and divider noise, it has little effect on the attenuation of the reference

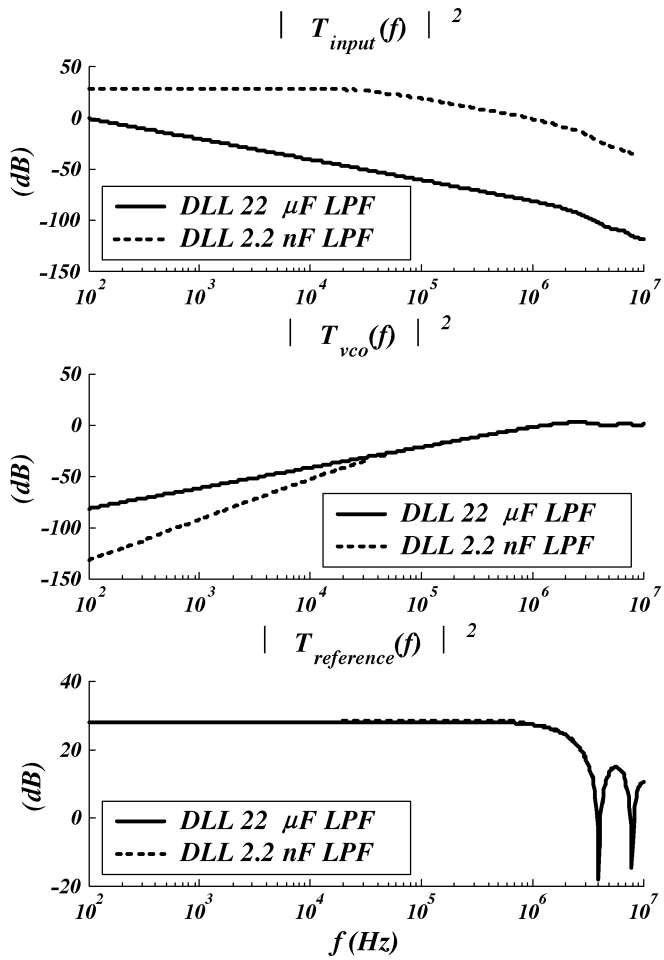

Fig. 3. Calculated noise transfer functions of the recirculating DLL with a first-order loop filter using the linearized model. The bandwidth is controlled by the loop filter capacitor.

noise. Thus, although a small bandwidth may lead to less jitter based on the conventional time domain analysis [12], it does not necessarily lead to low in-band phase noise, especially when the noise is dominated by the VCO. For illustration purposes, Fig. 3 shows the calculated noise transfer functions in a recirculating DLL with a first-order loop filter where the bandwidth is controlled by the loop filter capacitor. The effect of a wide and narrow bandwidth is compared. These general observations are quantified below for the recirculating DLL prototype.

III. Switched Biasing for Flicker Noise Reduction

In modern submicron CMOS processes, $1/f$ noise is a significant noise source and is a critical issue in VCO design. It has been reported that periodically switching a MOS transistor between "on" and "off" states results in a significant reduction of the $1/f$ noise. This phenomenon, although on a microscopic scale, is analogous to VCO phase noise attenuation through phase realignment.

The concentration of noise power at low frequencies indicates there is long-term correlation in the $1/f$ noise. The VCO close-in phase noise is similar in that the long-term correlation is caused by the phase integrating nature of the VCO. A widely

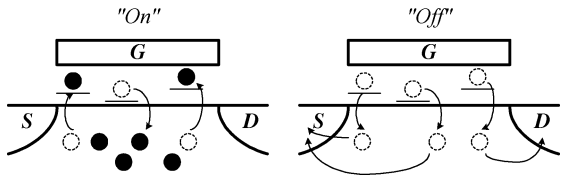

Fig. 4. Periodically switching a MOSFET between "on" and "off" resets the memory of the noise such that the long-term correlation in the noise is suppressed.

accepted theory for the source of $1/f$ noise in MOSFET transistors is the trapping and releasing of carriers in the gate oxide. The distribution of the time constant in the trapping–releasing process is such that the noise power spectral density (PSD) is proportional to $1/f$. As shown in [4]–[6] and later explained theoretically by [14], interference with the noise correlation by periodically switching the MOSFET transistor between "on" and "off" states results in a reduction in $1/f$ noise. As illustrated in Fig. 4, when the transistor is turned off, the trapped carriers tend to be released, resulting in the reset of the noise source. This phenomenon is analogous to the phase realignment where the phase error is reset so that the memory to the past noise is removed.

As reported in [4]–[6], the $1/f$ noise attenuation strongly depends on the way in which the transistor is turned off. Using an nMOS transistor as example, decreasing the gate–source voltage in the off state leads to greater noise attenuation. As explained in [6], when the decrease of the gate–source voltage results in a significant change in the Fermi level at the surface, thereby changing the occupation of the trapped carriers, a significant reduction of $1/f$ noise is observed. In analogy to the effect of β, the change of the Fermi level affects how completely the trapped carriers are released. A greater change in the Fermi level is analogous to a greater β, which leads to more complete erasure of the noise memory and, therefore, greater attenuation of the $1/f$ noise.

IV. Implementation Details

A. DLL and VCO Topology

Fig. 5 shows the simplified block diagram of the proposed recirculating DLL. The VCO contains two NAND gates and several voltage-controlled delay cells to form the ring [15]. When the signals "rlgn" and "pulse_sw" are set high, the NAND gates act as inverters and the VCO behaves as a conventional ring VCO. Phase realignment is performed in two steps. First, by setting "rlgn" and "pulse_sw" low, the noisy VCO edge is blocked and the "ring" is temporarily opened. Then, when the clean reference edge arrives, it causes both "rlgn" and "pulse_sw" to go high so as to start a new cycle of oscillation free of phase noise memory. Specifically, "pulse_sw" is a slightly delayed version of "rlgn" to avoid any potential glitches. A simplified timing diagram is shown in Fig. 6. The implementation is functionally equivalent to that presented in [2], so the VCO must be set to its maximum frequency during start-up as reported in [2].

When the clean reference clock edge is switched in to replace the noisy VCO clock edge, it is desirable to match the shape of the waveform of the reference and VCO clock to minimize the disturbance to the VCO core. However, in a typical NAND gate

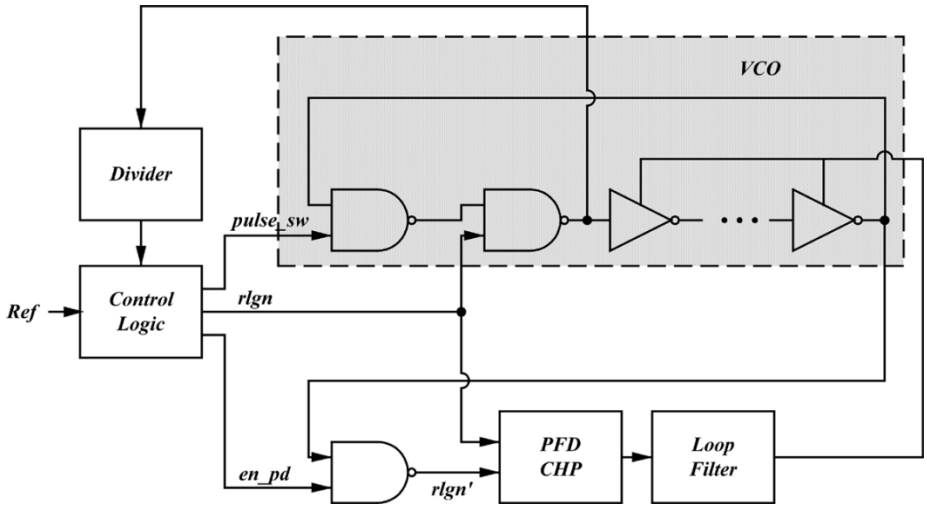

Fig. 5. Proposed recirculating DLL block diagram.

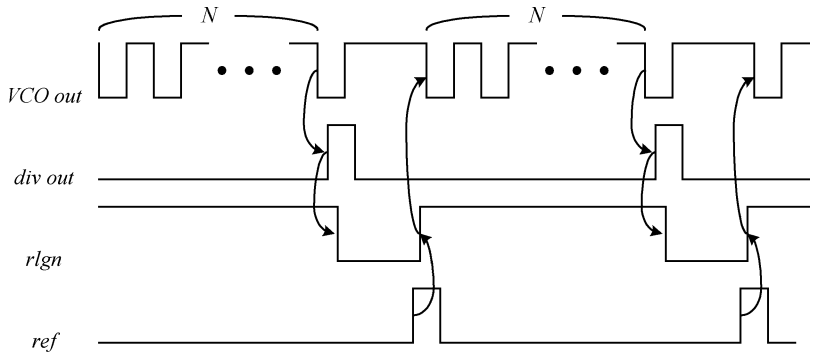

Fig. 6. Simplified timing diagram of the phase realignment control in the prototype.

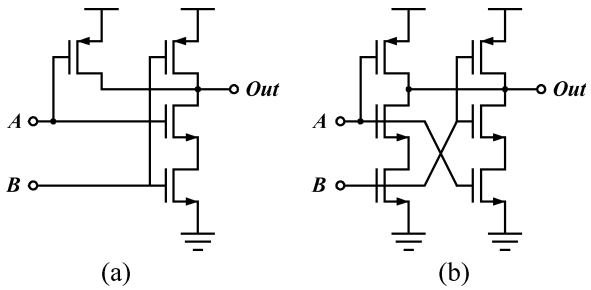

Fig. 7. (a) Conventional NAND gate. (b) Proposed NAND gate for better waveform matching.

as shown in Fig. 7(a), when one input switches from "0" to "1" while the other stays at "0," the falling edge of the output waveform is mismatched because of the body effect in the nMOS transistor even if the rising edges of the two inputs are identical. To alleviate this problem, the NAND gate in Fig. 7(b) is used. With the addition of two more nMOS transistors and cross-coupling of the gates, both the pull-down and pull-up paths of the output are matched with respect to the two inputs to ensure good symmetry of the output waveform.

The signals into the two NAND gates are single-ended to ensure good waveform matching during the phase realignment. However, the waveforms in the VCO delay cells are pseudo-differential for better rejection of common mode noise. Thus, although not shown in the figure, a single-ended to differential converter and differential to single-ended converter are implemented at the beginning and end of the voltage-controlled delay chain, respectively.

B. Switched Biasing in the VCO Delay Cell and Bias Circuitry

To minimize the $1/f$ noise, switched biasing is used in both the voltage-controlled delay cell and its biasing circuitry. Because the loop filter is single-ended, the bias circuitry must generate the control voltages for both the pMOS and nMOS transistors in the delay cell to ensure symmetry of the waveform, which is critical for $1/f$ noise reduction [16]. Fig. 8(a) shows a simple implementation of the bias circuitry. Despite its simplicity, the $1/f$ noise generated from the bias can significantly degrade the VCO phase noise as shown in [17]. Conventional approaches for $1/f$ noise reduction are to increase the size of the device or to filter the control voltage. Neither approach is area-efficient. In addition, filtering could potentially compromise the loop dynamics. Switched biasing, on the other hand, offers an area efficient solution for $1/f$ noise suppression. A straightforward approach is shown in Fig. 8(b). It consists of two identical bias branches that are used alternately with only one on at any time. As shown in Fig. 8(c), the branch not in use is switched off by setting the gate-source voltage to zero. As a result, this approach has almost the same power consumption as that shown in Fig. 8(a) except for the slight overhead in the switching circuitry. While the approach has the desired effect of

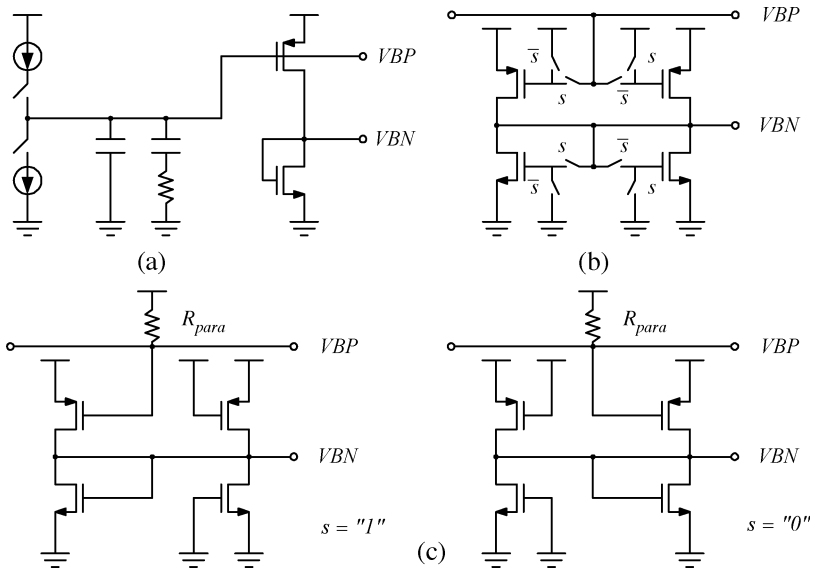

Fig. 8. (a) Typical complementary bias generation. (b) A straightforward approach to implement switched biasing for $1/f$ noise reduction. (c) Illustration of the detailed operation of the bias: an equivalent parasitic resistor is introduced between the loop filter and the power supply.

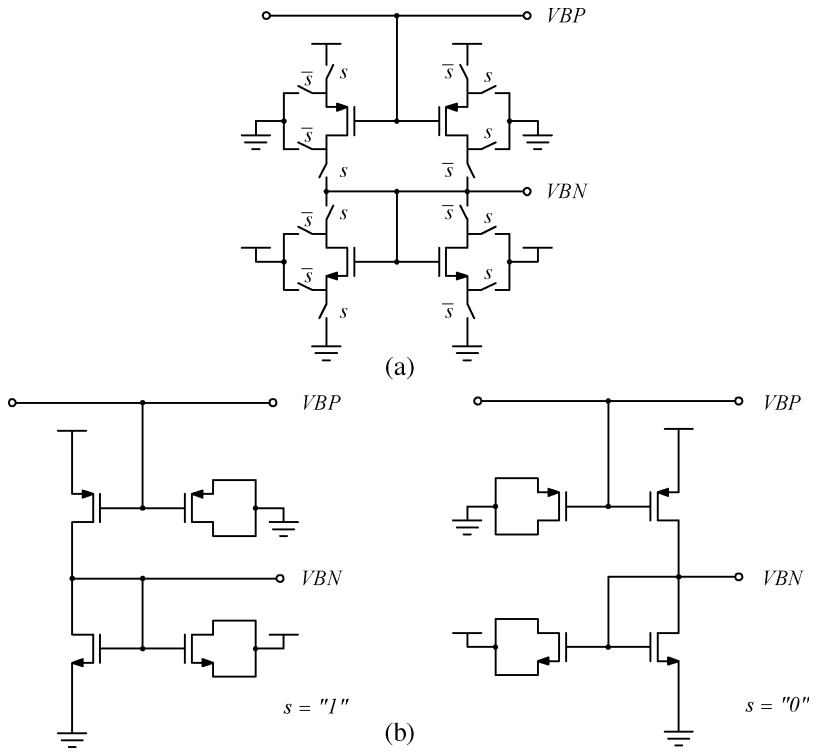

Fig. 9. Proposed bias generation with improved $1/f$ noise reduction. (a) Simplified schematic of the bias circuit. (b) Detailed illustration of the bias circuit's operation.

suppressing $1/f$ noise, the switching introduces the equivalent of a parasitic resistor between the loop filter node and the power supply, which can adversely affect the loop dynamics.

To alleviate this problem, the bias circuit shown in Fig. 9(a) is used in the recirculating DLL prototype. This circuit switches the source and drain to turn off each transistor as illustrated in Fig. 9(b). For example, when an nMOS transistor is turned off, its source and drain are both switched to V_{DD}. Thus, the gate–source voltage is negative in the "off" state. The clock for the switched biasing is provided by a buffered version of the VCO output. For illustration purposes, Fig. 10 shows the simulated gate, drain, and source voltages of the nMOS transistors when the switched biasing is enabled. In practice, mismatches between the two biasing branches are inevitable. However, since the biasing branches are switched at the VCO frequency, the mismatches only introduce a slight error in the duty cycle of the VCO, which is not typically a concern in practice.

The performance of the voltage-controlled delay cells in the VCO is critical. Their phase noise and value of β strongly depend on their circuit topology. As described in [3], to maximize

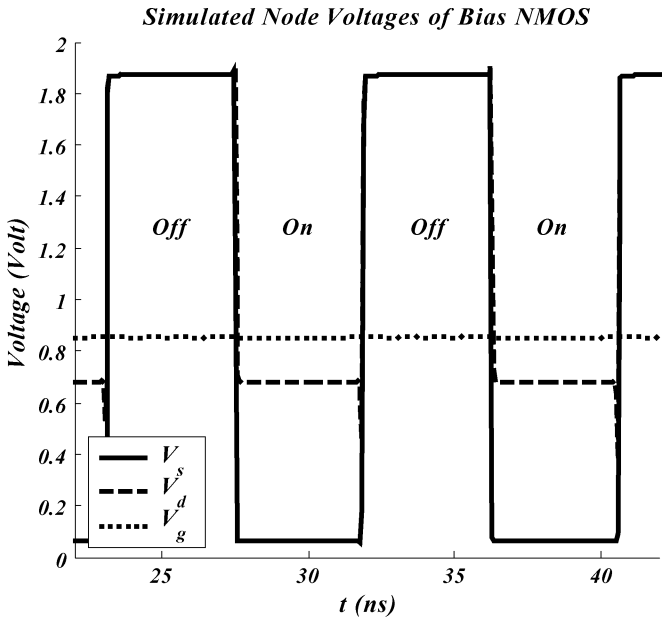

Fig. 10. Simulated node voltages of the nMOS transistor in the bias circuitry when switched biasing is enabled.

β it is necessary to minimize the coupling among delay cells and ensure that each cell is truly edge-triggered. The proposed delay cell is an extension of that shown in Fig. 11(a), wherein the delay is varied by controlling the transconductance of M_p, M_n, $M_p{}'$, and $M_n{}'$. This topology minimizes the inter-cell coupling because, except for the delay control lines, the delay cells are only connected through low impedance power supply lines. Transistor level simulations confirm that the resulting VCO achieves a β of very nearly 1, the theoretical maximum, across process corners. The topology also allows rail-to-rail signal swing and a wide tuning range (1–160 MHz) to cover the large component spread in typical CMOS processes. As the maximum power supply voltages of CMOS processes continue to scale down with feature size, the rail-to-rail swing is particularly desirable because it enables more efficient use of the power supply to increase the signal-to-noise ratios inside the VCO.

The pseudo-differential topology is used to reject common-mode noise from the supply and substrate. Normally, the differential signal is created using a latch with two back-to-back inverters at the outputs as shown in Fig. 11(a). Transistor-level simulations indicate that M_p, M_n, $M_p{}'$, and $M_n{}'$ are the dominating $1/f$ noise contributors in the delay cell. Unfortunately, the transistor size can not be increased arbitrarily to reduce the $1/f$ noise without severely reducing the speed of the VCO. Therefore, it is desirable to use switched biasing here as a compact solution. In a normal oscillation cycle, every transistor is turned on and off. However, if the conventional latch is used, when M_p, M_n, $M_p{}'$, and $M_n{}'$ are off, unlike the other transistors their gate–source voltages are not set to zero. In order to further exploit the switched biasing technique to suppress $1/f$ noise in these transistors, a special latch is implemented, as shown in Fig. 11(b). The operation of M_n is explained here for illustration purpose. When it is turned off using the proposed latch, both its source and drain are pulled to V_{DD} to turn it off as hard as possible. Fig. 12(a) shows the simulated outputs of

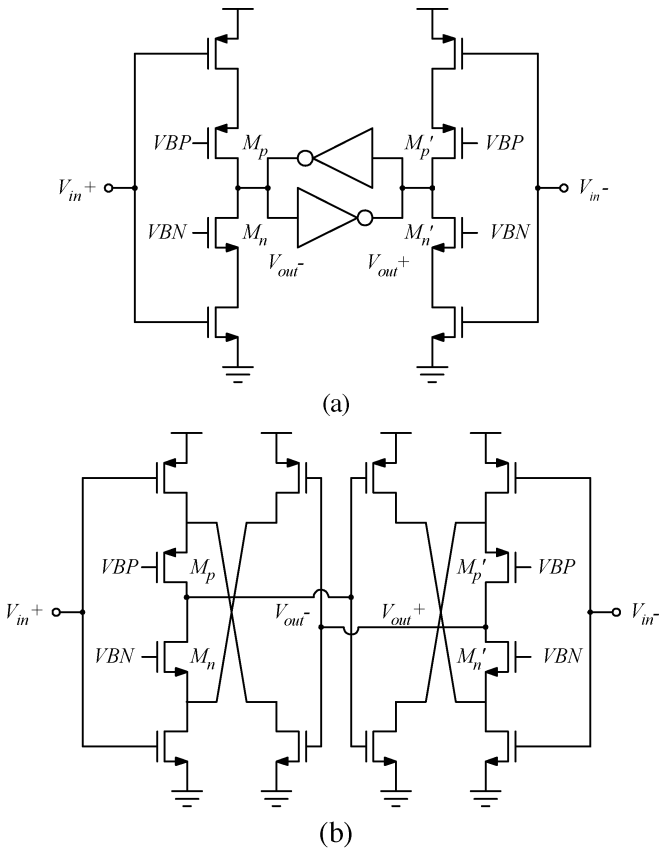

Fig. 11. Pseudodifferential voltage-controlled delay cell design. (a) Conventional latch using two back-to-back inverters. (b) Improved latch for better $1/f$ noise reduction.

the delay cell where the transistors are sized to make the rising and falling edges as symmetric as possible for better $1/f$ noise rejection [16]. Fig. 12(b) shows the node voltages of M_n where the "off" state is identical to the "off" state of the transistor in the bias described above.

V. Measurement Details

A. VCO Phase Noise Measurement

The prototype IC was fabricated in a single-poly, six-metal, 0.18-μm TSMC CMOS process and was packaged in a 32-pin QFN package. The 4-MHz reference clock for the DLL is derived from a 32-MHz crystal. Figs. 13–16 present measured results with superimposed theoretical results. The theoretical PSD curves were obtained by applying the calculated transfer functions from the linearized model to the measured phase noise PSD of the open-loop VCO. The open-loop VCO phase noise PSD was obtained by measuring the phase noise PSD of the system with and without switched biasing and with a very narrow bandwidth so that the phase noise was dominated by the VCO. The phase noise was measured by an HP 4352 VCO/PLL analyzer.

Fig. 13 shows superimposed measured and theoretically calculated phase noise PSD curves for the synthesizer configured as conventional PLL and as a recirculating DLL with a second-order loop filter, both with and without switched biasing. The system parameters are shown in the figure caption.

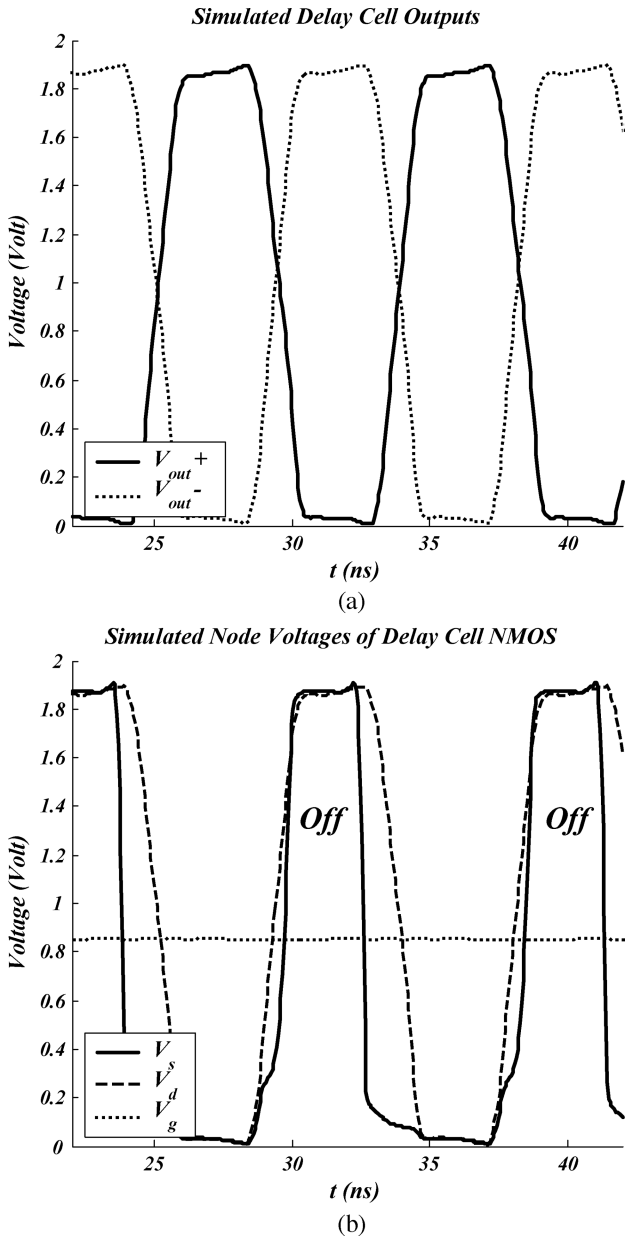

Fig. 12. Simulated waveforms in the delay cell. (a) Delay cell outputs. (b) Node voltages of M_n when the switched biasing is enabled.

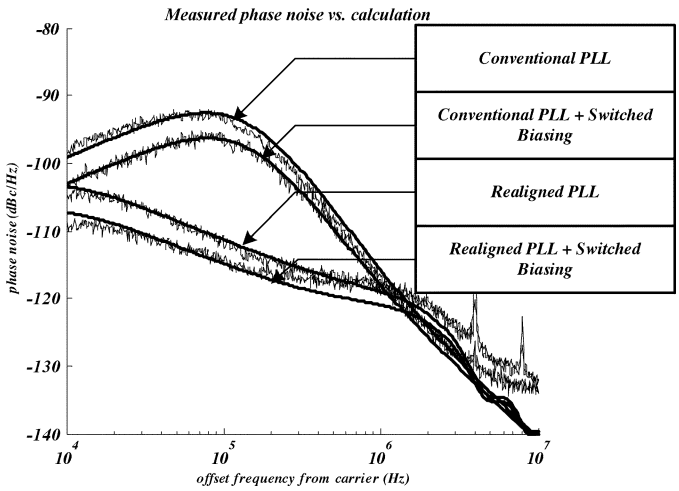

Fig. 13. Comparison between conventional PLL and the recirculating DLL with a second-order loop filter, with and without switched biasing. Theoretical calculations are superimposed on the measured data. System parameters: $f_{\rm ref} = 4$ MHz, $N = 25$, $K_{\rm vco} = 190$ MHz/V, $I_{\rm chp} = 0.5$ mA, loop filter: $R = 330\ \Omega$, $C_1 = 680$ pF, $C_2 = 8.2$ nF, PLL bandwidth $= 200$ kHz.

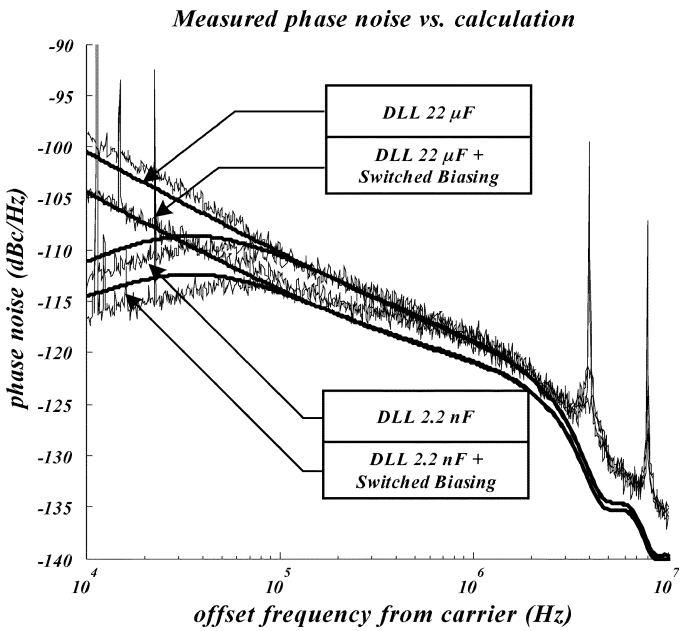

Fig. 14. Recirculating DLL phase noise PSDs: wide loop bandwidth results in more in-band noise attenuation. Theoretical calculations are superimposed on the measured data.

The results indicate that phase realignment significantly attenuates the in-band VCO phase noise. With the switched biasing enabled, a peak spot phase noise reduction of 5 dB is observed in both the PLL and the recirculating DLL. Since the transistors in the delay cell are switched off the same fashion as in the bias, it is reasonable to expect similar noise attenuation is achieved inside the delay cell. This result confirms that the switched biasing technique is feasible up to at least 100 MHz. With both noise reduction schemes enabled, a peak spot phase noise reduction of 21.5 dB is observed compared to the conventional PLL.

Fig. 14 shows the measured phase noise when the synthesizer is configured as a recirculating DLL with a first-order loop filter. The results support the theoretical predictions made above that a wide-band first-order loop filter yields the best results.

The phase noise performance of a VCDL-based DLL as shown in Fig. 1(a) is reported in [18] where no significant $1/f$ noise is detected in the output. Although it is predicted in [18] that the $1/f$ noise in the DLL output is reduced because the $1/f$ noise in the circuit is modulated to $f_{\rm ref}$, no detailed analysis is available to support this claim. Since the prototype recirculating DLL achieves a β value of nearly 1, the suppression of phase noise memory in the recirculating DLL is essentially as good as a VCDL-based DLL. Therefore, in a recirculating DLL, in addition to the phase noise suppression from the phase realignment, one would expect much less $1/f$ noise from the VCO even without the switched biasing. However, this phenomenon

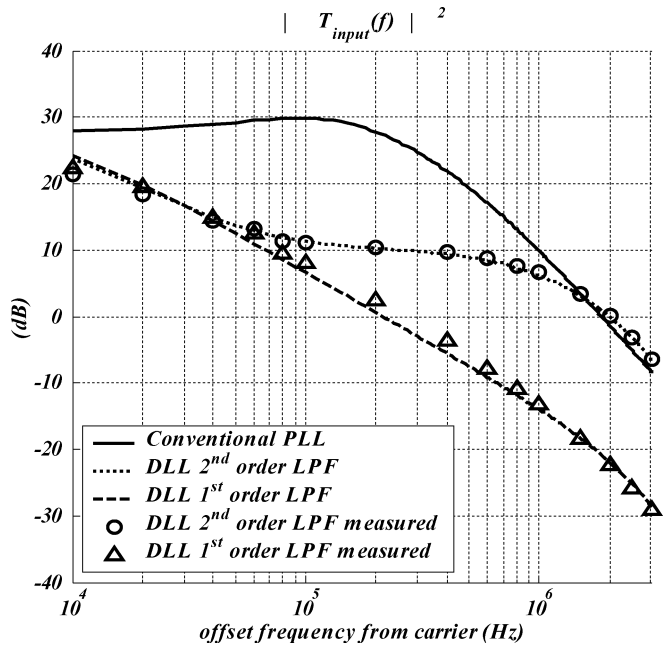

Fig. 15. Measured input noise transfer function for recirculating DLL with second-order loop filter and with first-order loop filter, the conventional PLL input noise transfer function is used as the reference theoretical predictions are shown as continuous curves while the discrete measured data points are represented by triangles and circles.

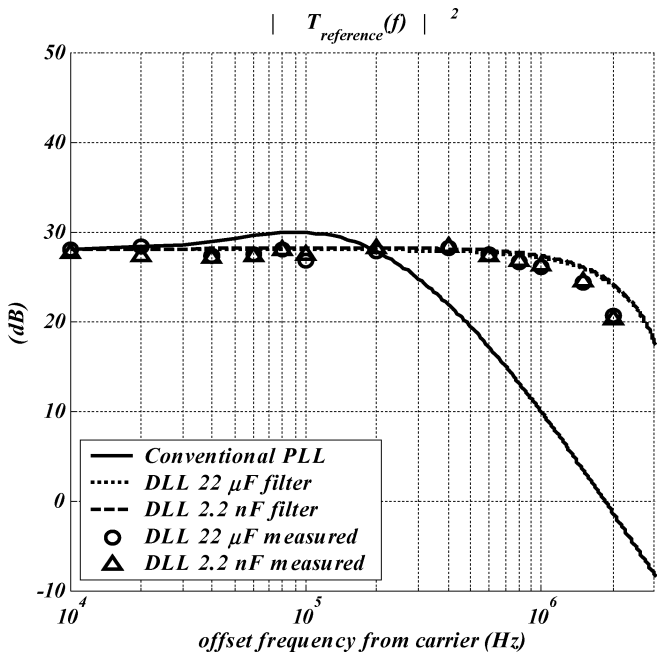

Fig. 16. Measured reference noise transfer function for DLL with 22 μF loop filter and DLL with 2.2-nF loop filter: the loop bandwidth has little effect on the reference noise. The conventional PLL reference noise transfer function is used as the reference. Theoretical predictions are shown as continuous curves while the discrete measured data points are represented by triangles and circles.

was not observed in the recirculating DLL prototype measurement results. Taking the top curve of Fig. 14 as an example, the theoretical calculation was using the standalone VCO phase noise measured separately with the switched biasing disabled. The good agreement between theory and measurement indicates the $1/f$ noise inside the VCO is not attenuated by the phase realignment. This is because the phase realignment does not affect the mechanism by which the $1/f$ noise is generated. Therefore, in order to reduce the contribution of the $1/f$ noise to the in-band phase noise, both system-level optimization such as the choice of a recirculating DLL for phase realignment, a wide loop bandwidth, and device-level innovation such as switched biasing, are required.

B. Reference and Input Noise Transfer Function Measurement

Because the in-band phase noise was dominated by the VCO, it was difficult to measure the input and reference noise transfer functions from the measured phase noise. In order to characterize the two transfer functions, a sinusoid, generated by an Agilent 8648C signal generator, was ac coupled into the loop filter and the reference clock pin, respectively. This injected signal, which is shaped by the noise transfer functions, is upconverted to the synthesizer output and results in spurious tones around the VCO center frequency. The power of the spurs was measured using an Agilent E4405B spectrum analyzer. Sweeping the frequency of the injected signal provided a sampled version of the noise transfer function.

Due to the parasitic capacitance and inductance from the PCB board, it was difficult to measure the absolute value of the transfer functions. Alternatively, since the input noise transfer function of a conventional PLL is well known, it was used as a reference, and the measured results for the recirculating DLL with second- and first-order loop filters were normalized with respect to the conventional PLL noise transfer function. Fig. 15 shows the input phase noise transfer functions of the conventional PLL, and recirculating DLL with second- and first-order loop filters. As shown in the figure, theoretical predictions are shown as the continuous curves while the measured data points are represented by discrete triangles and circles.For the same total loop filter capacitance, the DLL with a first-order loop filter provides more attenuation to input noise than that with a second-order loop filter. Fig. 16 shows the reference noise transfer function of the conventional PLL, recirculating DLL with 22-μF loop filter and DLL with 2.2-nF loop filter. As predicted by the theory, the loop filter bandwidth does not significantly affect the in-band attenuation of reference noise.

TABLE I
PERFORMANCE SUMMARY

Technology	*1.8V, 0.18 μm CMOS (1 poly, 6 metal)*
Chip Size	*2.2mm × 2.2 mm*
Package	*32 Pin QFN*
Reference Frequency	*4MHz (derived from a 32 MHz crystal)*
VCO Frequency	*100MHz*
Tuning Range	*1MHz ~ 160MHz*
Power Consumption	*8.6mW (core)*

The measured performance of the prototype IC is summarized in Table I. There is no observable difference in power consumption between the PLL mode and DLL mode. A die photograph of the fabricated circuit indicating the major functional blocks is shown in Fig. 17.

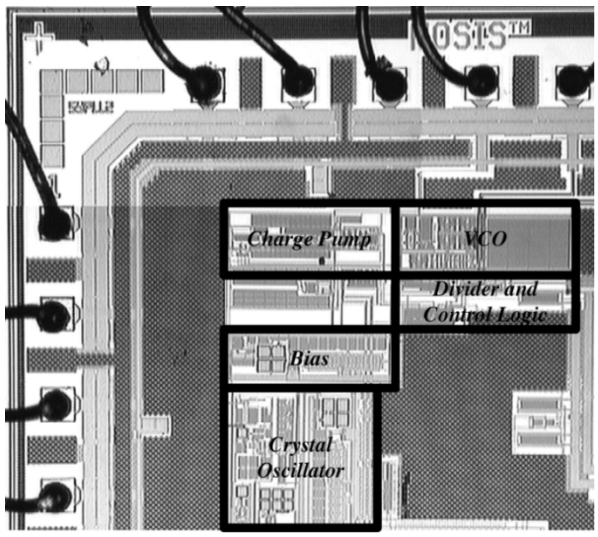

Fig. 17. Die photo.

VI. Conclusion

This paper presents a recirculating delay-locked loop (DLL) with various innovations to improve in-band phase noise suppression. The VCO and bias circuitry incorporate circuit-level techniques that reduce $1/f$ noise through switched biasing. The phase realignment theory is applied to optimize the VCO so as to maximize the phase noise suppression, which is achieved by periodically switching in a clean reference pulse to reset the VCO phase noise memory. It is further applied to optimize the loop filter and deduce several loop parameter design guidelines for recirculating DLLs. Measurements of the fabricated prototype agree well with theoretical predications.

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