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A Highly-Digital Frequency Synthesizer Using Ring Oscillator Frequency-to-Digital Conversion and Noise Cancellation

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Text

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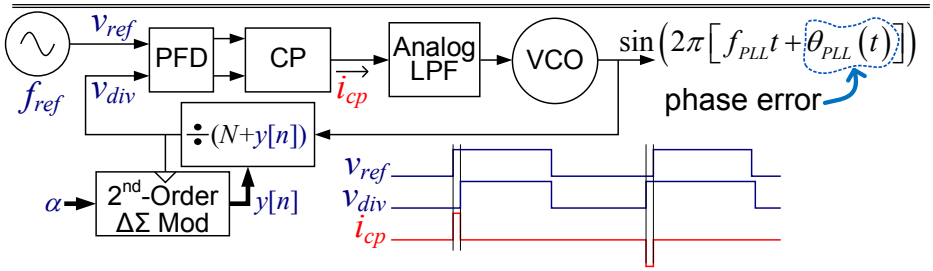
Outline

- Fractional-*N* PLL background information
- Build-up of the proposed PLL architecture
- Circuit details
- Measured results

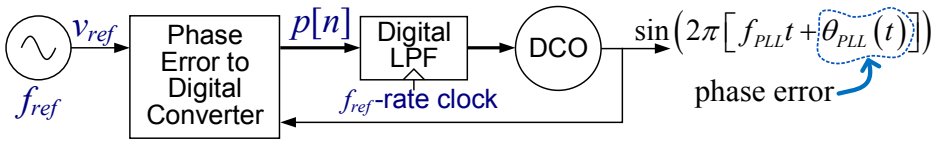
Conventional Analog Fractional-*N* PLL



- $f_{PLL}=(N+\alpha)f_{ref}$ where N = integer and $-½ \le \alpha \le ½$
- Charge in n^{th} ref period's CP pulse $= -\theta_{PLL}[n] + \varepsilon_q[n]$
  $\theta_{PLL}[n]$ = sampled phase error
  $\varepsilon_q[n]$ = integrated 2nd-order ΔΣ quant noise
- Lowest noise and spurs to date ☺
- Analog LPF is big & CP is sensitive to nonlinearity/leakage ☹

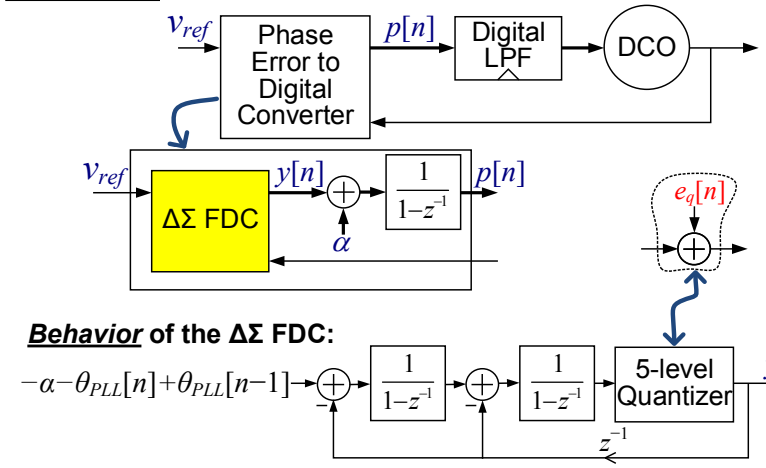
  ⇒ Not compatible with highly-scaled CMOS technology

"Digital" Fractional-*N* PLLs Avoid These Problems



- $p[n] \cong -\theta_{PLL}[n] + \varepsilon_q[n]$ (reference-rate digital sequence)
- In prior digital PLLs:
  - $\varepsilon_q[n]$ = coarse uniform or 1st-order ΔΣ quantization error so it usually contains large spurs
  - Dither sometimes used to reduce spurs but increases noise
- This work is a new digital PLL in which:
  - $\varepsilon_q[n]$ = integrated 2nd-order ΔΣ quantization error just like in an analog PLL
  - 2nd-order ΔΣ self-dithering property ⇒ low spurs & noise

2nd-Order FDC-Based Phase Error to Dig. Converter

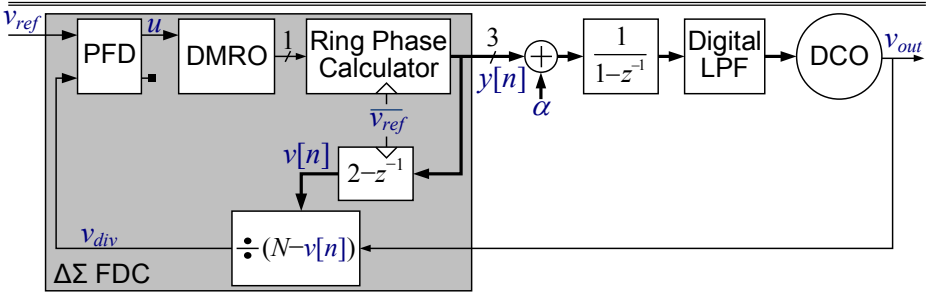


$\Rightarrow y[n]+\alpha = -\theta_{PLL}[n]+ \theta_{PLL}[n-1] +$ (2nd-order ΔΣ quantization error)

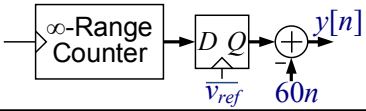
$\Rightarrow p[n] = -\theta_{PLL}[n] + e_q[n] - e_q[n-1]$

$\therefore$ 2nd-ord ΔΣ $\Rightarrow p[n]$ has 1st-order shaped noise but low spurs

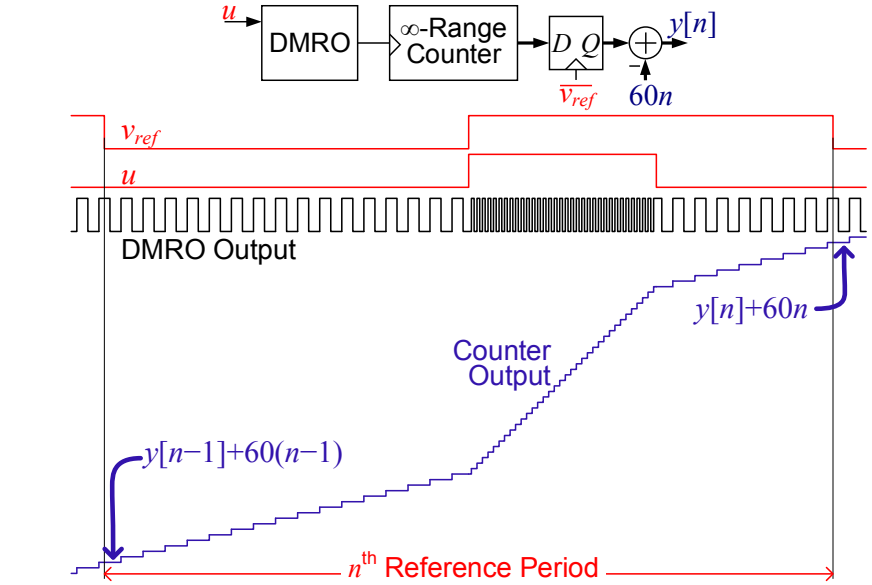
Simplified Version of New PLL Architecture



- Dual-mode ring oscillator (DMRO):
  - $f_{DMRO}=f_{high}$ when $u = 1$ and $f_{DMRO}=f_{low}$ when $u = 0$
  - Configured such that $f_{high}-f_{low}\cong f_{PLL}$
  - Can be gated ($f_{low}=0$) or switched ($f_{low}\neq 0$) ring oscillator
- When PLL is locked ring phase calculator is equivalent to:

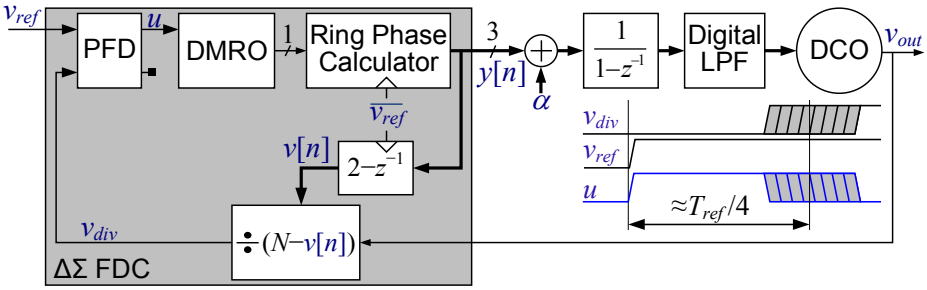


DMRO and Ring Phase Calculator Behavior



$\therefore$ Counter output = quantized integral of DMRO frequency

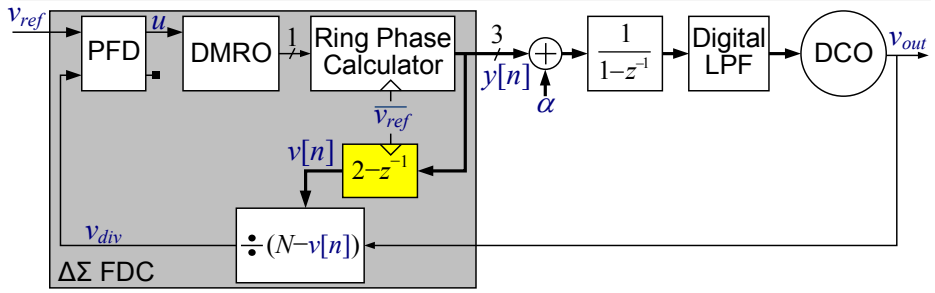
ΔΣ FDC Behavior When PLL is Locked



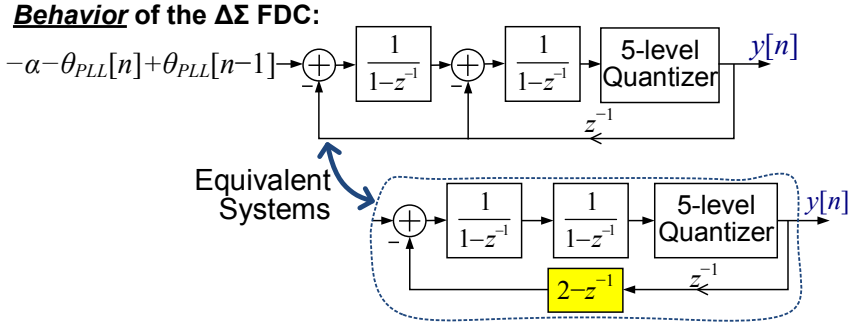
Negative feedback within ΔΣ FDC through divider:

- Larger $y[n]$
  - $\Rightarrow$ larger $v[n]$
    - $\Rightarrow$ earlier v_{div} edge
      - $\Rightarrow$ shorter u pulse
        - $\Rightarrow$ less DMRO phase change
          - $\Rightarrow$ smaller $y[n+1]$
- Causes f_{DMRO} to be $60f_{ref}$ on average and keeps $|y[n]| \leq 2$

What Causes the ΔΣ Modulator Behavior?

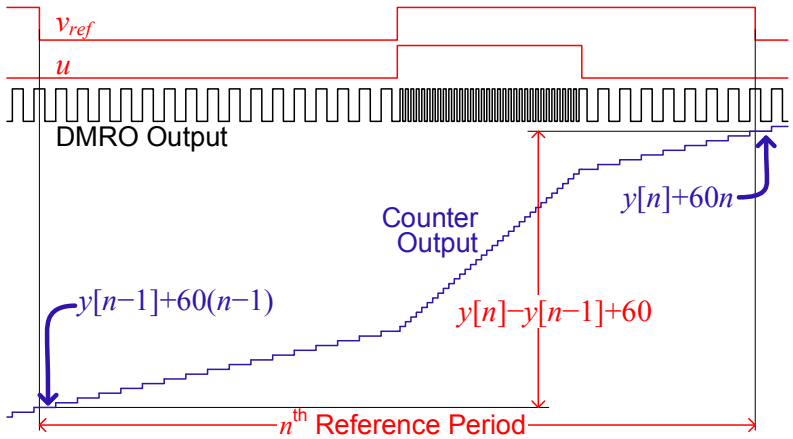


Behavior **of the ΔΣ FDC:**

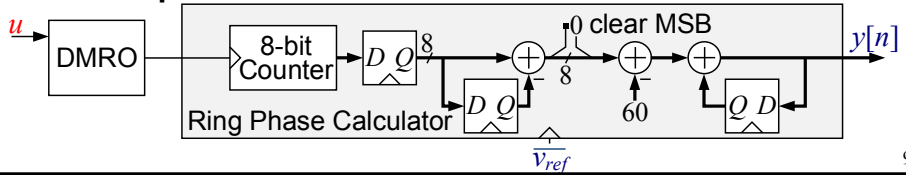


But How to Avoid an ∞-Range Counter?

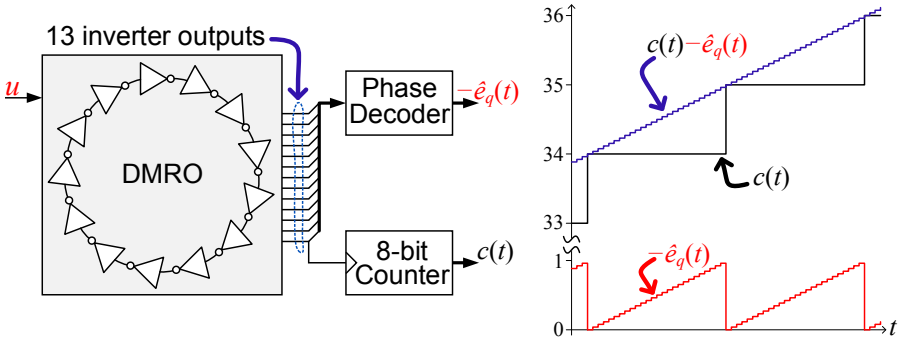
Recall:



Practical implementation:

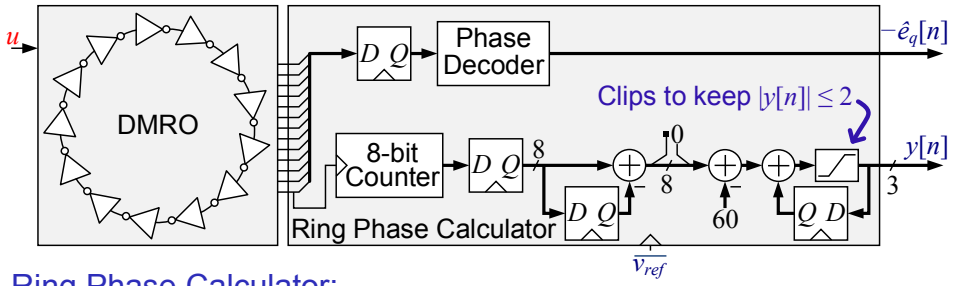


How to Make Use of All The DMRO Outputs?



- DMRO has 13 outputs
- Counter is clocked by just 1 DMRO output
- Counter quantizes DMRO phase ramp by counting integer cycles $\Rightarrow$ very coarse quantization
- Can use all DMRO outputs to measure fractional quantization error in steps of 1/26 of a cycle

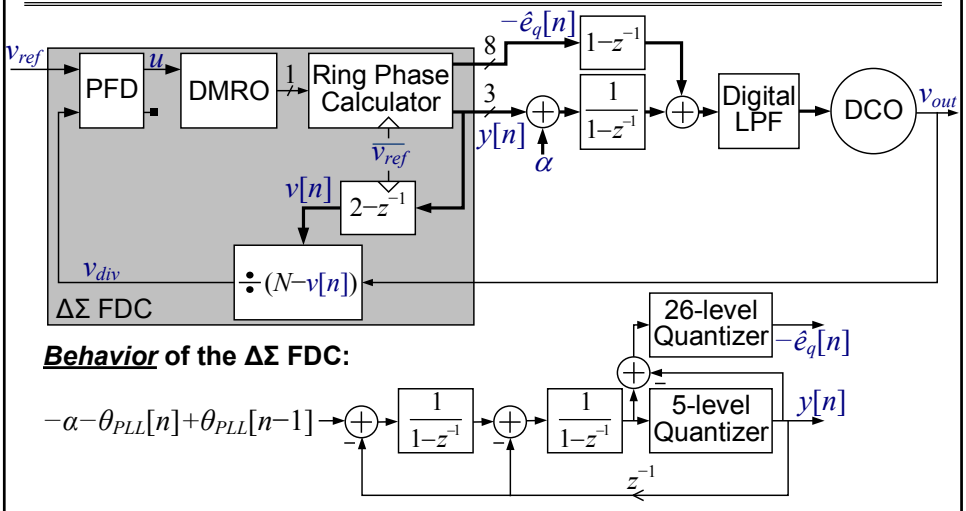
More Ring Phase Calculator Details



Ring Phase Calculator:

- Standard cell logic
- Samples DMRO phase on falling edges of v_{ref}
- Asynchronous sampling issue/solution described shortly
- $y[n]$ is integer-valued, $-\hat{e}_q[n]$ is fractional
- When PLL is locked, clipper has no effect
- Otherwise, clipper avoids roll-overs to reduce locking time

Implemented PLL High-Level Architecture

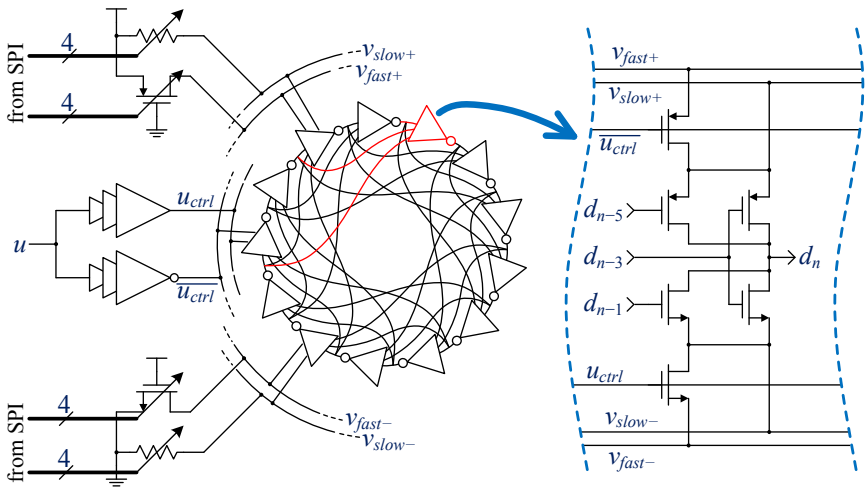


Behavior **of the ΔΣ FDC:**

$-\alpha-\theta_{PLL}[n]+\theta_{PLL}[n-1]$

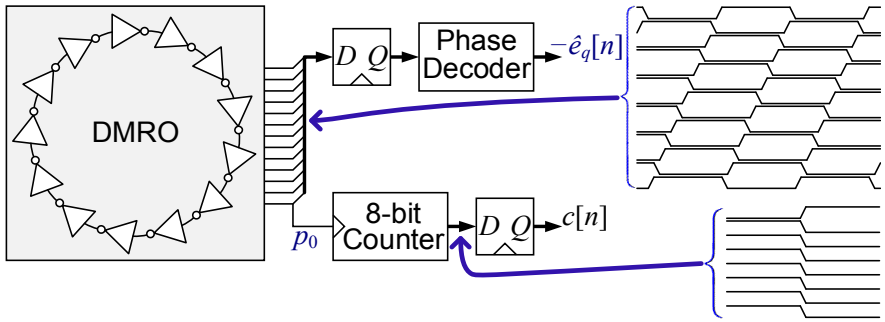
- Quantization noise cancellation (QNC) uses $-\hat{e}_q[n]$ to cancel coarse quantization noise prior to loop filter
- QNC allows wider loop filter bandwidth without noise penalty

DMRO Details



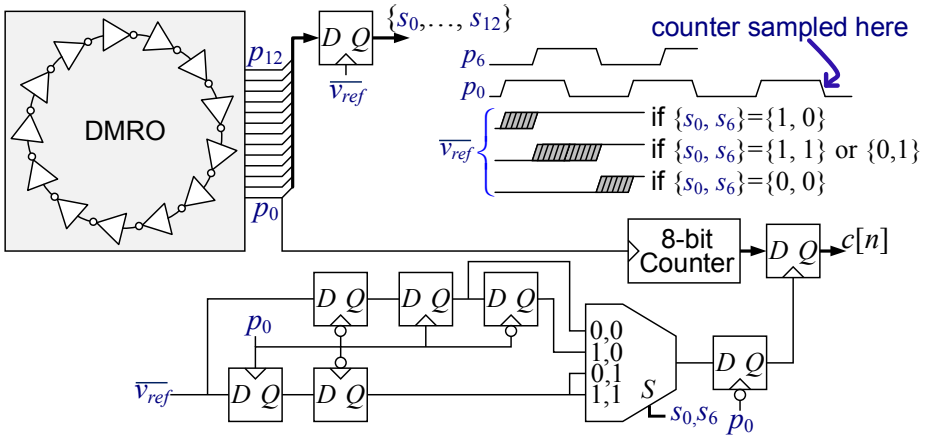
- Multi-path [Lee, Kim, Lee, JSSC 1997] current starved ring
- $f_{high}-f_{low} \cong f_{PLL}$ set with 5% resolution via ring supply resistances
- SPI selectable ranges: $0.4<f_{low}<3.4$ and $1.8<f_{high}<5.1$ GHz

RPC Asynchronous Sampling Issue



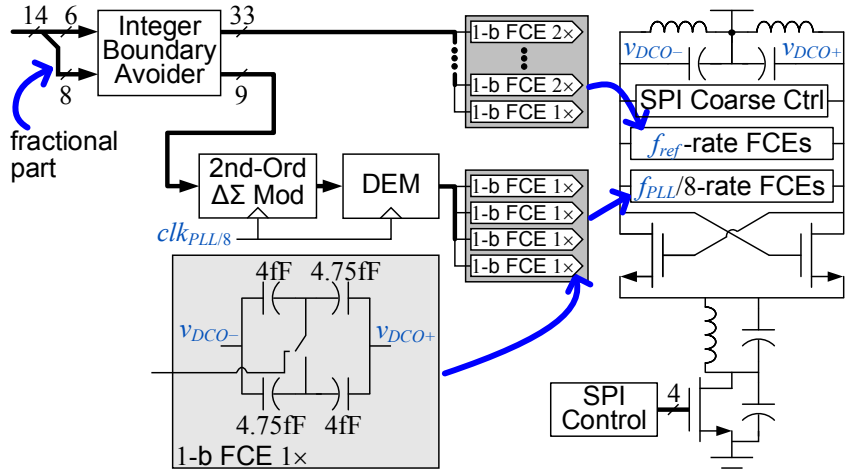
- Only one DMRO output bit changes at a time
  - ⇒ bit transitions occur at 1/26 quantization boundaries
  - ⇒ $-\hat{e}_q[n]$ errors from sampling during bit transitions << 1/26
  - ⇒ Asynchronous sampling of DMRO phases not a problem
- Multiple counter bits can change at once (e.g., 127 to 128)
  - ⇒ $c[n]$ errors from sampling during bit transitions can be huge
  - ⇒ Asynchronous sampling of counter output *is* a problem

RPC Asynchronous Sampling Solution



- $s_0, \ldots, s_{12}$ = DMRO outputs sampled on falling reference edge (phase decoder input bits)
- s_0 and s_6 indicate in which of 3 regions the edge occurred
- Retiming logic samples counter exactly 1.5 DMRO periods after the DMRO period in which the edge occurred

Digitally Controlled Oscillator



- FCEs as in [Venerus, Galton, JSSC 2015]
  ΔΣ modulation as in [Staszewski, et. al., ISSCC 2005]
- Integer Boundary Avoider adds/subtracts 0 or 1 to top/bottom FCE banks as needed to minimize top bank (f_{ref}-rate) toggling

Additional Design Information

DCO

- Unit FCE frequency step: 25 kHz
- PLL feedback-controlled DCO tuning span: 1.8 MHz
- SPI-controlled DCO tuning range: 2.8-3.7 GHz

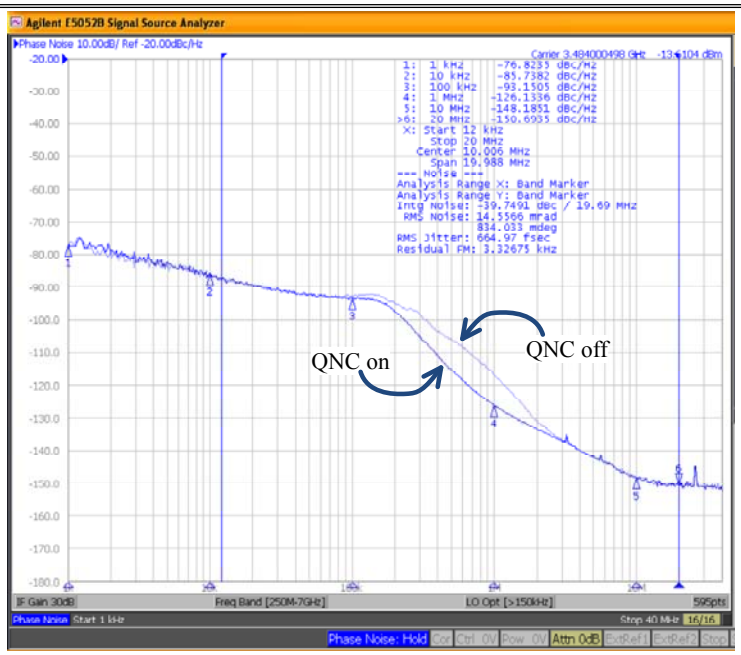
Divider

- 6 ÷2/3 pulse swallowing stages
- $f_{PLL}/8$-rate clock is output of 3rd ÷2/3 pulse swallowing stage

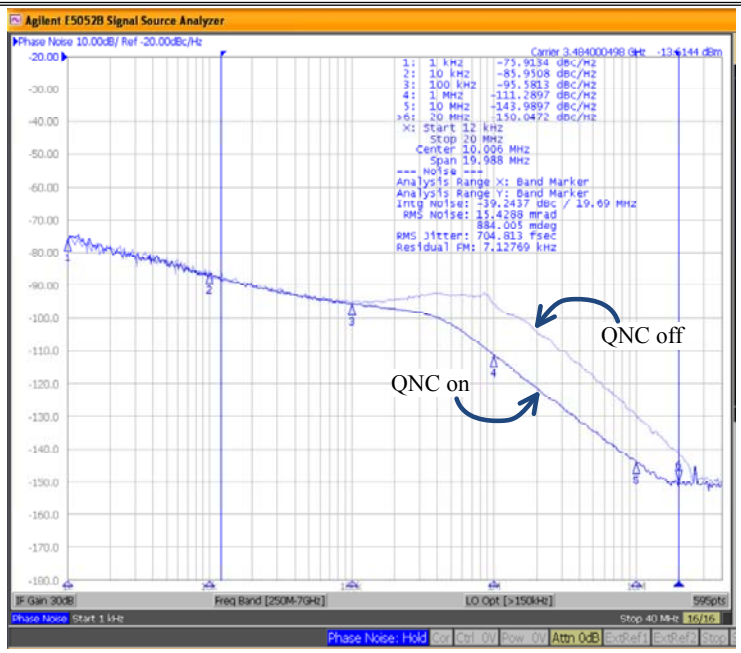
Digital

- All digital logic synthesized except divider and DMRO sampling circuitry
- Synthesized logic clocked by $f_{PLL}/8$-rate clock

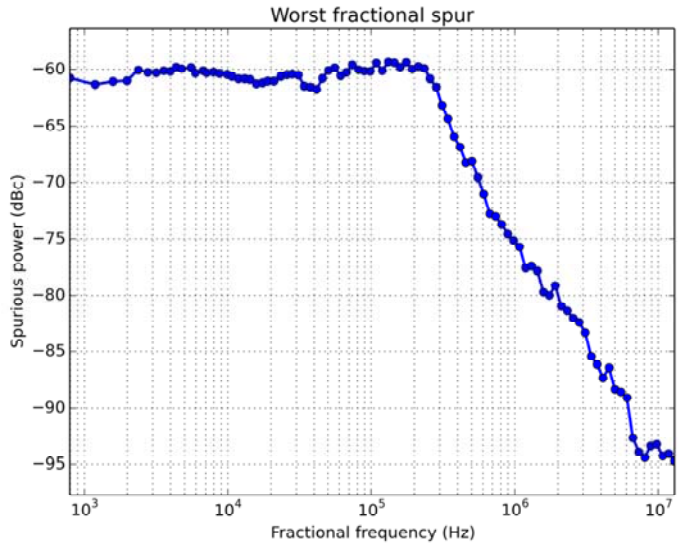
Measured Phase Noise (PLL BW = 140 kHz)



Measured Phase Noise (PLL BW = 260 kHz)

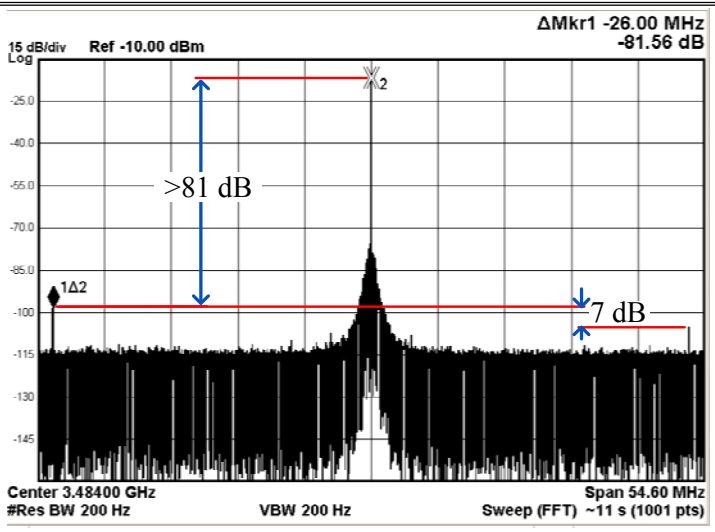


Measured Spurious Tone Performance at 3.5 GHz



Largest measured fractional spurious tone powers for several fractional frequency settings ranging from 800 Hz to 13 MHz

Measured PLL Output Spectrum



- Reference spur from DCO input and coupling <−81 dBc
- Asymmetry ⇒ reference spur from DCO input only <−88 dBc

Performance Summary

Technology (nm)	65
Supply (V)	1.0
Power Diss. (mW)	15.6
Area (mm^2)	0.35
Ref Freq (MHz)	26
PLL Freq (GHz)	3.5
PLL BW (kHz)	140
In-Band PN (dBc/Hz)	−93
PN@1MHz (dBc/Hz)	−126
PN@3MHz (dBc/Hz)	−138
PN@20MHz (dBc/Hz)	−151
Reference Spur (dBc	−81
In-Band Fract. Spur (dBc)	−60

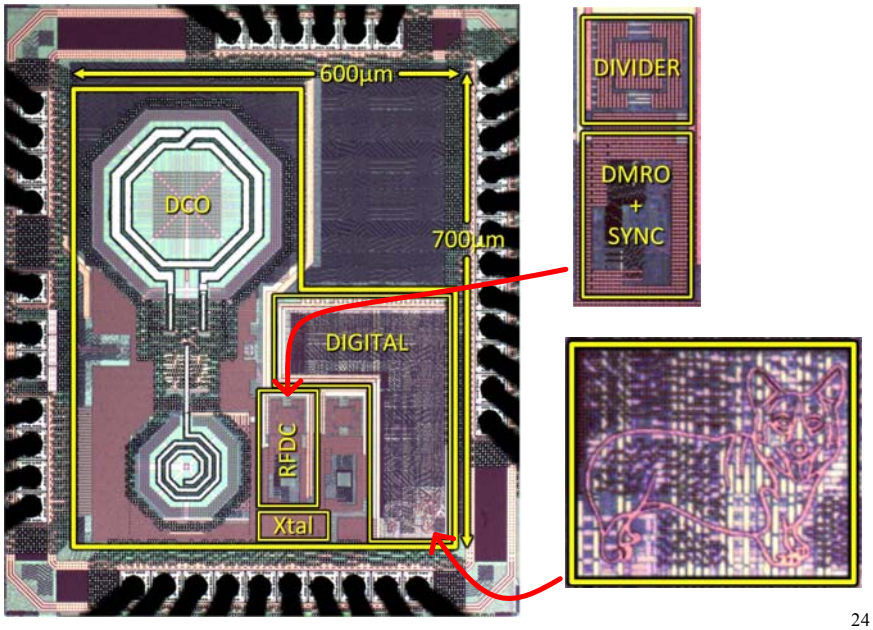
Power Diss. Breakdown	mA
Digital	4.6
Reference Oscillator	0.3
DCO and Output Buffer	9.0
ΔΣ FDC	1.7

Performance Comparison

Citation	This Work	[1]	[2]	[3]	[4]	[5]	[6]
Technology (nm)	65	90	130	130	65	55	65
Supply (V)	1.0	1.2	1.5	?	1.2	1.5	1.5/1.2
Power Diss. (mW)	15.6	?	39	>40	8.7	41.6	45
Area (mm^2)	0.35	?	0.95	0.86	0.44	0.7	0.6
Ref Freq (MHz)	26	26	50	26	35	26	78
PLL Freq (GHz)	3.5	3.6	3.7	3.6	3.5	1.8	4.0
PLL BW (kHz)	140	40	500	50	3400	800	1000
Norm In-Band PN (dBc/Hz)	−93	−81	−107	−79	−101	−102	−109
Norm PN@1MHz (dBc/Hz)	−126	−117	?	−126	?	?	?
Norm PN@3MHz (dBc/Hz)	−138	?	−131	−136	?	−122	?
Norm PN@20MHz (dBc/Hz)	−151	−152	−149	−152	−129	−154	−149
Reference Spur (dBc	−81	−92	−65	−84	−61	?	−56
In-Band Fract. Spur (dBc)	−60	?	−42	?	−58	−50	−40

Phase noise normalized to 3.5 GHz

Die Photo



Conclusion

- Have presented a new type of digital PLL
- Its quantization noise is equivalent to that of an analog PLL with 2nd-order ΔΣ modulation
- Consequently, it circumvents the spurious tone versus noise tradeoff of prior digital PLLs
- This is demonstrated by state-of-the-art measured results
  - Lower power dissipation than all prior digital PLLs with comparable noise performance
  - lower spurious tones than all prior digital PLLs