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A Multiple-Crystal Interface PLL with VCO Realignment to Reduce Phase Noise

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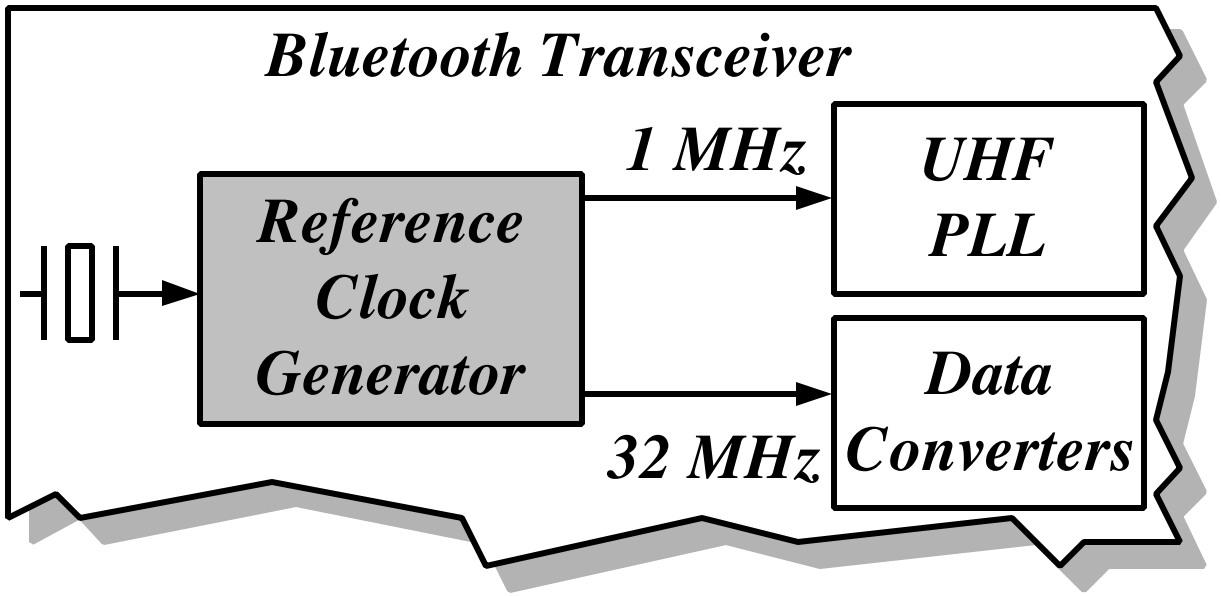
Outline

- Motivation
- Proposed PLL architecture
- Theoretical analysis
- Measured results
- Summary

Clock Generation for Bluetooth

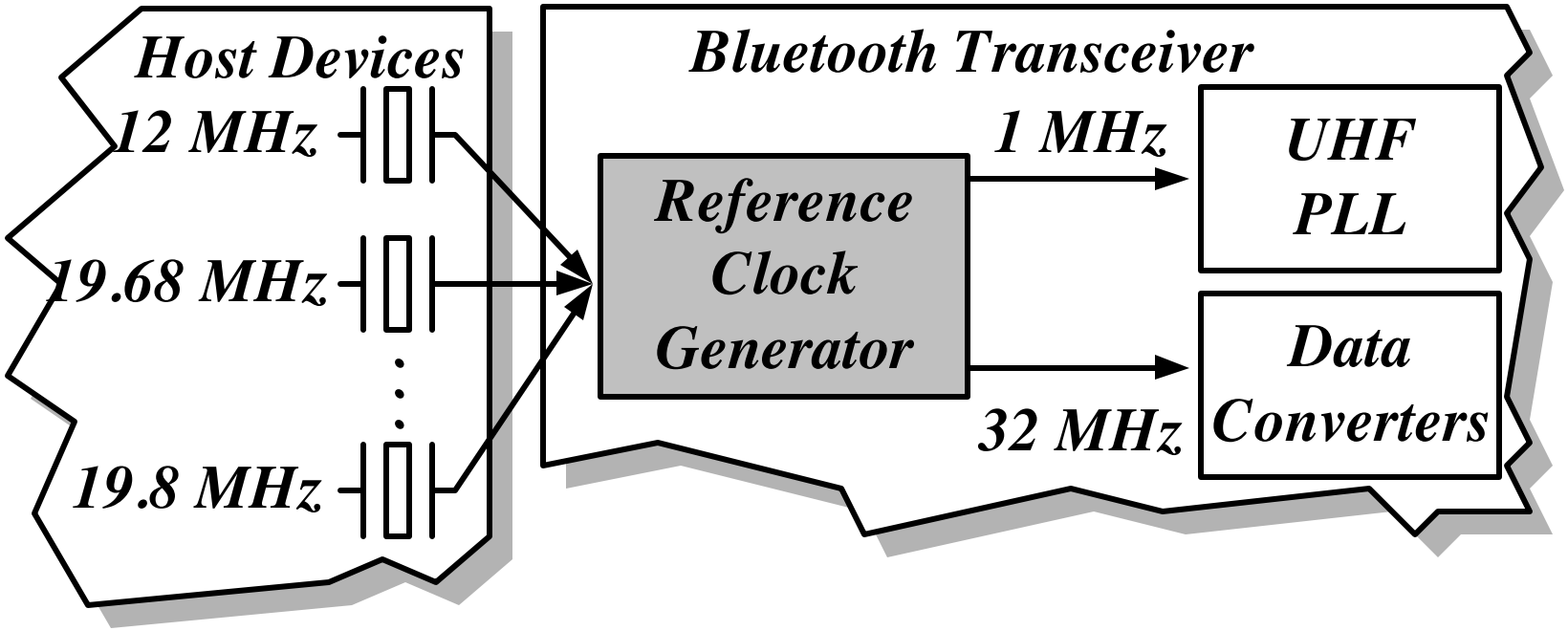


- Clock generator phase noise requirements:

  1 MHz: *low* (e.g., -140dBc/Hz @ 20kHz)

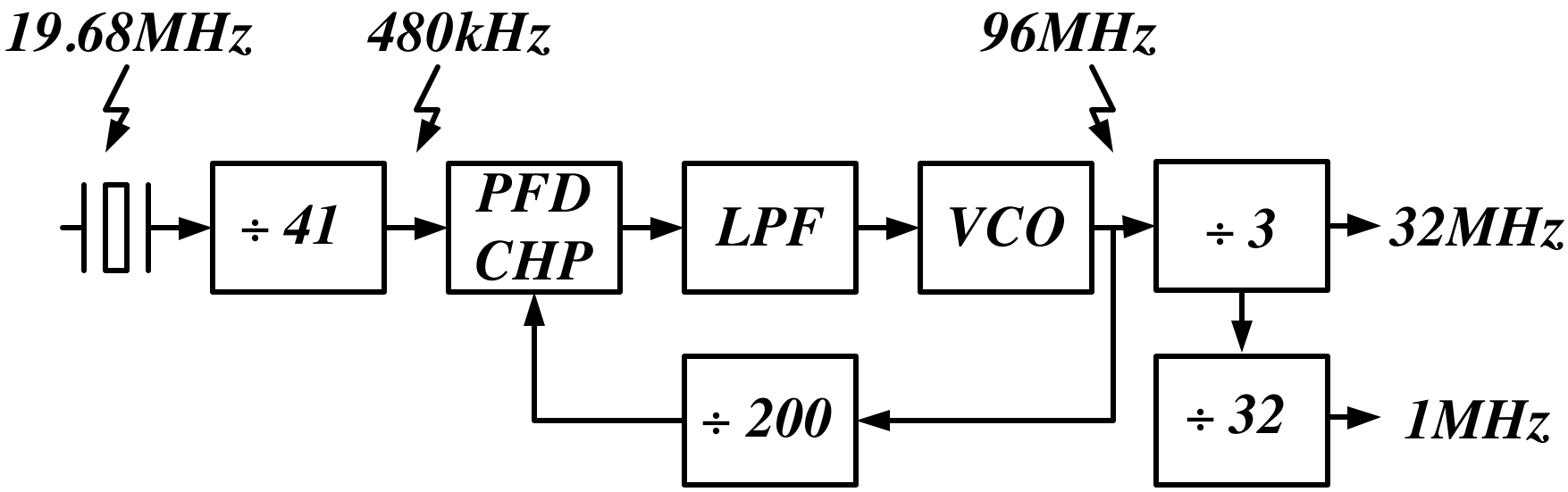
  32 MHz: *moderate* (e.g., -97dBc/Hz @ 20kHz)

Clock Generation For Bluetooth



Objective:		**Requirement:**
• Low cost	⇒	multiple crystal compatibility
• High integration	⇒	use ring VCO
• Low complexity	⇒	use integer-*N* PLL

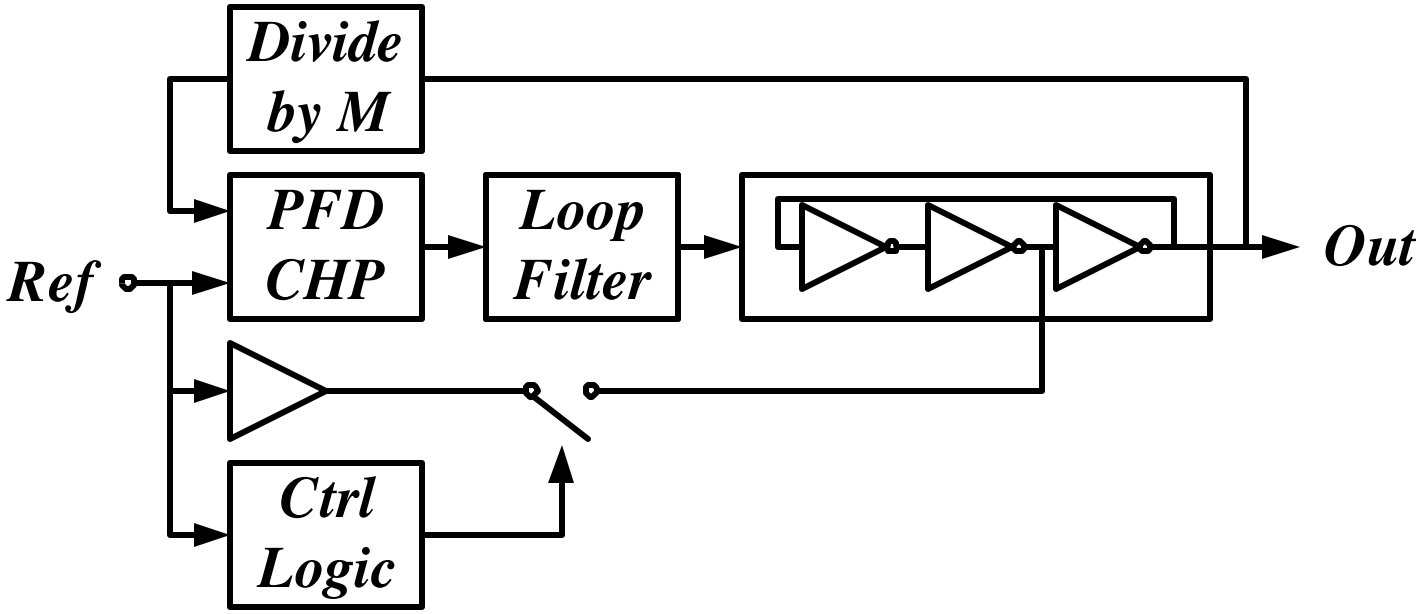
The Problem with a Conventional PLL



- Stability requirement ⇒ bandwidth < 25 kHz
- Noisy ring VCO
- Low noise spec

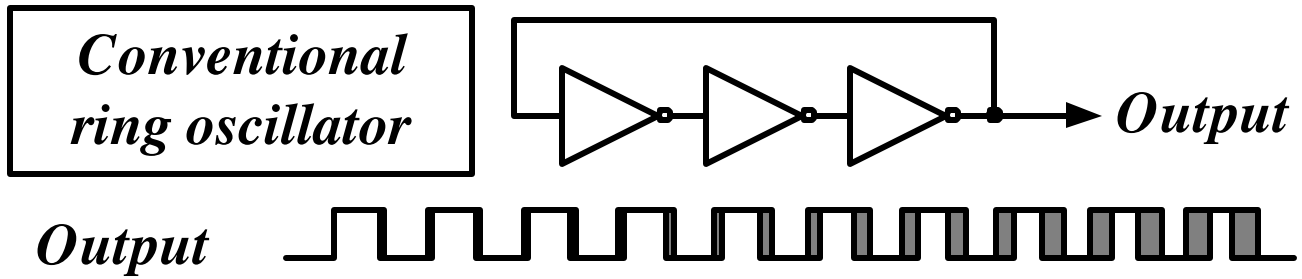
} ⇒ bandwidth > 100 kHz

Our Approach: Phase Realigned PLL



Conventional integer-*N* PLL *except* the VCO phase is realigned periodically to a buffered reference edge

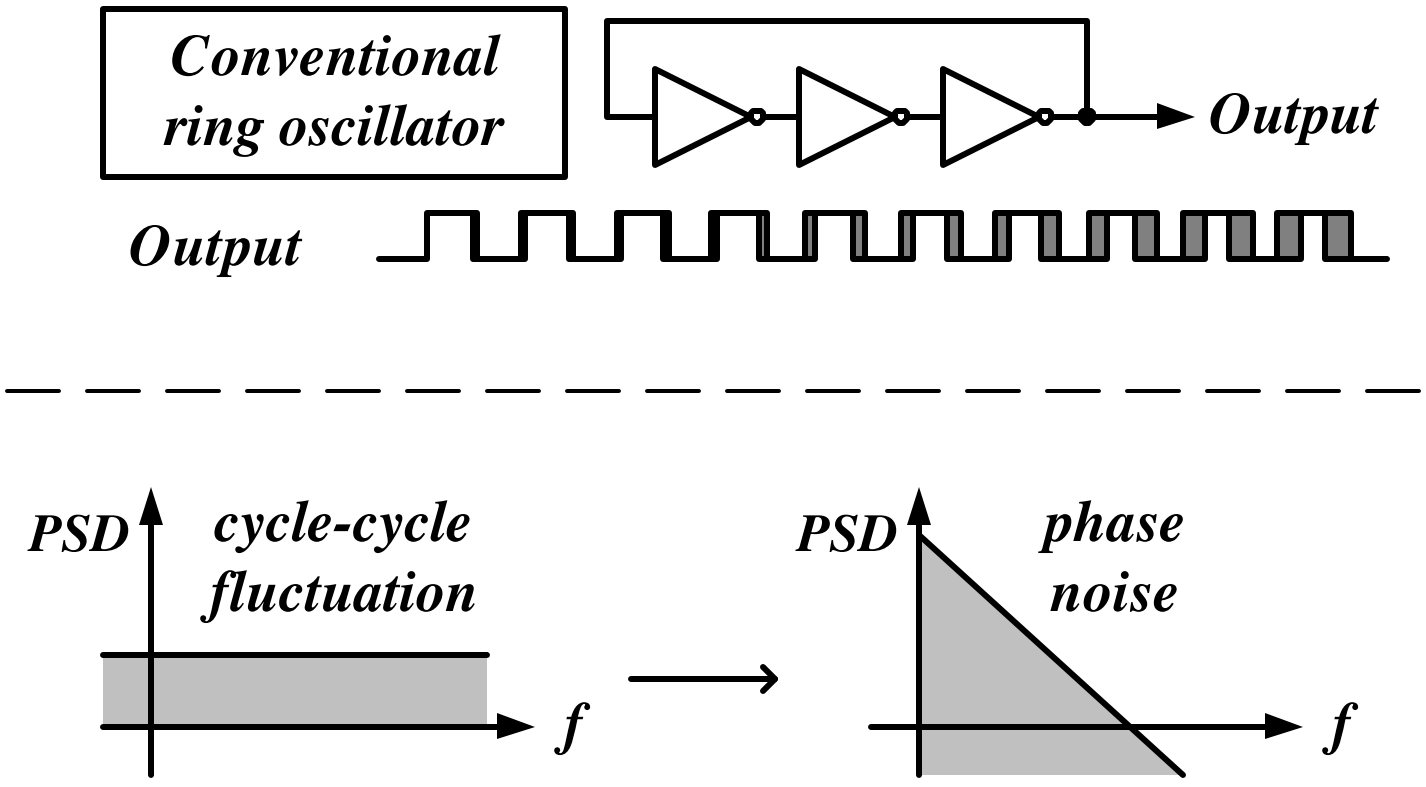
Oscillators Accumulate Phase Errors



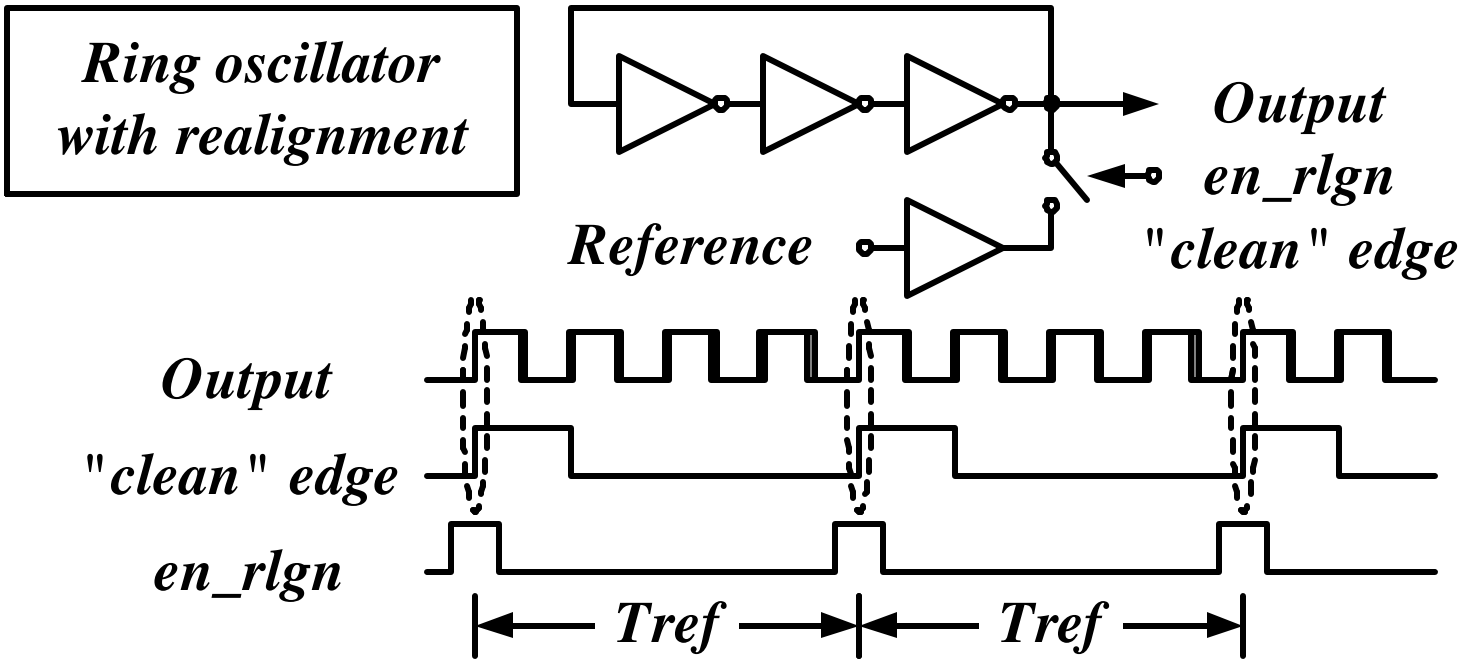
- Circuit noise ⇒ phase error in oscillators
- Phase error is accumulated in oscillators†
  - ⇒ Oscillator "remembers" previous phase errors
  - ⇒ Oscillator acts as a phase error integrator
  - ⇒ high phase noise in PLL passband

† [G.Chien *et al*., ISSCC 2000]

Oscillators Accumulate Phase Errors

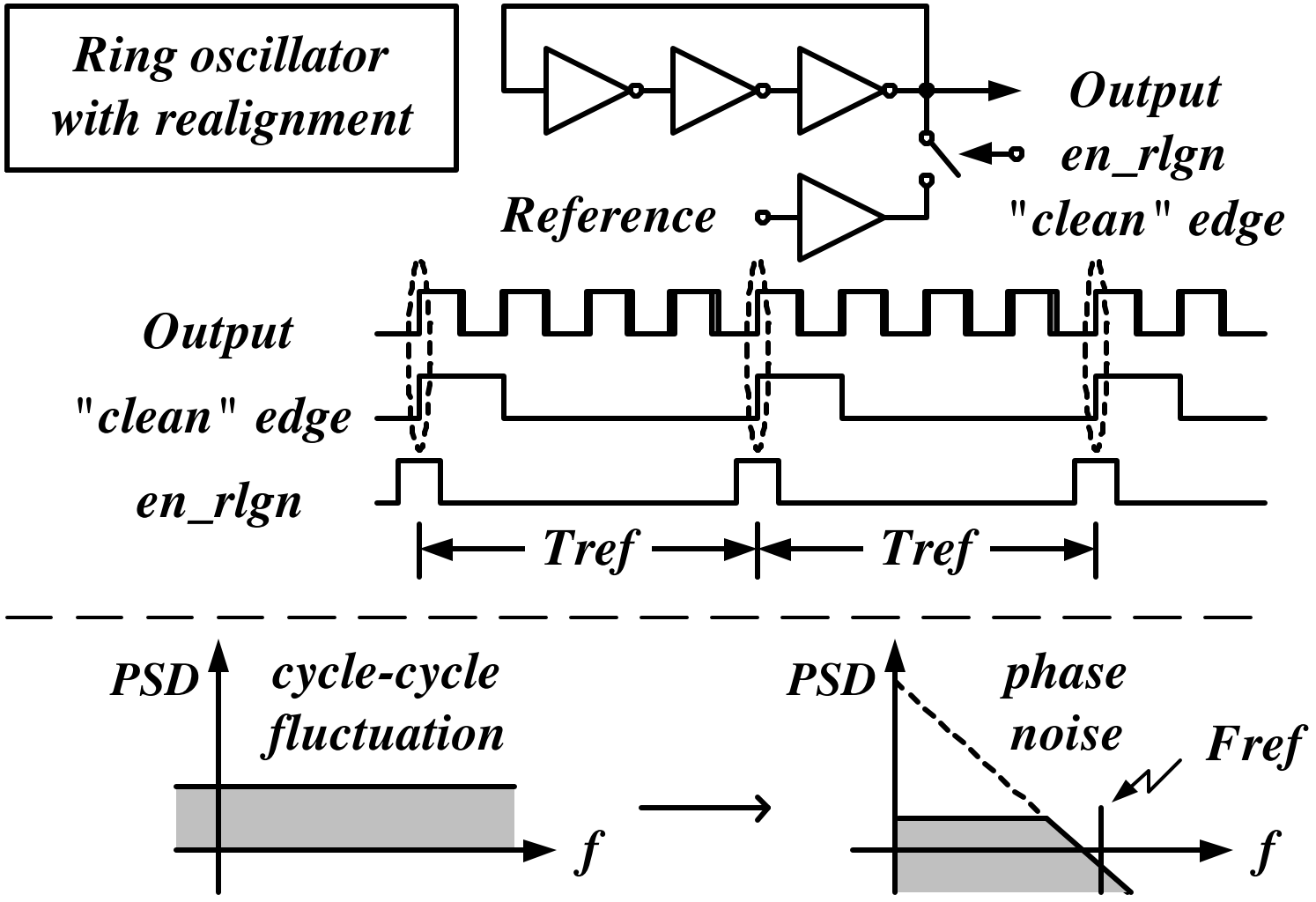


Realignment Blocks Noise Memory

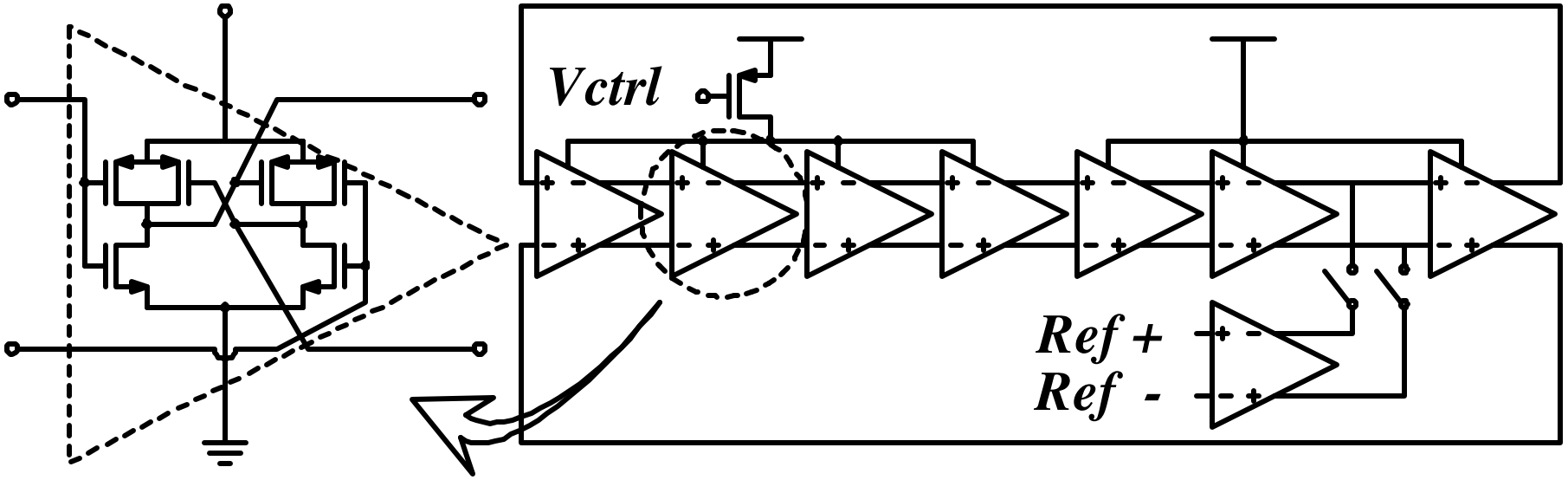


Periodically realigning the oscillator to a "clean" edge suppresses noise accumulation

Realignment Blocks Noise Memory



Realigned VCO Prototype



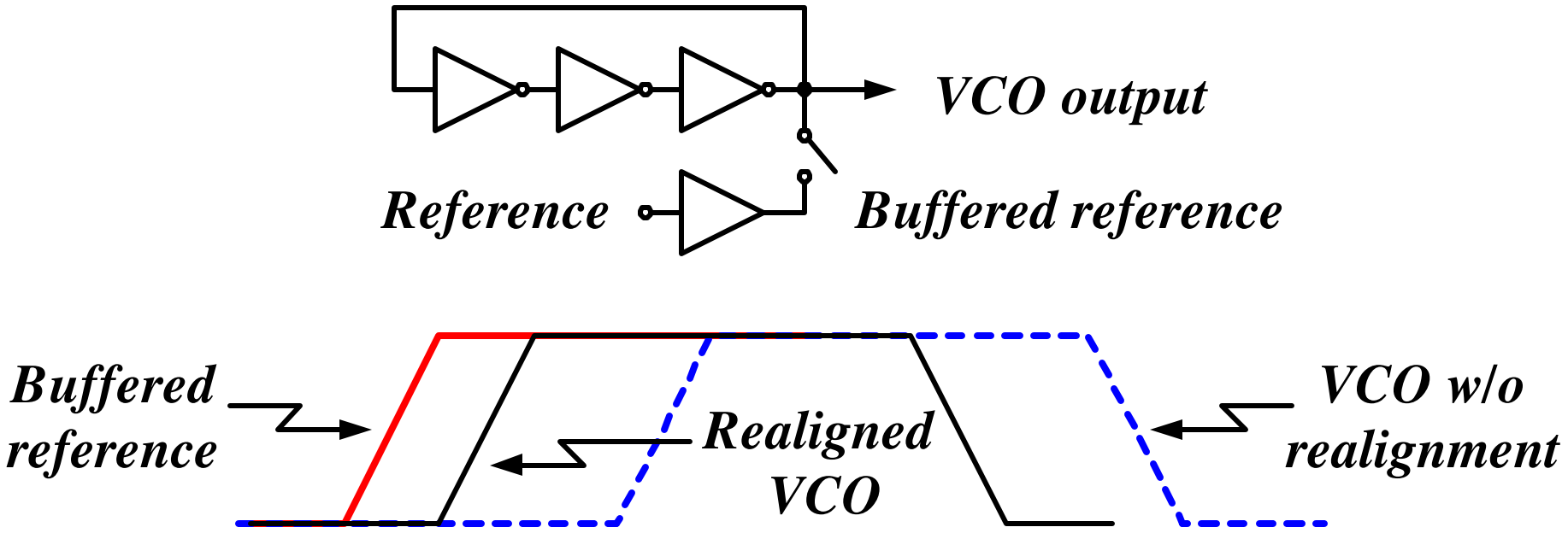
- 7-stage ring VCO:

4 stages, variable delay → frequency control

3 stages, fixed delay → phase realignment

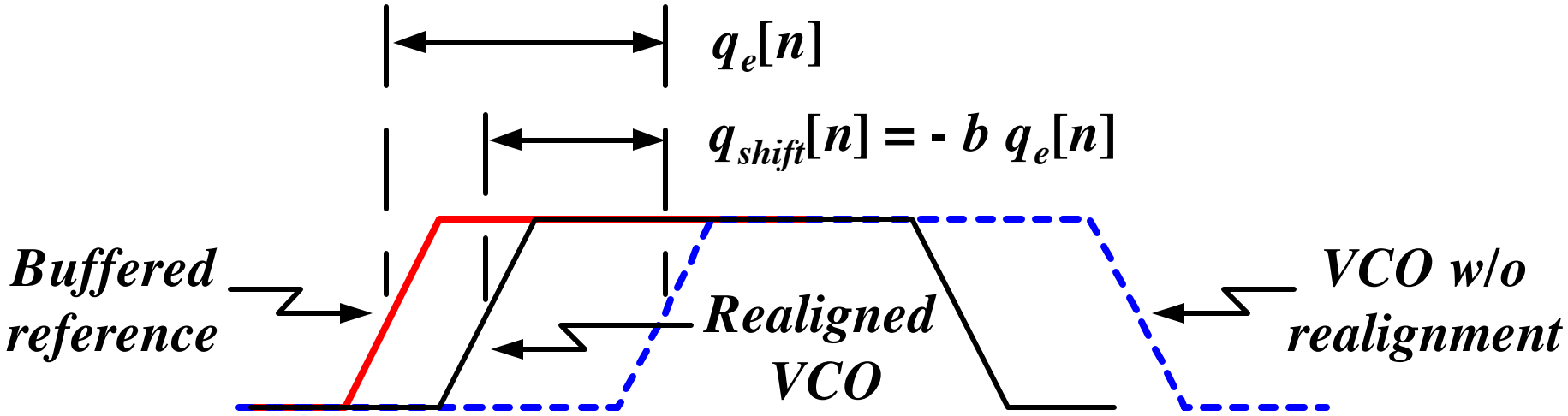
→ reduce disturbance

Phase Realigning Details (1)



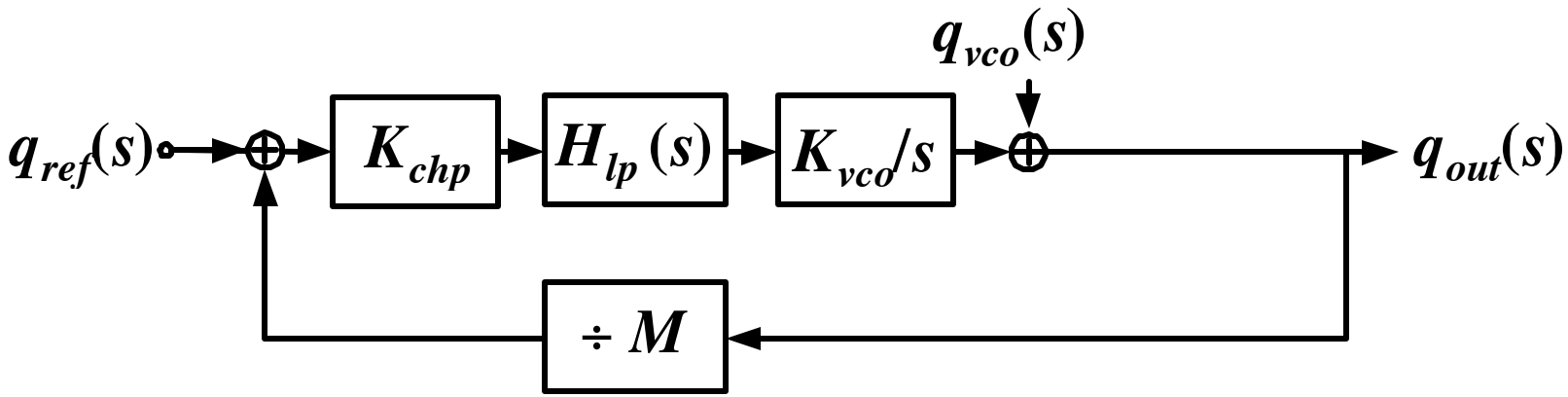
- VCO and buffered reference are in phase nominally; phase error is due to noise
- Phase realignment pulls the VCO edge toward its “correct” value

Phase Realigning Details (2)



- VCO phase shifts almost instantly when realigned
- VCO phase shifts almost linearly to phase error by a factor of β. ($0 \leq \beta \leq 1$)

Known Model for Conventional PLL



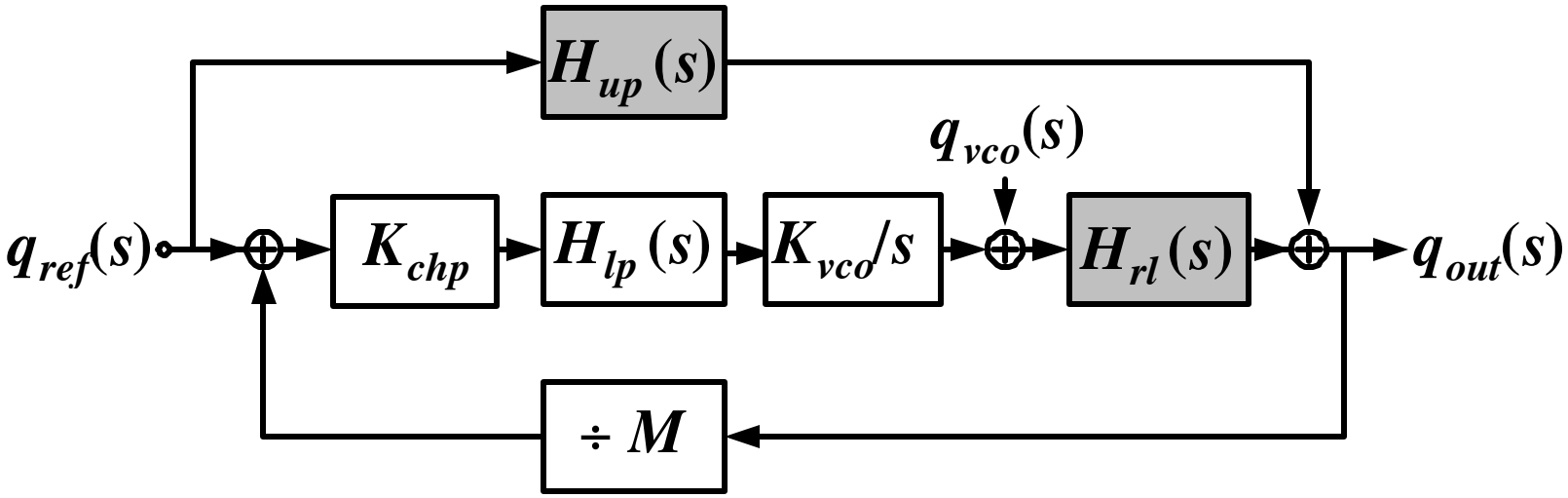
K_{chp}= Charge pump gain

K_{vco}=VCO gain

H_{lp}(s) = Loop filter transfer function

M = Divider ratio

Modified Model for Realigned PLL

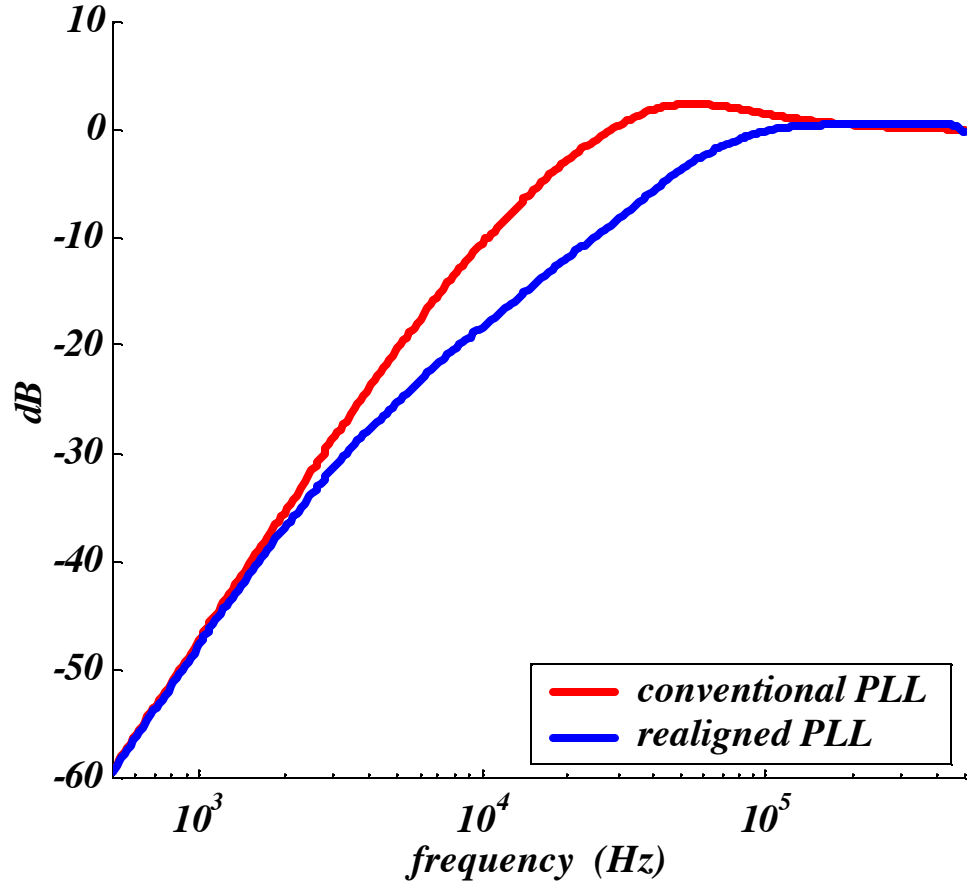


Realignment $\Rightarrow$ two new blocks:

$H_{up}(s)$: up-conversion of reference noise

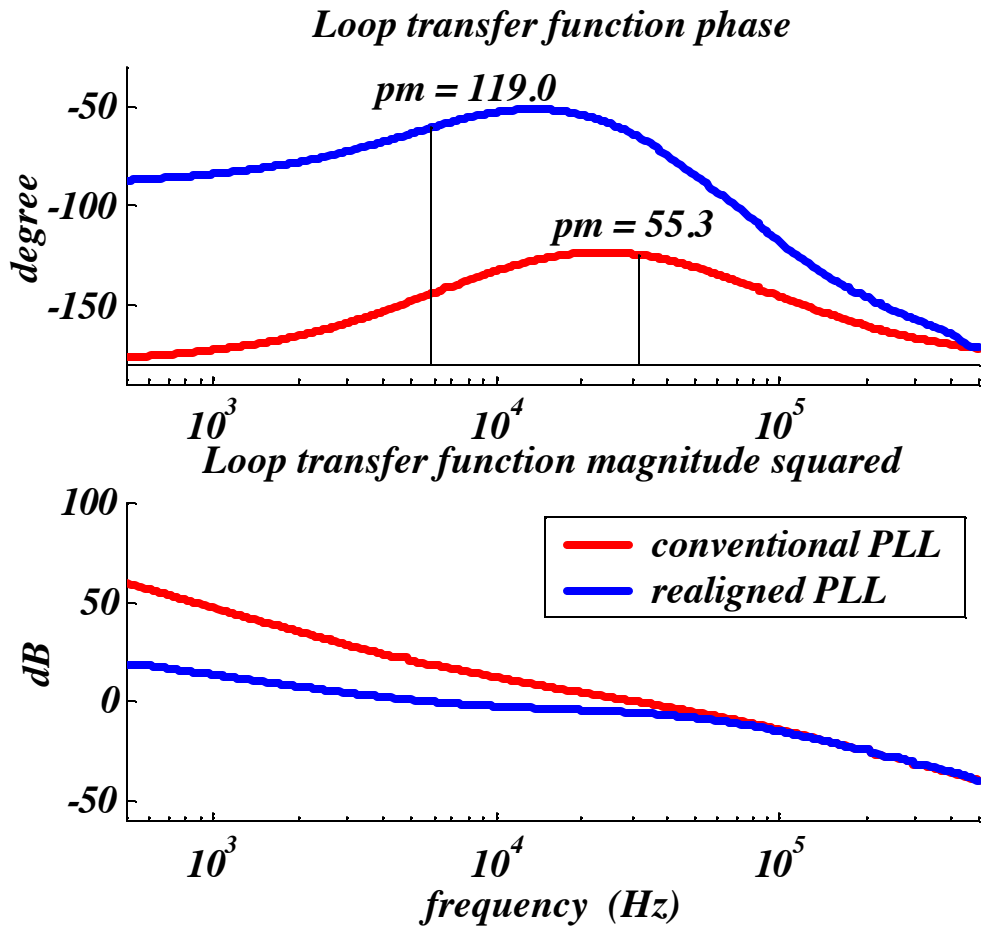
$H_{rl}(s)$: transfer function of realignment

VCO Phase Noise Transfer Function



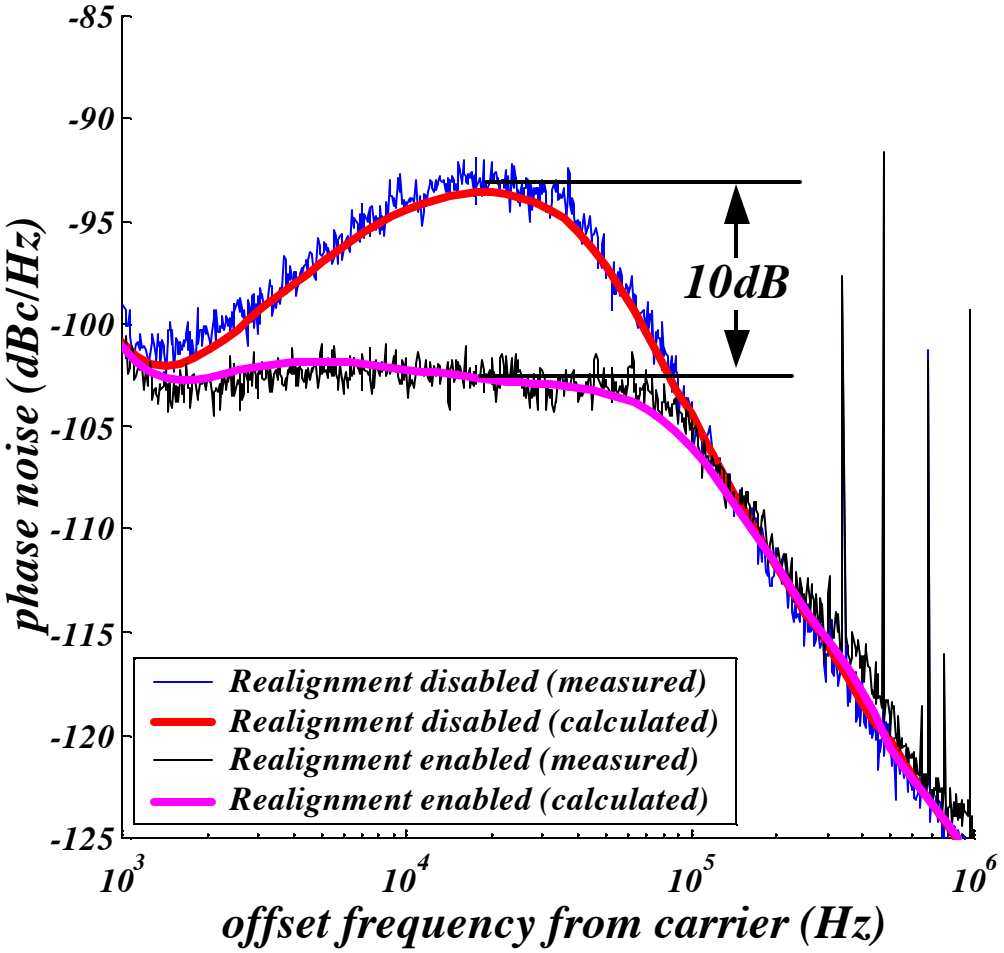
$\Rightarrow$ Realignment widens the noise stopband

Loop Transfer Function



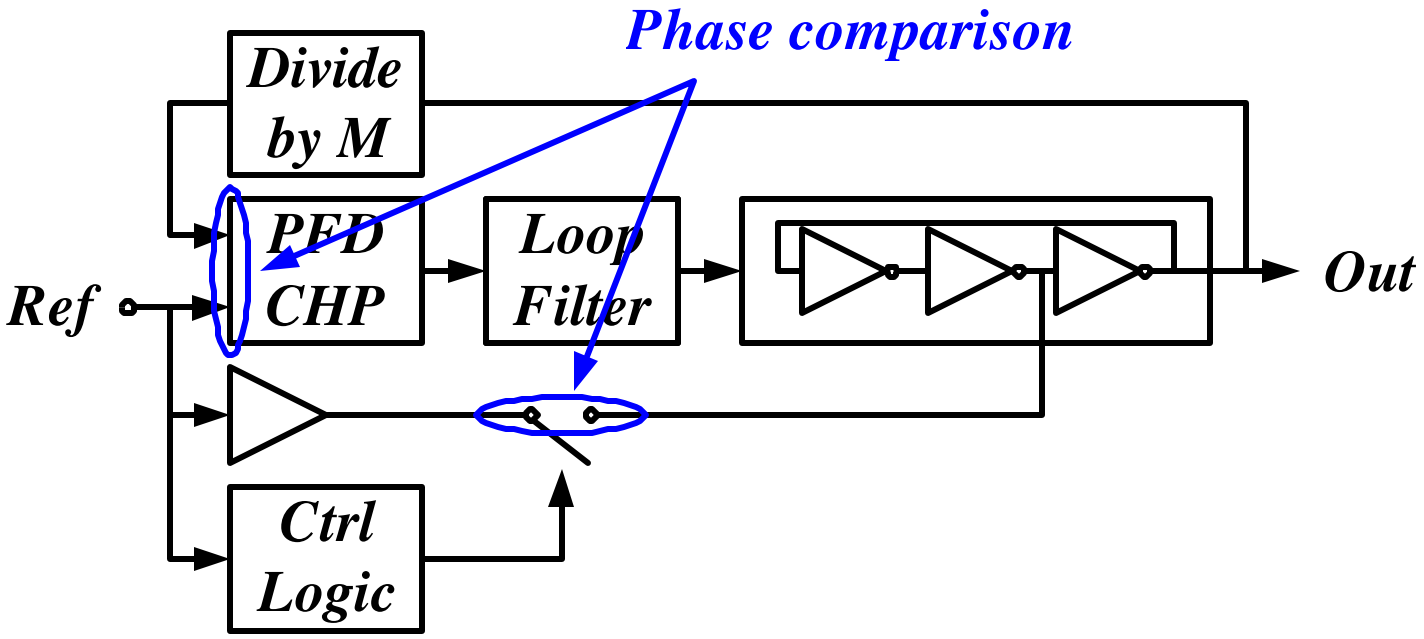
⇒ Realignment increases the phase margin

Measurement Versus Theory



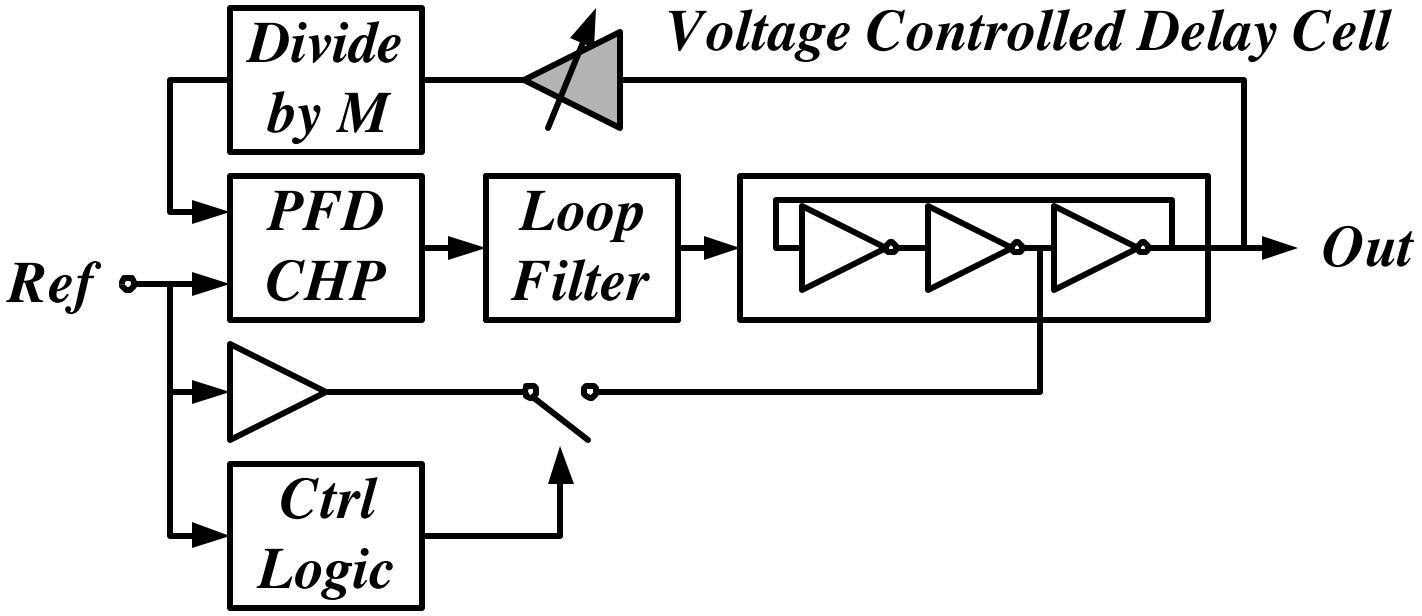
f_{ref} = 480 kHz, PLL bandwidth = 25 kHz

Reference Spur Issue



- 2 reference signal paths; 2 phase comparisons
- Delay mismatch ⇒ more reference spur power
- Realignment disabled: -78 dBc spur
- Realignment enabled: -34 dBc spur

Reference Spur Reduction

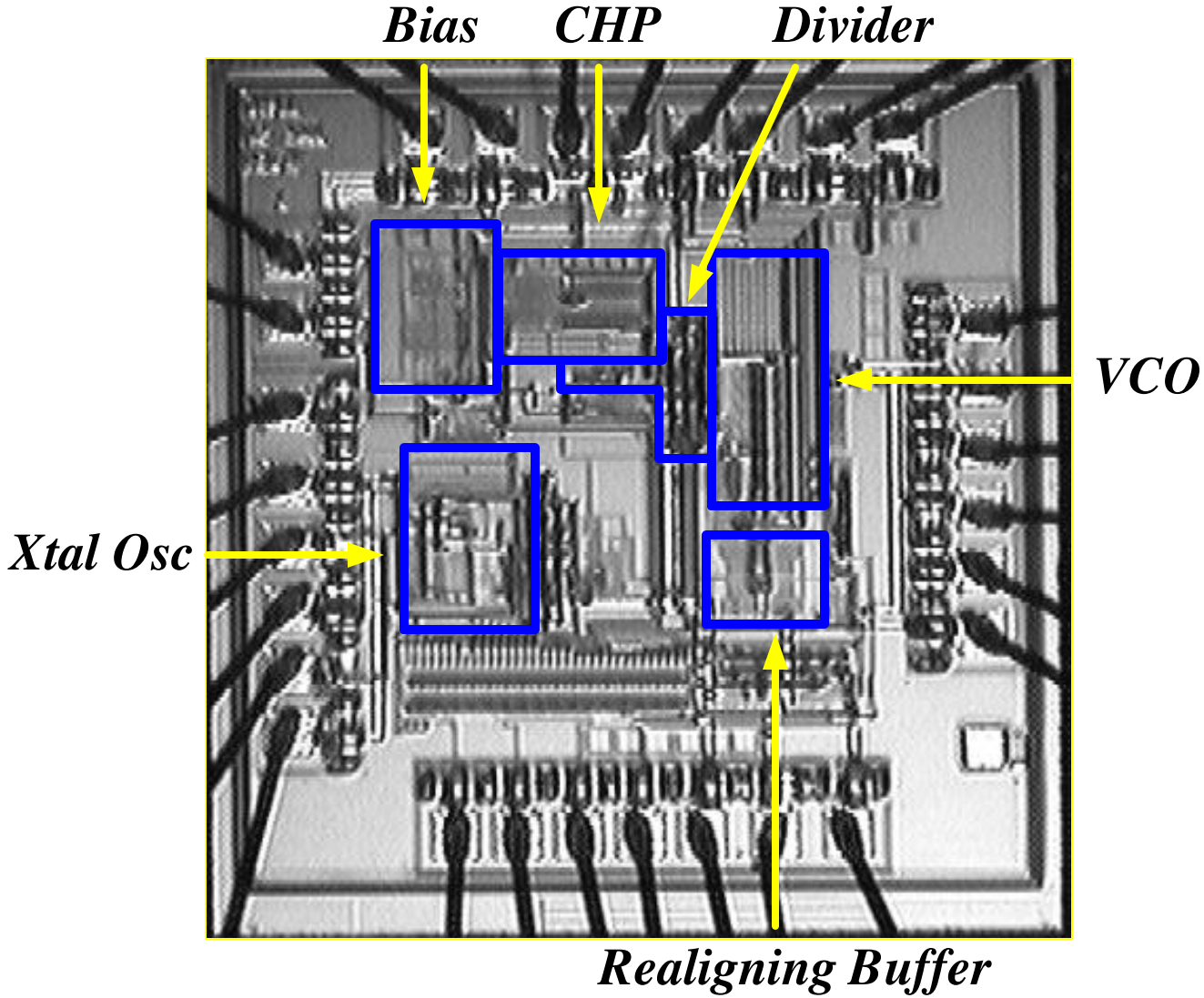


- Variable delay ⇒ compensate for mismatch
- Manual calibration ⇒ -71 dBc spur
- Auto-calibration loop feasible

Performance Summary

Technology	**0.35 μm BiCMOS SOI (with only CMOS components used)**
Supply voltage	**2.7-3.3V (measurements at 3V)**
Total power consumption	**6.8mW (no observable difference when realignment enabled)**
Die size	**1.8 mm^2**
Realigned PLL core area	**0.22 mm^2. Conventional PLL: 73% Realignment circuitry: 27%**
Spot noise @ 20 kHz Offset	**-92.5 dBc/Hz (realignment disabled) -102.5 dBc/Hz (realignment enabled)**
Reduction of noise power from 1 kHz - 50 kHz	**8.3 dB w/ 25 kHz PLL bandwidth 5.3 dB w/ 50 kHz PLL bandwidth**

Die Photo



Summary

- A new VCO phase realignment technique has been presented and shown to significantly reduce phase noise in an integer-*N* PLL

- A theoretical model has been developed that closely supports the measured results