# INFORMATION TO USERS

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Enabling Techniques for High-Resolution Analog-to-Digital

Conversion in IC Fabrication Processes Optimized for Digital Circuits

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy

in Electrical and Computer Engineering (Electronic Circuits & Systems)

by

Eric John Fogleman

Committee in charge:

Professor Ian Galton, Chair
Professor William Hodgkiss
Professor Miller Puckette
Professor Paul Siegel
Professor Bang-Sup Song

2000

UMI Number: 9970652

# UMI®

To my mother and father

# TABLE OF CONTENTS

# LIST OF FIGURES

Chapter 4

# LIST OF TABLES

# ACKNOWLEDGMENTS

Ferguson, Eric Nestler, David Johns, Nick van Bavel, Mike Brunolli, Lisa Lipscomb, Richard Henry, Bill Levine, Bill Hawkins, Walter McWilliams, Susan Miller, and James Torretti.

This dissertation is a collection of four papers that are intended for separate publication. Each paper forms a separate chapter of the dissertation. Chapter 1 appeared in the March 2000 issue of the *IEEE Journal of Solid State Circuits*. The research covered in Chapter 1 was presented at the *IEEE Custom Integrated Circuits Conference*, May 16–19, 1999, San Diego, California. Chapter 2 is in preparation for submission to the *IEEE Journal of Solid State Circuits*, and this research was presented at at the *IEEE Custom Integrated Circuits Conference*, May 21–24, 2000, Orlando, Florida. Chapter 3 has been submitted to the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* for review. Chapter 4 is in preparation for submission to *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*. Portions of the research presented in Chapters 3 and 4 were presented at the *IEEE International Symposium on Circuits and Systems*, May 30–June 2, 1999, Orlando, Florida.

# VITA

| | |
|---|---|
| 1990 | Bachelor of Science, University of Maryland, College Park |
| 1990–1993 | Product/Test Engineer,<br>Analog Devices Incorporated, Wilmington, Massachusetts |
| 1993–1995 | Senior Product Engineer,<br>Brooktree Corporation, San Diego, California |
| 1995–1996 | Senior Design Engineer,<br>Brooktree Corporation, San Diego, California |
| 1996–1998 | Graduate Student Researcher,<br>Department of Electrical and Computer Engineering,<br>University of California, San Diego |
| 1998 | Master of Science, University of California, San Diego |
| 1998–2000 | Graduate Student Researcher,<br>Department of Electrical and Computer Engineering,<br>University of California, San Diego |
| 2000 | Doctor of Philosophy, University of California, San Diego |

# PUBLICATIONS

E. Fogleman and I. Galton, "A digital common-mode rejection technique for differential analog-to-digital conversion," *IEEE Trans. Circuits Syst. II*, in preparation.

E. Fogleman and I. Galton, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADCs," *IEEE Trans. Circuits Syst. II*, under review.

E. Fogleman, J. Welz, and I. Galton, "An audio ADC delta-sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC," in *IEEE Custom Integrated Circuits Conf.*, May 2000, pp. 17-20.

E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB peak SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 297-307, March 2000.

E. Fogleman, I. Galton, and H. Jensen, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADCs," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2 of 6, June 1999, pp. 290-293.

E. Fogleman, I. Galton, and H. Jensen, "An area-efficient differential input ADC with digital common mode rejection," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2 of 6, June 1999, pp. 347-350.

E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3V single-poly CMOS audio ADC delta-sigma modulator with 98dB peak SINAD," in *IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 121-124.

# ABSTRACT OF THE DISSERTATION

Enabling Techniques for High-Resolution Analog-to-Digital

Conversion in IC Fabrication Processes Optimized for Digital Circuits

by

Eric John Fogleman

Doctor of Philosophy in Electrical and Computer Engineering

(Electronic Circuits & Systems)

University of California, San Diego, 2000

Professor Ian Galton, Chair

ADVANCES in CMOS integrated circuit (IC) fabrication technology have made it possible to use digital signal processing techniques to realize many signal processing functions traditionally implemented with analog circuits. In communication systems, digital filters provide well-controlled frequency responses that do not depend on the matching of circuit elements. In audio signal processing systems, digitally-controlled gain and attenuation circuits can control signal levels without "clicks" and "pops" due to dc offsets in analog implementations. In addition, digital hardware is well-suited to the application of adaptive signal processing techniques.

Exploiting these benefits to provide a highly-integrated, single-chip solution requires analog-to-digital converters (ADCs) which can be integrated on a single chip in a CMOS fabrication process optimized for digital circuits. Current digital-optimized CMOS processes are typically limited to supply voltages below 3.3 V and lack high-quality passive components such as thin-oxide linear capacitors. As a result, designing analog circuits to achieve 16-bit resolution at conversion rates of 48 kS/s to 200 kS/s in such a process is a challenging task.

This dissertation presents signal processing techniques developed to enable the implementation of high-resolution analog-to-digital converters in digital-optimized CMOS fabrication processes. These techniques are implemented in digital circuitry and significantly ease the design of the analog circuits in the ADC. Chapter 1 presents a prototype audio-rate multibit ADC $\Delta\Sigma$ modulator using a 33-level first-order mismatch-shaping DAC which achieves 98-dB peak signal-to-noise-and-distortion (SINAD) and 105-dB spurious-free-dynamic-range (SFDR). Chapter 2 presents a prototype audio-rate multibit ADC $\Delta\Sigma$ modulator using a low-complexity 33-level second-order mismatch-shaping DAC which achieves 100-dB peak SINAD and 103-dB dynamic range. Chapter 3 presents the implementation and theoretical details of a dynamic element matching technique used in the prototype $\Delta\Sigma$ modulators to provide spectral whitening of comparator offset errors in the 33-level flash ADC quantizer. Chapter 4 presents the implementation and theoretical details of a digital common-mode rejection flash ADC used to provide differential quantization of the differential output of the switched-capacitor loop filter.

# Chapter 1

# A 3.3-V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98-dB Peak SINAD and 105-dB Peak SFDR

Eric Fogleman, Ian Galton, William Huff, Henrik Jensen

**Abstract**—This paper presents a second-order $\Delta\Sigma$ modulator for audio-band analog-to-digital conversion implemented in a 3.3-V, 0.5-$\mu$m, single-poly CMOS process using metal-metal capacitors that achieves 98-dB peak signal-to-noise-and-distortion and 105-dB peak spurious-free-dynamic-range. The design uses a low-complexity first-order mismatch-shaping 33-level digital-to-analog converter and a 33-level flash analog-to-digital converter with digital common-mode rejection and dynamic element matching of comparator offsets. These signal processing innovations, combined with established circuit techniques, enable state of the art performance in CMOS technology optimized for digital circuits.

## I. INTRODUCTION

FOR mixed-signal ICs with high digital circuit content, single-poly CMOS optimized for digital circuits can provide the lowest overall implementation cost. For example, it is preferable to avoid the expense of double-poly capacitors, thick-oxide transistors for 5-V operation, or other analog process enhancements when analog circuits such as data converters make up only a small portion of the total die area. This is often true even if the lack of analog enhancements significantly increases the area of the analog circuitry. However, the performance that can be achieved by data converters in a digital-optimized, single-poly CMOS process may limit the extent to which this advantage can be exploited.

1

High-resolution data converters require linear capacitors and low-noise, low-distortion amplifier circuits to implement fundamental building blocks such as sample-and-holds, integrators, and comparators. Though the specific circuits and performance specifications are determined by the data converter's architecture, the lack of linear capacitors with low parasitic capacitance, and process-related supply voltage restrictions in modern, digital-optimized, single-poly CMOS processes generally present key challenges in realizing high-performance data converters.

In a CMOS process without double-poly capacitors or other thin-oxide, linear capacitor structures, the metal interconnect layers or MOS structures must be used to implement capacitors. MOS capacitor structures (MOSCAPs) require special biasing to keep them in an accumulated or depleted operating region and to mitigate their inherent nonlinearity. Metal interconnect (metal-metal) capacitors are inherently linear, but for a given value of capacitance, a metal-metal capacitor can require as much as 30 times the area of a double-poly capacitor. Moreover, the bottom plate capacitance of a metal-metal capacitor is comparable to the inter-plate capacitance, while the double-poly capacitor's parasitic capacitance is typically less than 50% of the inter-plate capacitance.

Process-related limitations on supply voltages to 3.3 V or below restrict signal swings in amplifiers and through analog switches. In switched-capacitor circuits, this necessitates increased sampling capacitances to achieve the target signal to thermal noise ratio. In switched-capacitor integrators, large feedback capacitances may be required to scale the output down to fit within the amplifier's output swing. Thus, the reduced headroom and increased loading complicate the task of realizing fast settling, low-distortion switched-capacitor circuits.

It might be possible to mitigate these problems through critical refinement of

the analog circuits, but a strategy that uses digital processing to minimize the performance requirements of the analog circuits makes better use of the strengths of a digital-optimized CMOS process. Multibit $\Delta\Sigma$ modulation using mismatch-shaping DACs exemplifies this approach. By reducing the quantization noise power to be shaped out of band relative to two-level quantization, a multibit $\Delta\Sigma$ modulator can achieve the same SINAD with a lower order $\Delta\Sigma$ modulator and a lower oversampling ratio than a single-bit design. The reduction in $\Delta\Sigma$ modulator order implies that fewer switched-capacitor stages are required, and the reduced oversampling ratio relaxes the bandwidth and slew rate requirements on the integrators. The mismatch-shaping DAC in the feedback path causes static DAC mismatch errors to fall predominantly outside the signal band and significantly relaxes the matching requirements on the DAC's analog components [1]-[12].

The multibit approach eases the design requirements on the switched-capacitor circuits, but it also introduces several new design challenges. The transfer function from the first integrator input to the $\Delta\Sigma$ modulator output provides no noise shaping. Therefore, the first stage feedback DAC must have the same signal-band precision as the overall data converter. Furthermore, the reduced $\Delta\Sigma$ modulator order and oversampling ratio imply that the noise transfer function provides less attenuation of circuit noise and distortion in the flash ADC quantizer. Thus the flash ADC must provide sufficient common mode noise rejection and SFDR performance to meet the overall data converter's performance targets.

This paper presents an audio ADC $\Delta\Sigma$ modulator implemented in a 3.3-V, 0.5-$\mu$m CMOS process using metal-metal capacitors that achieves 98-dB SINAD and 105-dB SFDR [13]. To the knowledge of the authors, this level of performance has not been achieved previously under these process constraints [14]-[16]. The
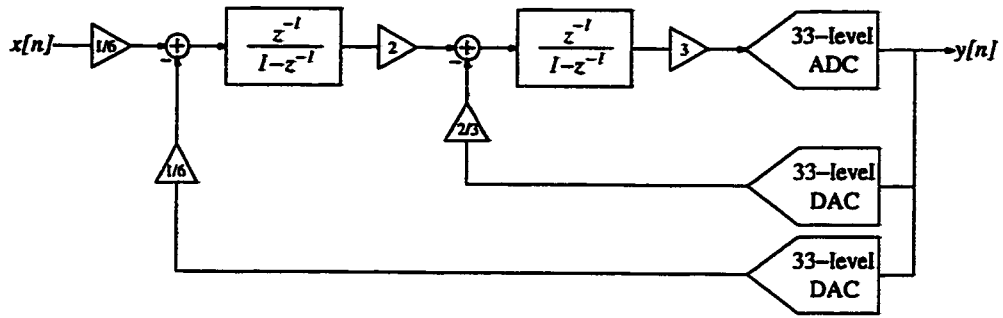
**Figure 1.1:** The high-level $\Delta\Sigma$ modulator topology.

$\Delta\Sigma$ modulator makes extensive use of digital processing to simplify or avoid analog circuit design problems and minimize the use of large-area metal-metal capacitors. A low-complexity mismatch shaping DAC digital encoder provides spur-free, first-order shaping of static mismatches in the feedback DAC. The differential input flash ADC uses a pair of single-ended, 33-level flash ADCs whose binary outputs are subtracted to reject common mode noise. The flash ADC comparators use a dynamic element matching technique to spectrally whiten spurious tones caused by their static input offsets. A modified linear feedback shift register (LFSR) efficiently provides the multiple uncorrelated pseudo-random sequences required by the mismatch-shaping DAC and flash ADC.

The remainder of the paper consists of three main sections. Section II presents the signal processing innovations of the $\Delta\Sigma$ modulator, the mismatch-shaping DAC, the flash ADC and the pseudo-random sequence generator. Section III provides circuit implementation details. Section IV describes the layout floorplan and presents measured performance of the $\Delta\Sigma$ modulator prototype.

## II. SIGNAL PROCESSING DETAILS

### DELTA-SIGMA MODULATOR

The prototype is based on the second-order $\Delta\Sigma$ modulator implemented with

Figure 1.2: Mismatch-shaping DAC encoder.

two delaying integrators presented in [17]. The $\Delta\Sigma$ modulator incorporates 33-level quantization, and the coefficients have been modified as shown in Figure 1.1 to match each integrator's full-scale output to the amplifier's output swing. It operates at an oversampling ratio of 64 with an input sample rate of 3.072 MHz. In the absence of non-ideal analog circuit behavior, the $\Delta\Sigma$ modulator achieves a peak signal to quantization noise ratio of 108 dB over the 24-kHz signal band.

Figure 1.3: Switching block implementation.

## MISMATCH-SHAPING DAC DIGITAL ENCODER

The $\Delta\Sigma$ modulator uses the tree-structured mismatch-shaping DAC digital encoder presented in [11]. The encoder, shown in Figure 1.2, operates on the 33-level output of the flash ADC and generates 32 single-bit select lines controlling the two banks of 32 one-bit DAC elements. The 31 switching blocks within the encoder implement a first-order mismatch-shaping algorithm.

To minimize the complexity of the encoder, the implementation shown in Figure 1.3 was used to realize the 31 switching blocks [18]. This circuit is logically equivalent to the dithered first-order switching block shown in [11] but eliminates the need for adders in each block by representing the $(2^b+1)$-level data as $b$ binary bits plus an additional LSB-weighted bit. The resulting 33-level encoder is comprised of 279 combinational logic gates and 62 D flip-flops.

To eliminate spurious tones in the shaped DAC noise, five uncorrelated single-

bit random sequences, denoted as $r_k[n], k = 1, \ldots, 5$ in Figure 1.3, are used to dither the switching blocks in each layer of the encoder [18]. The use of one random sequence per layer of the digital encoder is sufficient to decorrelate the sequences generated by the 31 switching blocks. Assuming $3\sigma = 1\%$ Gaussian-distributed DAC element mismatch, the first-order encoder provides 104-dB peak SINAD.

## DIFFERENTIAL FLASH ADC

To preserve the common mode noise rejection benefits of the fully-differential switched-capacitor circuitry, the flash ADC must quantize the second integrator's differential output with respect to a set of differential reference levels. The second-order noise transfer function provides only 52 dB of attenuation at the passband edge, and thus the flash ADC's common mode rejection is a critical factor in meeting the $\Delta\Sigma$ modulator's 105-dB SFDR target.

A common approach to implementing a differential input flash ADC in a $\Delta\Sigma$ modulator uses a pair of switched-capacitors to sample and compare the differential signal and reference levels on alternate clock phases [19],[20]. For the prototype, sampling capacitors larger than 100 fF would have been required to reduce sufficiently the error caused by charge-sharing with each comparator's parasitic input capacitance. If implemented this way, the 33-level flash ADC would have required an array of 64 capacitors which would have consumed approximately 5% of the entire chip's die area. Moreover, the approach would have required a low output impedance reference ladder capable of driving switched-capacitor loads and would have contributed significant loading of the second integrator. Buffering the reference ladder with source-followers would have presented a circuit design challenge given the limited headroom, and using a low resistance ladder would have significantly increased the power dissipation. To avoid these problems, an approach that
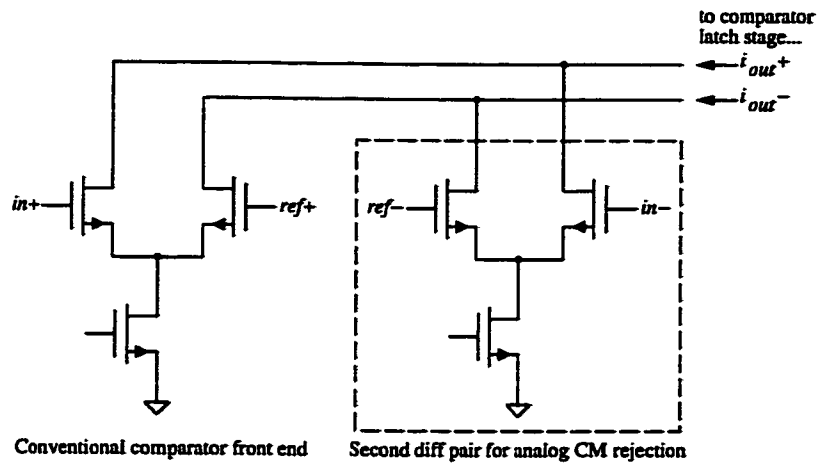
Figure 1.4: A possible analog common mode rejection technique for implementing a differential input flash ADC.

eliminates the need for switched-capacitors is desirable.

In principle, an analog approach that would avoid the need for capacitors involves the use of a comparator with two differential inputs to cancel the common mode component. Such a scheme is shown in Figure 1.4, wherein the comparator converts the signals $(in_+ - ref_+)$ and $(in_- - ref_-)$ to currents using two differential pairs, subtracts the differential currents to cancel the common mode component and sends the resulting signal to a conventional latching stage. While this technique provides small-signal common mode rejection, it can be verified that the common mode signal modulates the differential transconductance. This leads to signal dependent offsets and creates a mechanism for intermodulation of the differential and common mode signals. Though this problem could possibly be mitigated by careful design, the approach was not used because of the aggressive $\Delta\Sigma$ modulator SFDR target.

To provide both large- and small-signal common mode rejection without using additional capacitors, the prototype incorporates digital common mode rejection (DCMR) implemented using a pair of single-ended, 33-level flash ADCs and digital processing to cancel the common mode noise component [21]. As shown in Figure
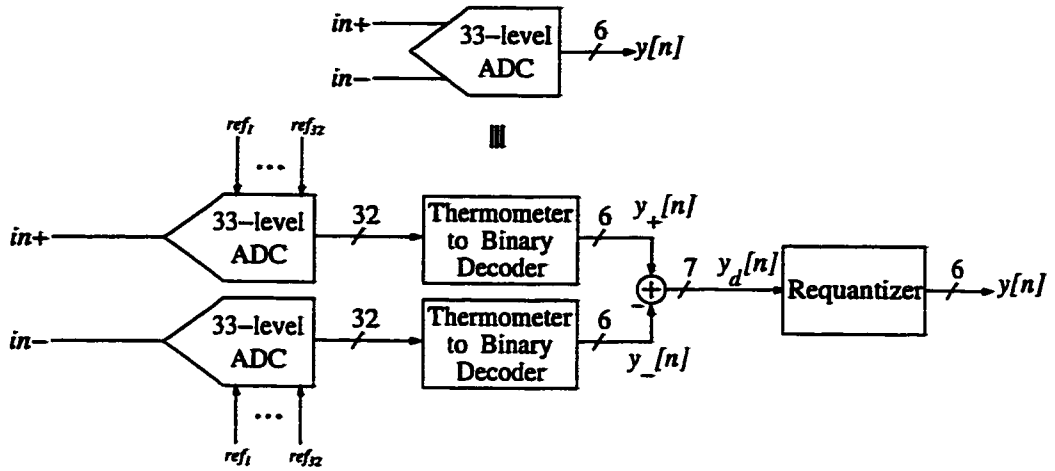
Figure 1.5: High-level view of the 33-level DCMR flash ADC.
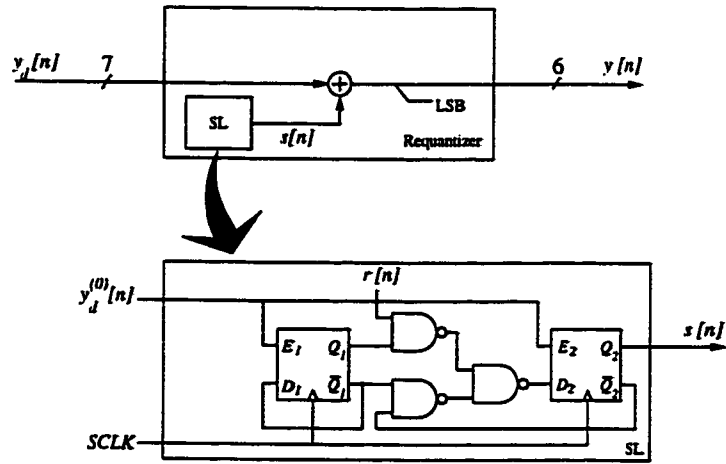


Figure 1.6: Requantizer implementation.

1.5, the single-ended flash ADC outputs, $y_+[n]$ and $y_-[n]$, are subtracted to cancel the common mode component yielding a 65-level difference signal, $y_d[n]$. The difference is requantized to a 33-level signal, $y[n]$, to avoid the need for a 65-level DAC.

In the absence of common mode noise, the DCMR flash ADC is equivalent to a conventional 33-level flash ADC. In this case, the outputs $y_+[n]$ and $y_-[n]$ are complementary signals and the difference signal, $y_d[n]$, takes on only even values. In this case, dropping the LSB of $y_d[n]$ would yield the correct 33-level output.

When common mode noise is present at the input of the DCMR flash ADC, it can be shown that the digital subtraction cancels the common mode noise without generating spurious tones and that the quantization noise power of $y_d[n]$ is between that of a 33-level quantizer and that of a 65-level quantizer. However, $y_+[n]$ and $y_-[n]$ are not complementary in this case, so $y_d[n]$ is a 65-level signal that takes on both even and odd values. Rather than implementing a 65-level mismatch-shaping DAC digital encoder and incurring the additional hardware overhead, a noise-shaping requantizer was used to requantize $y_d[n]$ to a 33-level signal. By rounding odd values of $y_d[n]$ up or down in a first-order, noise-shaped fashion and eliminating the LSB, the circuit shown in Figure 1.6 causes the requantization error to be spur-free and to fall predominantly outside the signal band [21].

Relative to a single differential input ADC, the DCMR architecture requires two single-ended, 33-level flash ADCs, a second bubble correction circuit and thermometer-to-binary encoder, a 6-bit subtractor, a 5-bit adder, a switching block of the type used in the DAC digital encoder, and a single-bit random sequence. The digital circuitry consists of 240 combinational logic gates and two D-flip-flops. As shown in Section IV, this approach yielded net area savings over the switched-capacitor implementation.

## DYNAMIC ELEMENT MATCHING COMPARATOR

The reduced $\Delta\Sigma$ modulator order and oversampling ratio imply that the noise transfer function provides less attenuation of distortion introduced at the quantizer, so the non-linearity of the flash ADC can limit the SINAD and SFDR performance of the $\Delta\Sigma$ modulator. While both reference ladder resistor mismatches and comparator input offsets contribute to errors in the placement of the quantization levels, the comparator offsets are the dominant error source. Input offsets with $\sigma_{V_{os}} \approx 10$ mV
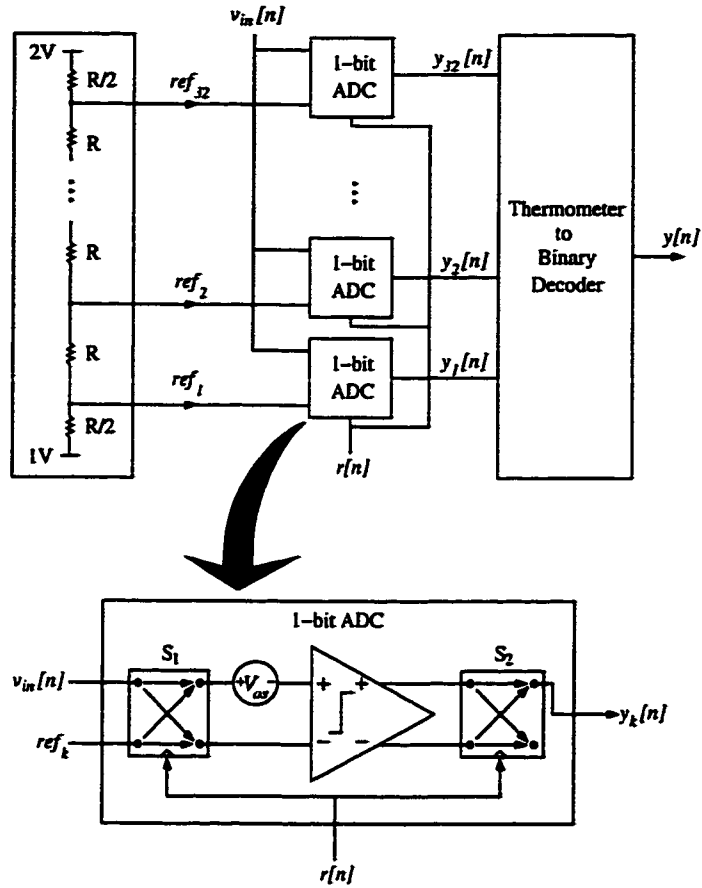
Figure 1.7: Comparator offset DEM implementation.

are typical with the small geometry devices used in the comparators, and the resulting errors in the quantization levels are comparable to the 31.25-mV LSB of the flash ADC. Behavioral simulations confirmed that $\sigma_{V_{os}} = 10$ mV comparator offset errors could limit the SFDR performance of the $\Delta\Sigma$ modulator to below 105 dB. In contrast, 1% resistor mismatches in the reference ladder give rise to quantization level errors on the order of 1 mV. The dominant effect of the comparator offset errors becomes even more pronounced as the number of quantization levels is increased or as the signal swings are reduced. This occurs because the offset errors are fixed and do not scale with the reference voltages as do the errors due to resistor mismatch.

Switched-capacitor offset calibration was not used to overcome this problem be-

cause the large-area metal-metal capacitors required for each of the 64 comparators would significantly increase the size of the flash ADC. Instead, a randomization technique was used to spectrally whiten errors caused by comparator input offsets [22]. This approach is referred to as comparator offset dynamic element matching (DEM) because of its similarity to DEM techniques used in DACs.

Figure 1.7 shows one of the single-ended flash ADCs with comparator offset DEM. The input and output of each comparator in the flash ADC are swapped according to a single-bit random sequence. The swapping is performed by transmission gates arranged such that the sign of each comparator offset is modulated by the random sequence but the polarity of the signal is unaffected. Only one threshold is active in the ADC per sample, so the random sequence only affects one comparator in the ADC per sample. Thus, a single random sequence is sufficient for the entire comparator bank.

It can be shown that comparator offset DEM causes the offset errors to appear as white noise and attenuated spurious components [22]. Though it does not completely whiten spurious tones caused by offset errors, it was verified through simulations that comparator offset DEM along with the attenuation of the noise transfer function was sufficient to achieve better than 105-dB SFDR.

## PSEUDO-RANDOM SEQUENCE GENERATOR

The mismatch-shaping DAC digital encoder and flash ADC require a total of seven single-bit pseudo-random sequences. To avoid introducing periodic artifacts in the 10-Hz – 24-kHz audio band, the sequences must have a repeat rate well below 10 Hz and must be mutually uncorrelated for time shifts up to 100 ms. Though a linear feedback shift register (LFSR) using 19 D flip-flops can generate a single pseudo-random sequence with a period of 170 ms, taking seven adjacent bits

28 D flip-flops
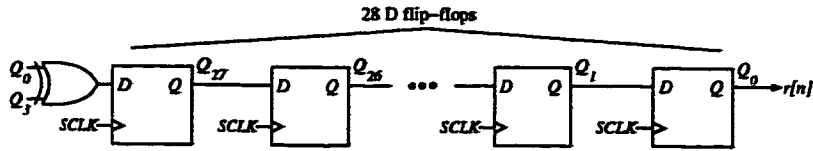
Figure 1.8: A "type-I" LFSR implementing the generator polynomial $1 + x^3 + x^{28}$.
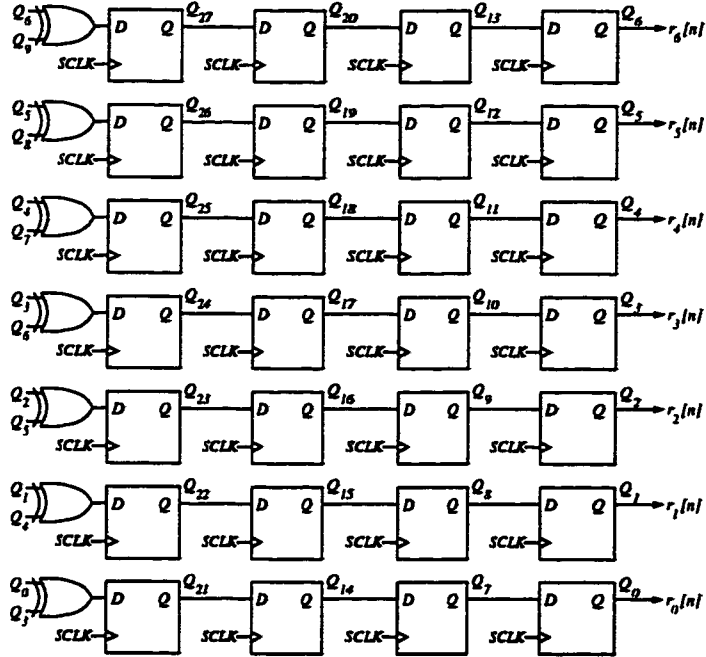
Figure 1.9: The "type-I" LFSR modified to advance from state $n$ to state $n + 7$ on each clock cycle.

from a LFSR will result in signals that are merely delayed versions of each other. Though the correlation can be reduced by using a so-called "type-II" LFSR, this implementation does not provide sufficiently low correlation between the pseudo-random sequences for this application.

Seven separate LFSRs with differing lengths or with carefully chosen initial conditions could be used to provide uncorrelated sequences, but this approach would require on the order of 140 D flip-flops.

Alternatively, the seven uncorrelated sequences could be obtained from a single LFSR clocked seven times per sample period because a single-bit sequence taken from an LFSR approximates a white random sequence. Figure 1.8 shows an example of such a circuit [23]. The increased clock rate implies that the period of each

sequence is reduced by a factor of seven. Thus, a minimum of 22 D flip-flops are necessary to keep the period of each sequence above 100 ms. The drawback to this approach is the requirement for a clock signal at seven times the sample clock.

To circumvent this problem, the state update logic of the circuit in Figure 1.8 can be modified to cause the LFSR to jump from state $n$ to state $n + 7$ on each clock cycle. It follows from Figure 1.8 that $Q_{27}[n + 1] = Q_0[n] \oplus Q_3[n]$. Noting that the shift register connection of the D flip-flops in Figure 1.8 implies $Q_k[n + m] = Q_{k+m}[n]$, for $0 \leq k \leq 27$ and $-k \leq m \leq 27 - k$, the state at time $n + 7$ can be written in terms of the state at time $n$ as follows:

$$Q_k[n + 7] = \begin{cases} Q_{k+7}[n] & 0 \leq k < 21, \\ Q_{k-21}[n] \oplus Q_{k-18}[n] & 21 \leq k \leq 27. \end{cases}$$

The modified circuit, shown in Figure 1.9, implements the state update logic above. Thus, it is logically equivalent to the circuit in Figure 1.8 clocked at seven times the sample rate but avoids the need for a high-rate clock. It generates seven sequences that are uncorrelated for time shifts up to 12.46 seconds using 28 D flip-flops and seven exclusive-or gates. Though the LFSR was implemented off-chip to facilitate experimentation, it requires little hardware and could easily be integrated on-chip.

## III. CIRCUIT IMPLEMENTATION DETAILS

### SWITCHED-CAPACITOR CIRCUITS

The $\Delta\Sigma$ modulator was implemented using delaying, fully-differential, switched-capacitor integrators as shown in Figure 1.10. The use of two delaying integrators decouples their settling behavior and simplifies their design. The 2.8-V peak differential input voltage was chosen to accommodate typical line-level audio signals. The DAC operates with 3.0-V and 0-V references, and the flash ADC uses 2.0-V
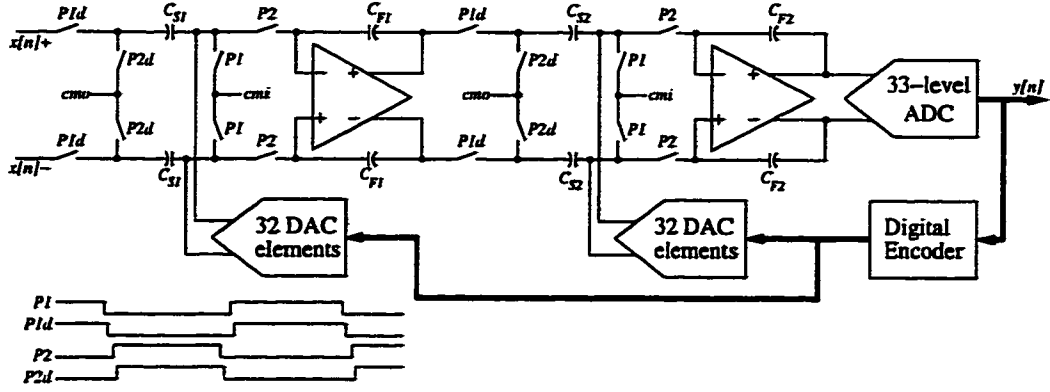
Figure 1.10: The circuit-level $\Delta\Sigma$ modulator topology. $C_{S1} = 4.35$ pF, $C_{F1} = 25.28$ pF, $C_{S2} = 12.64$ pF, and $C_{F2} = 6.53$ pF.
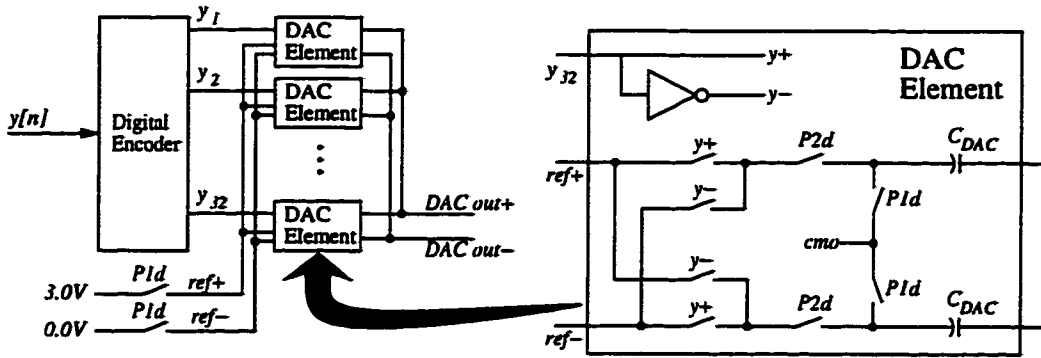


Figure 1.11: The DAC bank circuit topology. $C_{DAC} = 136$ fF.

and 1.0-V references; this choice of reference levels provides an implicit gain of three from the flash ADC input to the DAC output in Figure 1.10.

The output of the mismatch-shaping DAC digital encoder controls both of the 32-element DAC arrays, and each DAC element is implemented as a differential switched-capacitor pair as shown in Figure 1.11. The DAC capacitors are sized such that $32C_{DAC} = C_{S1}$. By discharging the entire array on phase 1 ($P1$) and connecting each DAC element to the references in a normal or an inverted sense on phase 2 ($P2$), the DAC provides 33-level feedback to each integrator. This implementation avoids signal-dependent reference loading that can generate second harmonic distortion. Four transmission gates are required per DAC element, and they are placed on the bottom plate side to keep the summing nodes of the integrator

as small and well-shielded as possible.

It can be shown that the input-referred thermal noise contribution of the first stage DAC and sampling capacitors is,

$$\overline{V}_{th} = \sqrt{\frac{8kT}{C_{S1}M}},$$

where $k$ is Boltzmann's constant, $T$ is temperature in Kelvin, $C_{S1}$ is the sampling capacitance and $M$ is the oversampling ratio. Thus for a 2.8-V peak, differential input and $M = 64$, $C_s = 4.35$ pF is sufficient to achieve a 105-dB signal to thermal noise ratio at 27 C. This implies $C_{DAC} = 136$ fF.

Metal-metal capacitors were chosen over MOSCAPs, since the best SINAD performance reported for MOSCAP-based switched-capacitor circuits to date is below 90 dB [24], [25]. The metal-metal capacitors use a three layer parallel-plate structure with metal 3 and metal 1 forming the parasitic "bottom plate" and metal 2 forming the non-parasitic "top plate". The first stage feedback capacitors and second stage sampling capacitors use 3.16 pF unit capacitors measuring 112 $\mu$m by 369 $\mu$m with a bottom plate parasitic capacitance of 1.62 pF. All other capacitors use a 136 fF unit capacitor measuring 46 $\mu$m by 46 $\mu$m with a bottom plate parasitic capacitance of 126 fF. The 136 fF unit capacitors use a poly layer tied to a quiet 0-V potential as a bottom plate shield, while the 3.16 pF capacitors use an N-well shield. The poly shield was used under the smaller unit capacitors to provide better shielding of the most sensitive nodes at the expense of higher parasitic capacitance, while the N-well shield was used under the feedback and second stage sampling capacitors to reduce their parasitic capacitance.

The integrators use single-stage folded-cascode OTAs with differential gain enhancement [26]. The amplifiers are designed for exponential settling without slew-rate limiting, and the output swing is modest to keep the dc gain relatively constant

over the entire output range. Over temperature, supply, loading, process corners and the 1-V peak differential output range, simulations show that during $P1$ the first integrator has > 118-dB dc gain, > 40.5-MHz unity gain bandwidth and > 57° phase margin and during $P2$ it has > 106-dB dc gain, > 13.9-MHz unity gain bandwidth and > 112° phase margin.

The switch sizes were chosen to allow adequate settling while minimizing distortion and susceptibility to coupled noise. As a result, the on-resistance of the switches limits the settling behavior. The summing node switches were sized small to limit the bandwidth of the sampling networks and to minimize their charge injection. The input transmission gates were sized to provide sufficiently low on-resistance over the entire input signal range.

SPICE transient simulations were used to verify the integrators' settling behavior on $P1$ and $P2$. To verify that incomplete settling did not lead to appreciable distortion, eight SPICE transient simulations of the full $\Delta\Sigma$ modulator were run in parallel for 8192 clock cycles with different initial conditions. These simulations used a combination of transistor-level simulation of the critical switched-capacitor circuits and behavioral modeling of the remaining circuits to reduce simulation time. The 8192-point power spectral density estimate obtained by averaging the periodograms taken from each of these runs verified that the harmonic distortion was better than 100 dB below the 10-kHz full-scale input signal.

Established high-performance switched-capacitor techniques such as delayed bottom plate switching [27] and isolation of analog and digital switching events were used. The digital cells and output pads were designed for modest switching speed to minimize noise generation. The substrate ties for all digital circuits and output drivers were kept separate from the current-bearing $V_{ss}$ lines to re-
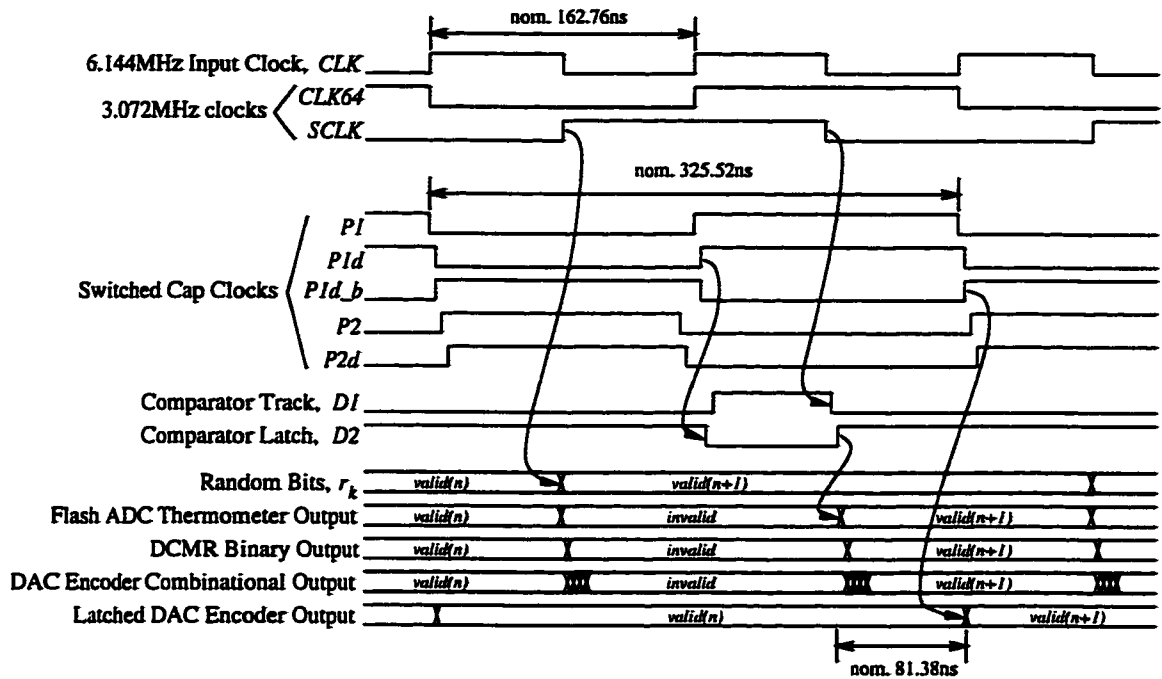
Figure 1.12: Timing diagram for $\Delta\Sigma$ modulator prototype's switched-capacitor circuits and digital logic.

duce noise coupling into the substrate. Four on-chip supply domains were used to isolate the switched-capacitor amplifiers and switches from the switched-capacitor clock generation and switch driver circuits, the flash ADCs and the digital logic. This conservative approach was used because even synchronous, signal-independent switching noise from "clean" circuits such as the non-overlapping clock generator can create distortion when coupled into the input through the signal-dependent on-resistance of the sampling network.

## DIGITAL LOGIC CIRCUITS

The $\Delta\Sigma$ modulator's 6.144-MHz input clock is divided on-chip to produce a pair of 3.072-MHz clock signals. One clock drives the switched-capacitor non-overlapping clock generator to produce $P1$, $P1d$, $P1d\_b$, $P2$, and $P2d$ shown in Figure 1.12. The other clock signal, $SCLK$, updates the state of the pseudo-random sequence generator, the requantizer state machine and the switching blocks.

The switched-capacitor topology in Figure 1.10 and Figure 1.11 implies that the flash ADC pair must sample the second integrator's output at the end of $P1$ and that the switched-capacitor DAC element select lines must be stable by the beginning of the following $P2$ cycle. This was accomplished by sampling the second integrator's output halfway through the $P1$ clock phase as shown in Figure 1.12 to allow the remainder of the $P1$ cycle for digital processing. Because the second integrator is simply holding its output during $P1$, no additional settling error is incurred by sampling at the midpoint rather than at the end of $P1$. The non-overlapping clock generator for the comparators is driven by $P1d \cdot SCLK$, where "$\cdot$" denotes the logical AND operation. Thus, the flash ADCs track during the first half of $P1$ and are latched for the remainder of $P1$ and $P2$.

Once the flash ADCs' comparator outputs are latched, the data path through the thermometer-to-binary decoder, digital common mode rejection, and switching blocks consists only of combinational logic. The combinational output of the mismatch shaping DAC encoder is clocked into a register bank on the rising edge of $P1d\_b$ as shown in Figure 1.12 to provide stable select signals for the switched-capacitor DAC elements. The longest propagation delay observed through the combinational path in simulation under worst case process, temperature and loading conditions was under 50ns. Thus, the digital processing is completed well within the 81ns time window from the time when valid flash ADC data is available to the time of the rising edge of $P1d\_b$.

## IV. PROTOTYPE RESULTS

Reducing analog complexity and capacitor area at the cost of increasing the digital complexity resulted in net area savings. From the floorplan and die photograph shown in Figure 1.13 and the performance summary in Table 1.1, it can be

| Sample Rate | 3.072 MHz |
|---|---|
| Oversampling Ratio | 64 |
| Full-scale input range | ±3.0 V peak differential |
| Peak SINAD | 98.1 dB at 2.8 V, 10 Hz – 24 kHz |
| SFDR | 105 dB, 10 Hz – 24 kHz |
| DR | 99.4 dB, 10 Hz – 24 kHz |
| Power dissipation | 66 mW analog, 2.6 mW digital |
| Technology | 3.3-V, 0.5-$\mu$m CMOS (1 poly, 3 metal) |
| Chip size | 5 mm × 1.9 mm |
| Package | 65 pin PGA |

Table 1.1: Performance and specification summary.



Figure 1.13: Die photograph and layout floorplan.

seen that the area and power are dominated by the switched-capacitor circuits. The capacitor area that would be required to implement a switched-capacitor differential input flash ADC is roughly equal to the DAC array. It can be seen from Figure 1.13 that this capacitor array would have been double the size of the single-ended flash ADC used in this design. The additional digital logic to implement the mismatch-

(a)                                          (b)

Figure 1.14: Power spectral density; 1.5-kHz, 2.8-V peak differential input; (a) 0 Hz - 24 kHz, (b) 0 Hz - 1.536 MHz.

shaping DAC, digital common-mode rejection and comparator DEM occupy only 14% of the total chip area and consume 4% of the total power.

As implemented in the prototype, the digital common mode rejection flash ADC was approximately 13% smaller than the switched-capacitor differential flash ADC described in Section III. Because the area required for digital common mode rejection is dominated by digital logic, improvements in digital layout and reduced device geometries will result in further area savings over the switched-capacitor approach. For example, it is estimated that the area of the DCMR flash ADC can be reduced by logic minimization and improved digital layout to make it 40% smaller than the switched-capacitor flash ADC.

The prototype achieves 98-dB peak SINAD for single tone audio band inputs and 105-dB SFDR for single tone and two tone inputs. These results represent the worst case measured performance for a wide range of single tone and two tone audio band inputs. Figure 1.14 shows the power spectral density for a 2.8-V peak, differential input signal at 1.5 kHz. The third harmonic is 105-dB below the fundamental and limits the $\Delta\Sigma$ modulator's SFDR. The $\Delta\Sigma$ modulator also has excellent small-signal

(a)                                                                    (b)
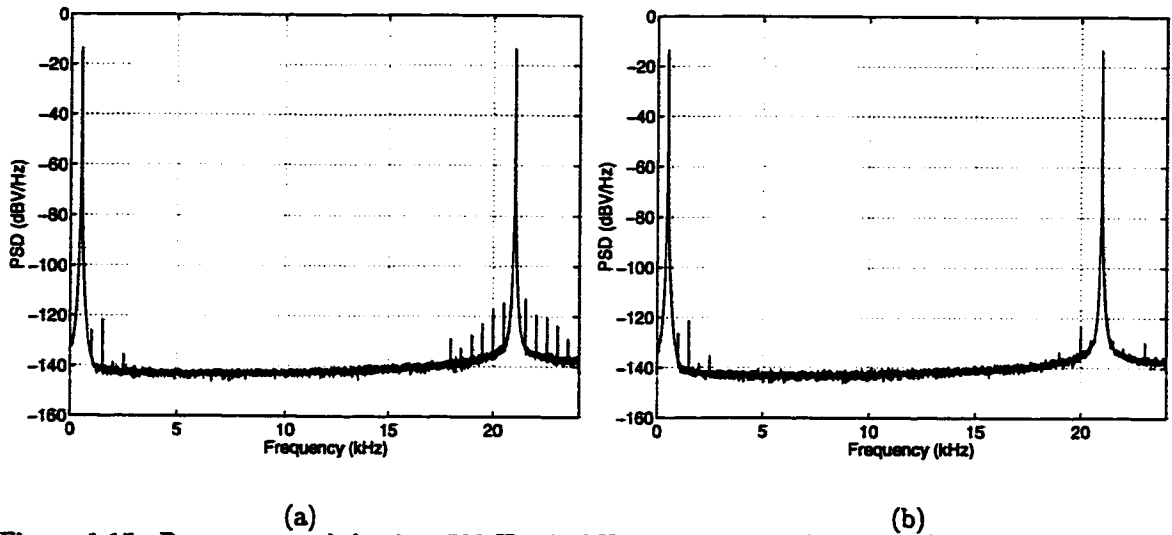
Figure 1.15: Power spectral density; 500-Hz, 21-kHz two-tone, 2.8-V peak differential input; (a) comparator offset DEM disabled, (b) comparator offset DEM enabled.
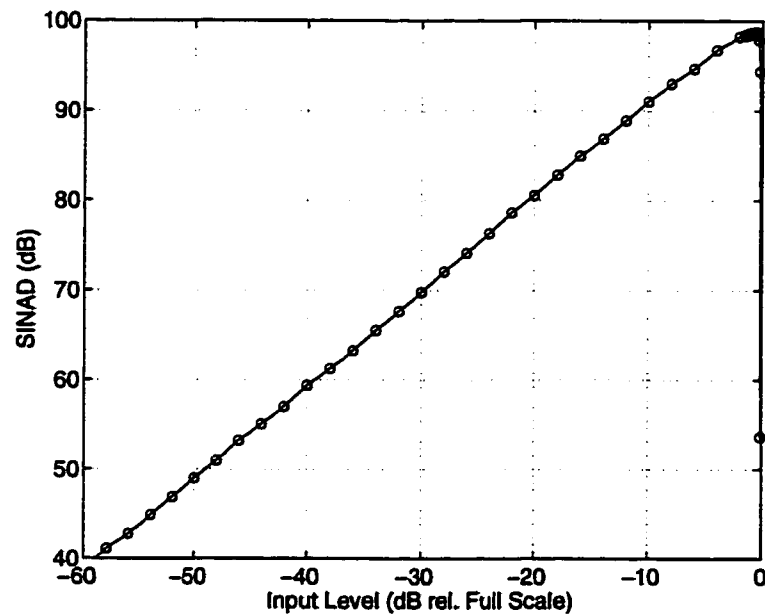


Figure 1.16: 1.5-kHz SINAD versus input level.

performance with a measured dynamic range (DR) of 99.4 dB.

To demonstrate the reduction of spurious tones provided by comparator offset DEM, Figure 1.15 shows the power spectral density with and without DEM for a full-scale, two-tone 500-Hz, 21-kHz input. This two-tone input was chosen

because the intermodulation products near the 24-kHz passband edge receive the least attenuation from the noise transfer function. Therefore, this particular input signal gives a clearer indication of the flash ADC's distortion than a low frequency single-tone test. Figure 1.15a shows the $\Delta\Sigma$ modulator's measured power spectral density with comparator offset DEM disabled. For this input, the inband SFDR is limited to 99 dB by the second order intermodulation product at 21.5 kHz. When comparator offset DEM is enabled, as shown in Figure 1.15b, the SFDR is improved to 108 dB.

Figure 1.16 shows the $\Delta\Sigma$ modulator's SINAD versus input level and demonstrates the large no-overload range of the $\Delta\Sigma$ modulator. The peak SINAD occurs at -0.5 dB relative to the full-scale digital output. Thus, the $\Delta\Sigma$ modulator has an extremely wide usable input range and no gain scaling in the decimation filter is required.

## V. CONCLUSION

The $\Delta\Sigma$ modulator's performance demonstrates that the signal processing innovations used in the design — mismatch-shaping multibit feedback DACs, digital rejection of common-mode noise in the flash ADC, and DEM of comparator offsets — enable the design of high-performance ADCs in a single-poly 3.3-V CMOS process. The design approach used here shifted the design burden away from the switched-capacitor circuits at the expense of increased digital logic complexity and proved to be a successful tradeoff in a fabrication process optimized for digital logic.

## CHAPTER ACKNOWLEDGMENT

primary researcher. Ian Galton supervised the research which forms the basis of the chapter. William Huff and Henrik Jensen assisted in the design and verification of the IC prototype.

## REFERENCES

1. B. H. Leung and S. Sutarja, "Multi-bit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques", *IEEE Trans. Circuits Syst. II*, vol. 39, no. 1, pp. 35-51, Jan. 1992.

2. F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453-460, Apr. 1995.

3. M. J. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent No. 5,138,317, Aug. 11, 1992.

4. H. S. Jackson, "Circuit and method for cancelling nonlinearity error associated with component value mismatches in a data converter," U.S. Patent No. 5,221,926, June 22, 1993.

5. R. T. Baird and T. S. Fiez, "Improved $\Delta\Sigma$ DAC linearity using data weighted averaging," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1 of 3, May 1995, pp. 13-16.

6. R. T. Baird and T. S. Fiez, "Linearity enhancement of multi-bit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II*, vol. 42, no. 12, pp. 753-762, Dec. 1995.

7. R. Schreier and B. Zhang, "Noise-shaped multi-bit D/A converter employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712-1713, Sept. 28, 1995.

8. R. W. Adams and T. W. Kwan, "Data-directed scrambler for multi-bit noise shaping D/A converters", U.S. Patent No. 5,404,142, Apr. 4, 1995.

9. T. W. Kwan, R. W. Adams, and R. Libert, "A stereo multi-bit $\Sigma\Delta$ D/A with asynchronous master-clock interface", in *IEEE ISSCC Dig. Tech. Papers*, vol. 39, Feb. 1996, pp. 226-227.

10. T. W. Kwan, R. W. Adams, and R. Libert, "A stereo multibit sigma delta DAC with asynchronous master-clock interface", *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1881-1887, Dec. 1996.

11. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 10, pp. 808-817, Oct. 1997.

12. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," U.S. Patent No. 5,684,482, Nov 4, 1997.

13. E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3V single-poly CMOS audio ADC delta-sigma modulator with 98dB peak SINAD," in *IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 121-124.

14. S. Rabii and B. A. Wooley, "A 1.8V digital-audio sigma-delta modulator in $0.8\mu$ CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June 1997.

15. E. J. van der Zwan, "A 2.3mW CMOS $\Sigma\Delta$ modulator for audio applications," in *IEEE ISSCC Dig. Tech. Papers* vol. 40, Feb. 1997, pp. 220-221.

16. A. Yasuda, H. Tanimoto, T. Iida, "A 100kHz 9.5mW multi-bit $\Delta\Sigma$ DAC and ADC using noise shaping dynamic elements matching with tree structure," in *IEEE ISSCC Dig. Tech. Papers* vol. 41, Feb. 1998, pp. 64-65.

17. G. Lainey, R. Saintlaurens, and P. Senn, "Switched-capacitor second-order noise-shaping coder," *Electron. Lett.*, vol. 19, pp. 149-150, Feb. 1983.

18. H. T. Jensen and I. Galton, "A reduced-complexity mismatch-shaping DAC for delta-sigma data converters," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1 of 6, June 1998, pp. 504-507.

19. S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 954-961, Dec. 1987.

20. T. Shih, L. Der, S. H. Lewis, and P. J. Hurst, "A fully differential comparator using a switched-capacitor differencing circuit with common-mode rejection," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 250-253, Feb. 1997.

21. E. Fogleman, I. Galton, and H. Jensen, "An area-efficient differential input ADC with digital common mode rejection," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2 of 6, June 1999, pp. 347-350.

22. E. Fogleman, I. Galton, and H. Jensen, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADCs," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2 of 6, June 1999, pp. 290-293.

23. E. J. McCluskey, *Logic Design Principles*, New Jersey: Prentice-Hall, 1986, pp. 457-461.

24. L. Williams III, "An audio DAC with 90dB linearity using MOS to metal-metal charge transfer," in *IEEE ISSCC Dig. Tech. Papers* vol. 41, Feb. 1998, pp. 58-59.

25. H. Yoshizawa, Y. Huang, P. F. Ferguson, Jr., and G. C. Temes, "MOSFET-only switched-capacitor circuits in digital CMOS technology," *IEEE J. Solid-State Circuits,* vol. 34, no. 6, pp. 734-747, June 1999.

26. J. Lloyd and H. S. Lee, "A CMOS opamp with fully-differential gain-enhancement," *IEEE Trans. Circuits Syst. II,* vol. 41, no. 3, pp. 241-243, March 1994.

27. D. G. Haigh and B. Singh, "A switching scheme for switched-capacitor filters which reduces effect of parasitic capacitances associated with control terminals," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 2 of 3, June 1983, pp. 586-589.

# Chapter 2

# An Audio ADC Delta-Sigma Modulator with 100-dB Peak SINAD and 102-dB DR Using a Second-Order Mismatch-Shaping DAC

Eric Fogleman, Jared Welz, Ian Galton

Abstract—A second-order audio ADC $\Delta\Sigma$ modulator using a low-complexity 33-level second-order mismatch-shaping DAC is presented. The DAC encoder is designed to reduce signal-dependent DAC noise modulation. The prototype was implemented in a 3.3-V 0.5-$\mu$m single-poly CMOS process, and it achieves 100-dB SINAD and 102-dB DR.

## I. INTRODUCTION

MULTIBIT $\Delta\Sigma$ modulation has recently been applied to implement high-performance $\Delta\Sigma$ analog-to-digital converters (ADCs) [1]–[3]. A multibit $\Delta\Sigma$ modulator can achieve the same signal to quantization noise ratio as a 1-bit $\Delta\Sigma$ modulator with a lower modulator order and a reduced oversampling ratio. These benefits can be used to relax the performance requirements on the analog switched-capacitor circuitry and enable the implementation of high-performance $\Delta\Sigma$ADCs in digital-optimized CMOS fabrication processes [3]. However, realizing these benefits requires an internal DAC with the same inband precision as the $\Delta\Sigma$ADC.

The development of mismatch-shaping digital-to-analog converters (DACs) has helped make the implementation of multibit $\Delta\Sigma$ADCs practical. While several

mismatch-shaping algorithms have been reported that provide first-order spectral shaping of static DAC mismatch errors [4]–[10], only a few provide second-order mismatch shaping [8]–[11]. Though [8] and [9] show simulated second-order mismatch shaping, detailed hardware-level implementations are not presented.

While second-order mismatch shaping algorithms theoretically offer increased inband precision over first-order algorithms, they present several challenges. The encoder's increased complexity must not outweigh its performance gains. The switching or selection logic, which is based on $\Delta\Sigma$ modulation in [8]–[11], must be stable for real-world input signals. The encoder should minimize spurious tones in the DAC noise and signal-dependent DAC noise modulation because these effects can limit the dynamic range of high-resolution $\Delta\Sigma$ADCs.

This paper presents a second-order audio ADC $\Delta\Sigma$ modulator using a second-order mismatch-shaping DAC encoder based on the tree structure in [10] that addresses these challenges. The prototype $\Delta\Sigma$ modulator uses the analog front end circuitry presented by the authors in [3] with a redesigned mismatch-shaping DAC encoder. The DAC encoder uses an improved version of the second-order sequencing logic simulated in [9]. The modifications presented here reduce its hardware complexity and provide graceful degradation to first-order shaping under overload conditions. The tree-structured encoder employs a modified input layer block to reduce signal-dependent DAC noise modulation and improve SNR for low-level input signals. The prototype $\Delta\Sigma$ modulator is implemented in a standard 0.5-$\mu$m, 3.3-V single-poly CMOS fabrication process. All twelve of the fabricated prototypes achieve 100-dB peak SINAD and 102-dB dynamic range over the 10 Hz – 20 kHz audio band.

Figure 2.1: The switched-capacitor implementation of the $\Delta\Sigma$ modulator.

## II. MISMATCH-SHAPING DAC SIGNAL PROCESSING

The prototype uses the second-order $\Delta\Sigma$ modulator architecture shown in Figure 2.1 with 33-level quantization and feedback. The 33-level mismatch-shaping DAC encoder is based on the tree structure presented in [10]. The five layer binary input tree structure shown in Figure 2.2 drives the 33-level unit element DAC array. The layers of the DAC encoder are labeled 5 through 1; *layer 5* denotes the input layer and *layer 1* denotes the output layer. As shown in Figure 2.2, each layer, $k$, of the encoder has $2^{5-k}$ elements. The nodes in the encoder are referred to as *switching blocks* and are denoted $S_{k,r}$, where $k$ denotes the encoder layer and $r$ denotes the position within the layer. Each switching block has one input, $x_{k,r}[n]$, and two outputs, $x_{k-1,2r}[n]$ and $x_{k-1,2r-1}[n]$.

The *switching sequences*, $s_{k,r}[n]$, are generated within the switching blocks as shown in Figure 2.3 and determine the spectral shaping of the DAC noise. The sequence $d_k[n]$ is an i.i.d. sequence of uniform random variables on $(-1, 1)$. The switching sequences are constrained by the requirements that the encoder's 1-bit outputs must sum to the encoder's input and that $0 \leq x_{k,r}[n] \leq 2^k$. Restricting $s_{k,r}[n] = 0$ for $x_{k,r}[n]$ even and $s_{k,r}[n] = \pm 1$ for $x_{k,r}[n]$ odd is sufficient to meet these requirements. For the tree-structured mismatch-shaping DAC with input $x[n]$ and

Layer 5    Layer 4    Layer 3    Layer 2    Layer 1

Figure 2.2: The 33-level tree-structured mismatch-shaping DAC encoder.

output $y[n]$, it is shown in [10] that $y[n] = \gamma x[n] + \beta + e[n]$, where

$$e[n] = \sum_{k=1}^{5} \sum_{r=1}^{2^{5-k}} \Delta_{k,r} s_{k,r}[n],$$

and $\gamma$, $\beta$, and $\Delta_{k,r}$ are constants which depend only on the static DAC mismatches.

If the switching sequences are all uncorrelated and have the same spectral charac-
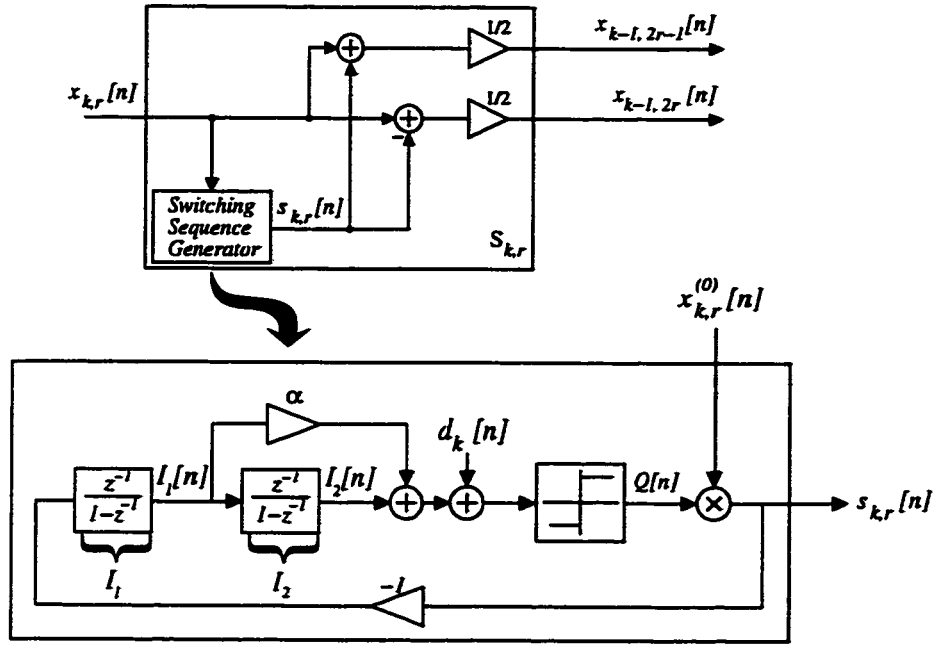
Figure 2.3: Second-order switching block signal processing.

teristics (e.g. second-order spectral shaping), then $e[n]$, referred to as *DAC noise*, will also possess this spectral shaping.

## SECOND-ORDER SWITCHING BLOCK

The signal processing of the second-order switching block is shown in Figure 2.3. This switching sequence generator with feedforward gain $\alpha = 8$ and $d_k[n] = 0$ was used to generate the simulation results shown in [9] though the circuit itself was not published. The switching sequence generator is analogous to a digital $\Delta\Sigma$ modulator with a zero input. The multiplier following the comparator in Figure 2.3 uses $x_{k,r}^{(0)}[n]$, the LSB of $x_{k,r}[n]$, to force $s_{k,r}[n] = 0$ for even $x_{k,r}[n]$.

Unlike the first-order switching blocks in [3] and [10], the second-order switching sequence generator in Figure 2.3 can exhibit instability. For example, if the first integrator's output, $I_1[n]$, is nonzero and a sequence of even inputs occurs, the second integrator's output, $I_2[n]$, will continue to grow in magnitude until an odd input occurs. Unless restrictions are placed on the occurences of even values of
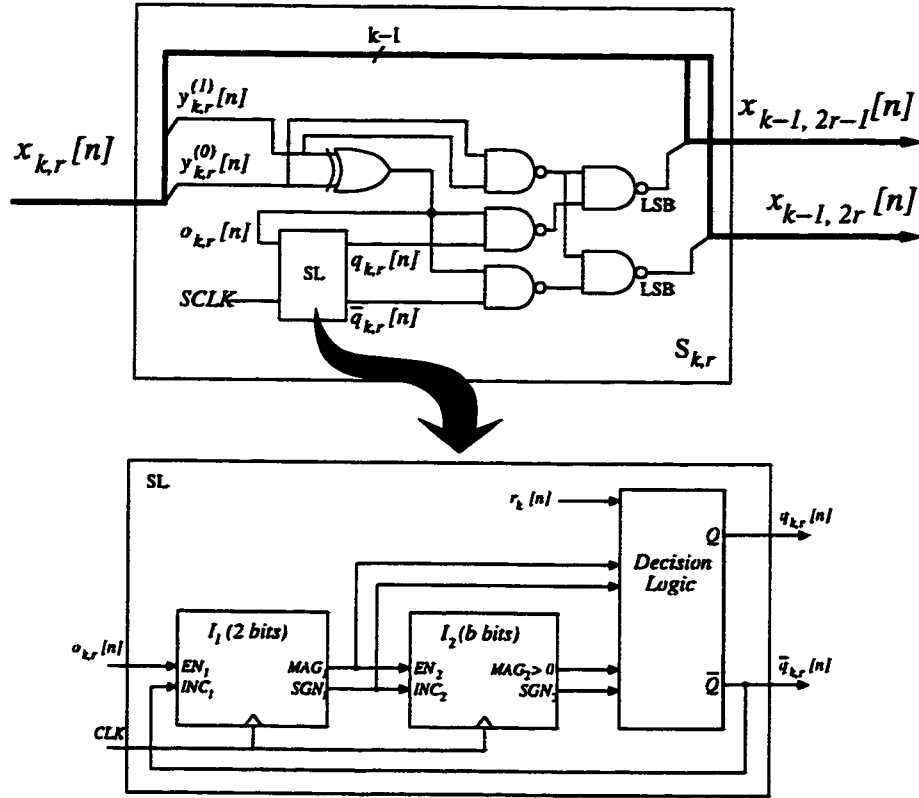
Figure 2.4: Second-order switching block logic-level implementation.

$x_{k,r}[n]$, no bound can be placed on $|I_2[n]|$. Therefore, the number of bits required to represent $I_1[n]$ and $I_2[n]$ depends on the choice of $\alpha$ and the statistics of $x_{k,r}[n]$.

A simplified implementation of the switching sequence generator shown in Figure 2.3 can be obtained by observing that in simulations $s_{k,r}[n]$ retains second-order spectral shaping for values of $\alpha > 8$. Thus, if $|I_1[n]| \leq M$ and $|I_2[n]| \leq M$, a gain of $\alpha > M$ can be implemented by allowing $I_1[n]$ to override $I_2[n]$ whenever $I_1[n]$ is nonzero. The gain element, adders, and comparator in Figure 2.3 can then be replaced by the following decision logic:

$$Q[n] = \begin{cases} +1 & \begin{aligned} &|I_1[n]| > 0 \text{ or} \\ &|I_1[n]| = 0 \ \& \ I_2[n] > 0 \text{ or} \\ &|I_1[n]| = I_2[n] = 0 \ \& \ r_k[n] = 1; \end{aligned} \\ -1 & \begin{aligned} &|I_1[n]| < 0 \text{ or} \\ &|I_1[n]| = 0 \ \& \ I_2[n] < 0 \text{ or} \\ &|I_1[n]| = I_2[n] = 0 \ \& \ r_k[n] = 0, \end{aligned} \end{cases} \tag{1}$$

where $r_k[n]$ is an i.i.d. dither sequence with $P(r_k[n] = 1) = P(r_k[n] = 0) = 1/2$.

For this choice of decision logic, $I_1[n]$ only takes on the values in the set $\{-1, 0, 1\}$, and a two-bit accumulator is sufficient to implement $I_1$. Figure 2.4 shows the simplified second-order switching block incorporating the decision logic in (1) as well as hardware simplifications presented in [3]. The $I_1$ and $I_2$ accumulators are designed such that they saturate at their extreme values rather than "rolling over".

The implementation in (1) ensures that $I_1$ continues to control $s_{k,r}[n]$ when $I_2$ saturates. Thus, in this overload condition, the switching sequence generator degrades to first-order spectral shaping until $I_2$ recovers from saturation. Because of this benign overload behavior, the bit-width of $I_2$ can be reduced at the expense of minor degradation of the spectral shaping near dc. Figure 2.5 shows the DAC noise PSD for various $I_2$ bit widths. This plot shows that even though encoders with four to six bits in $I_2$ do not yield ideal second-order shaping, they still offer significantly better performance than the first-order switching block.

## SIGNAL-DEPENDENT DAC NOISE MODULATION

As implemented in Figure 2.3 and Figure 2.4, $s_{k,r}[n]$ is forced to zero when $x_{k,r}[n]$ is even. As a result, long sequences of even inputs to a switching block will affect the spectral shaping of $s_{k,r}[n]$. Figure 2.6 shows the PSD of a single $s_{k,r}[n]$ sequence where $x_{k,r}^{(0)}[n]$ is a single-bit i.i.d. sequence with $P(x_{k,r}^{(0)}[n] = 1) = p$ and $P(x_{k,r}^{(0)}[n] = 0) = 1 - p$. Increasing the probability of even inputs dramatically changes the inband power of the $s_{k,r}[n]$ sequence. Because the DAC noise, $e[n]$, is the weighted sum of the $s_{k,r}[n]$ sequences, this directly translates to increased inband DAC noise.

For the tree structure of Figure 2.2, input values that are powers of two pose a problem because they propagate even inputs to successive layers of the tree structure. A commonly-encountered input for the 33-level DAC encoder is an input of 16,
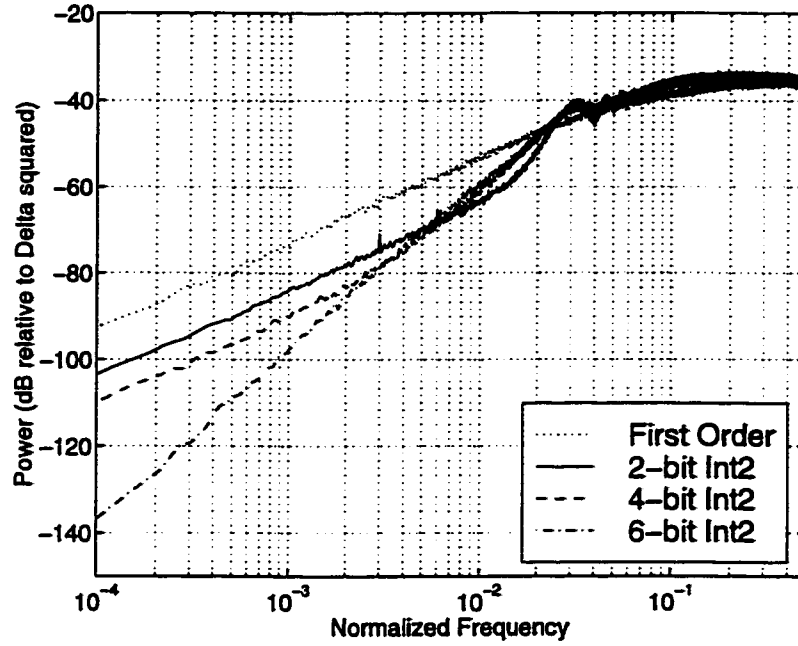
Figure 2.5: Simulated DAC noise PSDs for a 33-level mismatch-shaping DAC; 1st-order and 2nd-order shaping.
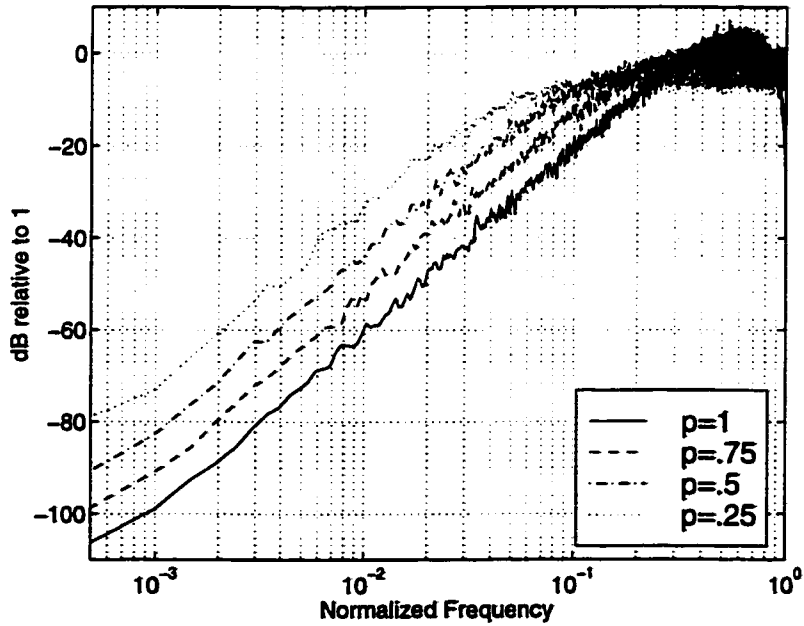


Figure 2.6: Simulated $s_{k,r}[n]$ sequence PSDs versus $P(x_{k,r}$ odd $)$.

the converter's midscale value. An input of 16 is factored into successive even values until the last layer and results in 15 of the 31 $s_{k,r}[n]$ sequences having significantly increased inband power.
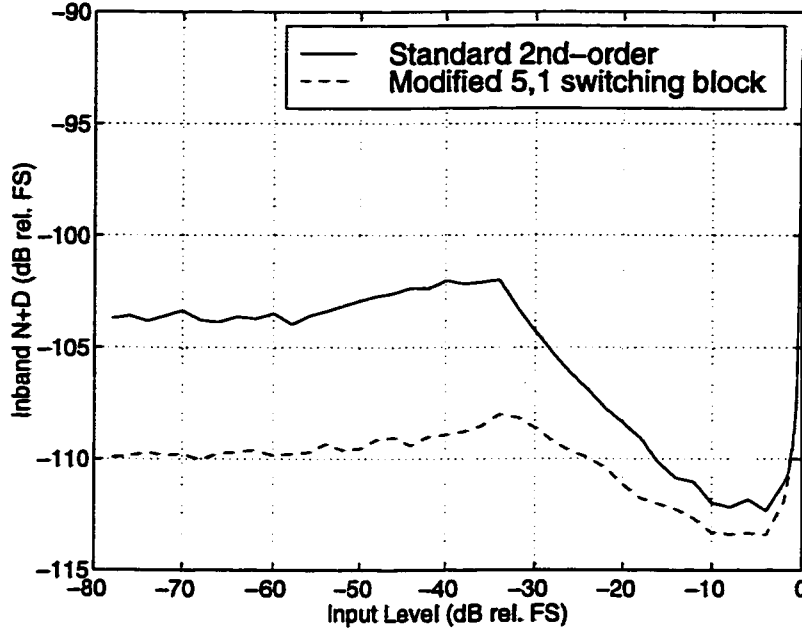
Figure 2.7: Simulated inband noise versus input level for the $\Delta\Sigma$ modulator.

The solid-line plot in Figure 2.7 shows simulated inband noise power versus input level for the $\Delta\Sigma$ modulator of Figure 2.1 using the second-order mismatch-shaping encoder shown in Figure 2.2. The encoder uses the second-order switching blocks shown in Figure 2.4 with 4-bit $I_2$ accumulators. For this implementation, the inband noise power increases by 10 dB as the input drops from full-scale to -35 dB. This is a direct result of the DAC encoder receiving a high density of midscale inputs. Combined with the inband thermal noise and $1/f$ noise, this level of DAC noise modulation would have limited the $\Delta\Sigma$ modulator's dynamic range to 100 dB. Thus, for small input signals, second-order mismatch shaping would yield little or no improvement in SNR over first-order mismatch shaping.

This effect can be mitigated by noting that $s_{k,r}[n] \in \{-1,0,1\}$ is sufficient, but not necessary, to satisfy the requirements that the encoder's output sum to its input value and that $0 \leq x_{k,r}[n] \leq 2^k$. In particular, the $S_{5,1}$ block is free to set $s_{5,1}[n] = \pm 2$ for $x_{5,1}[n] \in \{4,6,8,...28\}$. Thus, when $S_{5,1}$ receives a long run of
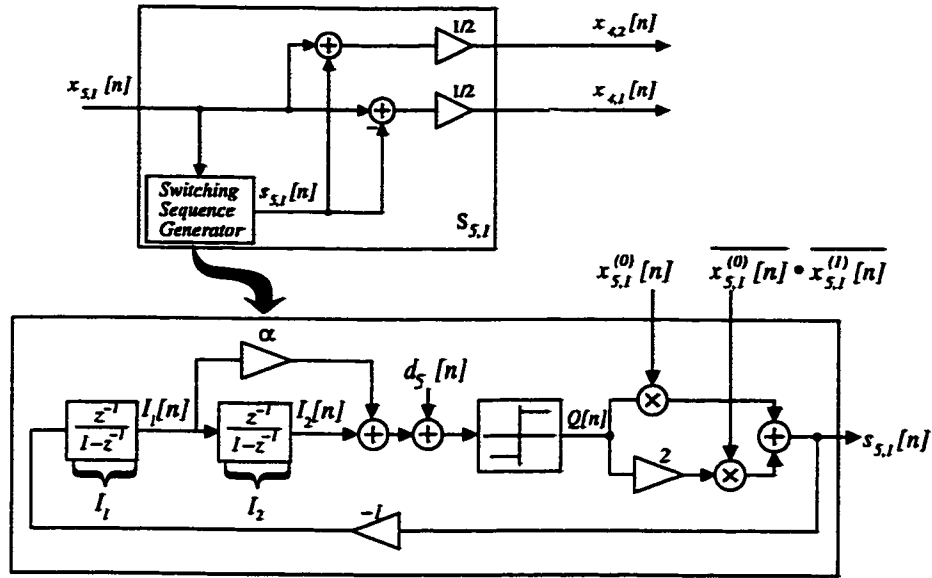
Figure 2.8: Modified $S_{5,1}$ switching block which allows $\pm 1$ feedback for odd inputs and $\pm 2$ feedback for inputs divisible by 4.

input value 16, it can still produce a second-order shaped $s_{5,1}[n]$ taking on values $\pm 2$. The $S_{5,1}$ block breaks the midscale input into output values of 7 and 9 and prevents the propagation of even values to the remainder of the tree structure. The dashed-line plot in Figure 2.7 illustrates the reduction in noise modulation provided by the modified $S_{5,1}$ block. The variation in inband noise is reduced from 10 dB to 5 dB, and the peak inband noise is reduced by 5 dB.

Figure 2.8 shows the $S_{5,1}$ switching sequence generator signal processing. The switching sequence generator produces $s_{5,1}[n] = \pm 1$ for odd $x_{5,1}[n]$ and $s_{5,1}[n] = \pm 2$ for $x_{5,1}[n]$ in the set $\{4, 8, 12, \ldots 28\}$. Though this modification increases the complexity of the $S_{5,1}$ block, the remainder of the tree structure uses the simple switching blocks shown in Figure 2.4. Because $s_{5,1}[n]$ is no longer a 3-level signal, explicit adders must be used to produce the outputs $x_{4,1}[n]$ and $x_{4,2}[n]$. However, simplifications similar to those applied to the switching sequence generator in Figure 2.4 can be used to reduce the complexity of the state machine that produces $s_{5,1}[n]$.
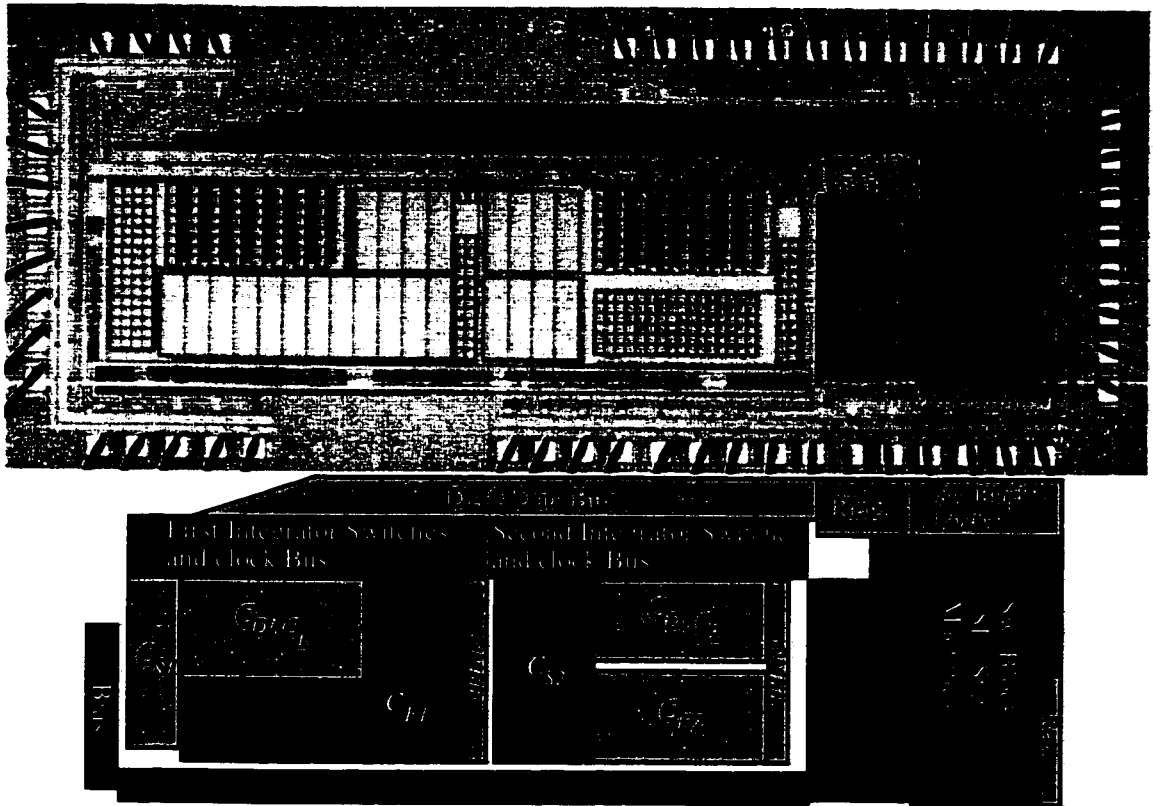
Figure 2.9: Prototype $\Delta\Sigma$ modulator die photograph and layout floorplan.

## III. PROTOTYPE RESULTS

The prototype $\Delta\Sigma$ modulator IC shown in Figure 2.9 was fabricated in a 0.5-$\mu$m, 3.3-V, triple-metal, single-poly CMOS process. The analog front end of the prototype — the switched-capacitor circuitry and flash ADCs with comparator offset DEM and digital common mode rejection (DCMR) — are identical to the audio ADC $\Delta\Sigma$ modulator using a first-order mismatch shaping DAC presented by the authors in [3]. Logic reduction and layout optimization were performed on the DCMR logic to reduce its area. Though the second-order mismatch-shaping DAC encoder with the modified $S_{5,1}$ block is approximately twice the die area of the first-order encoder of [3], the area reduction of the DCMR logic permitted the second-order design to fit in same pad ring as the first-order design.

Each second-order switching block shown in Figure 2.4 required 31 gates, while

| Sample Rate | 3.072 MHz |
| Oversampling Ratio | 64 |
| Full-scale input range | ±3.0 V peak differential |
| Peak SINAD | 100.3 dB at 2.8 V, 10 Hz – 20 kHz |
| SFDR | 105.6 dB, 10 Hz – 20 kHz |
| DR | 102.5 dB, 10 Hz – 20 kHz |
| Power dissipation | 66 mW analog, 4.4 mW digital |
| Technology | 3.3-V, 0.5-$\mu$m CMOS (1 poly, 3 metal) |
| Chip size | 5 mm × 1.9 mm |
| Package | 65 pin PGA |

Table 2.1: Performance and specification summary.

the modified $S_{5,1}$ block in Figure 2.7 required 58 gates. Thus the entire second-order mismatch-shaping DAC encoder was implemented using 988 gates. This is a lower gate count than that reported in [11] for a 9-level second-order mismatch-shaping DAC encoder.

Table 2.1 summarizes the device specifications and worst-case measured performance for the twelve fabricated prototypes. The $\Delta\Sigma$ modulator presented here has 1.5 dB greater peak SINAD and 2.3 dB greater dynamic range (DR) than the design presented [3] with no increase in die area and only a 2.6% increase in power dissipation. Figure 2.10 shows measured 1.5-kHz SINAD versus input level. Figure 2.11 shows the measured inband PSD for -1-dB and -60-dB input signals.

## IV. CONCLUSION

These results demonstrate that a hardware-efficient second-order mismatch-shaping DAC can be implemented to yield improved performance over a first-order design. Using the second-order switching block presented here, pure second-order spectral shaping of the DAC mismatches can be sacrificed to yield substantial hardware savings with minimal impact on performance. The prototype's dynamic range performance shows that the input-layer switching block can be modified to significantly reduce the amount of signal-dependent DAC noise modulation with minimal
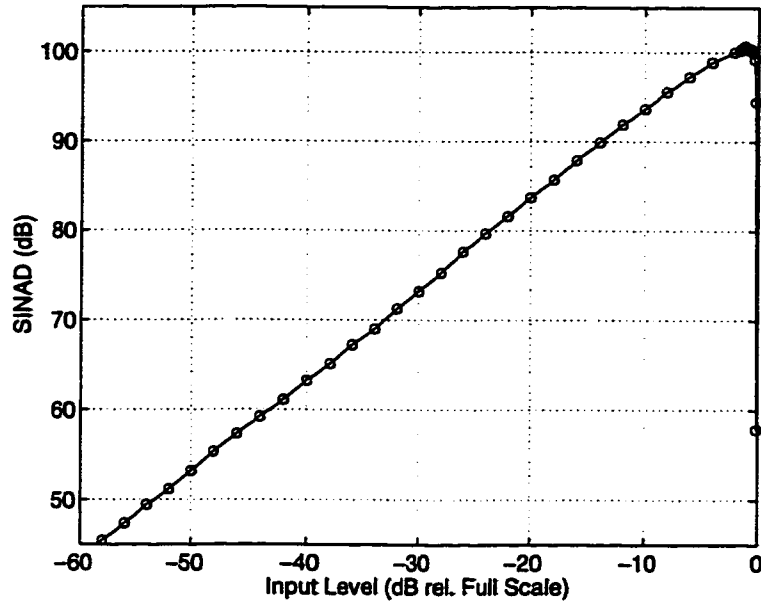
Figure 2.10: Measured SINAD versus input level for the prototype $\Delta\Sigma$ modulator.
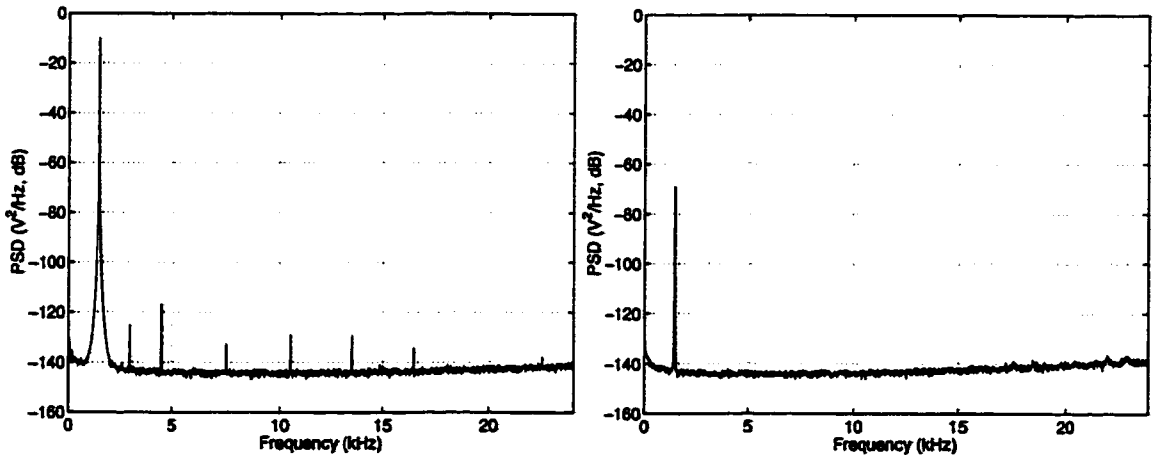


Figure 2.11: Measured inband PSD for -1-dB and -60-dB, 1.5-kHz input signals.

hardware cost.

## CHAPTER ACKNOWLEDGMENT

The text of Chapter 2 consists of material that will appear, in part or in full, as a Regular Paper in the *IEEE Journal of Solid State Circuits*. The dissertation author was the primary researcher. Jared Welz contributed to the architecture of the second-order mismatch-shaping DAC encoder. Ian Galton supervised the

research which forms the basis of the chapter.

## REFERENCES

1. T. Brooks, D. Robertson, D. Kelly, A. DelMuro, and S. Harston, "A 16b sigma-delta pipeline ADC with 2.5MHz output data rate," *IEEE ISSCC Digest of Technical Papers*, vol. 40, Feb. 1997, pp. 209-210.

2. K. Leung, E. Swanson, K. Leung, and S. Zhu, "A 5V, 118dB delta-sigma analog-to-digital converter for wideband digital audio", in *IEEE ISSCC Dig. Tech. Papers*, vol. 40, Feb. 1997, pp. 218-219.

3. E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB peak SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 297-307, March 2000.

4. M. J. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent No. 5,138,317, Aug. 11, 1992.

5. B. H. Leung, S. Sutarja, "Multi-bit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II*, vol. 39, no. 1, pp. 35-51, Jan. 1992.

6. H. S. Jackson, "Circuit and method for cancelling nonlinearity error associated with component value mismatches in a data converter," U.S. Patent No. 5,221,926, June 22, 1993.

7. R. W. Adams, T. W. Kwan, "Data-directed scrambler for multi-bit noise shaping D/A converters", U.S. Patent No. 5,404,142, Apr. 4, 1995.

8. R. Schreier and B. Zhang, "Noise-shaped multi-bit D/A converter employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712-1713, Sept. 28, 1995.

9. A. Keady and C. Lyden, "Tree structure for mismatch noise-shaping multibit DAC," *Electron. Lett.*, vol. 33, no. 17, pp. 1431-1432, Aug. 1997.

10. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 10, pp. 808-817, Oct. 1997.

11. A. Yasuda, H. Tanimoto, and T. Iida, "A third-order delta-sigma modulator using second-order noise-shaping dynamic element matching," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1879-1886, Dec. 1998.

# Chapter 3

# A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta-Sigma ADCs

Eric Fogleman, Ian Galton

Abstract—A multibit $\Delta\Sigma$ analog-to-digital converter can achieve high resolution with a lower order modulator and lower oversampling ratio than a single-bit design. However, in a multibit $\Delta\Sigma$ modulator, quantization level errors in the internal multibit quantizer can limit the $\Delta\Sigma$ modulator's signal-to-noise-and-distortion and spurious-free dynamic range. For a CMOS $\Delta\Sigma$ analog-to-digital converter using a flash analog-to-digital converter as its internal quantizer, comparator input offset errors are a significant source of quantization level errors. This paper presents a dynamic element matching technique, comparator offset DEM, that modulates the sign of the comparator input offsets with a random sequence and causes the offset errors to appear as white noise and attenuated spurious tones. Measured performance of a prototype $\Delta\Sigma$ modulator IC shows that comparator offset DEM enables it to achieve 98-dB peak signal-to-noise-and-distortion and 105-dB spurious-free dynamic range. Analysis and simulation of comparator offset DEM in a flash ADC with a periodic input and uniform dither give insight into its operation and quantify the spur attenuation it provides.

## I. INTRODUCTION

THE development of mismatch-shaping multibit digital-to-analog converters (DACs) has helped to make the implementation of high-performance multibit $\Delta\Sigma$ analog-to-digital converters (ADCs) feasible. A multibit $\Delta\Sigma$ modulator using a

41

mismatch-shaping feedback DAC can achieve the same signal to quantization noise specifications with a lower order modulator and lower oversampling ratio (OSR) than a single-bit design. The use of multibit feedback also relaxes the slew rate and settling time requirements on the analog integrators. While reducing the $\Delta\Sigma$ modulator order and OSR eases the design of the analog front end, it also reduces attenuation of circuit errors in the quantizer. These errors give rise to spurious tones that can limit the $\Delta\Sigma$ADC's signal-to-noise-and-distortion (SINAD) and spurious-free dynamic range (SFDR) performance.

In a flash ADC, the most commonly used quantizer in $\Delta\Sigma$ADCs, quantization level errors stem from the nonideal resistor reference ladder and from comparator input offset errors. Reference ladder errors result from resistor mismatches and scale with the quantization step size. In contrast, CMOS comparator input offsets are dominated by the process's inherent threshold voltage mismatches and become increasingly problematic as the signal swing or the quantization step size are reduced. With the near minimum-size devices required for small-area, high-speed comparators, input offsets with standard deviations on the order of 10 mV are typical. Switched-capacitor offset calibration can address this problem, but it significantly increases die area when a large number of comparators are required and large area metal-metal capacitors are the only available linear capacitor structures.

The technique presented in this paper mitigates the distortion introduced by comparator offsets by modulating the sign of each offset with a random bit sequence. This approach, named *comparator offset DEM* because of its similarity to dynamic element matching (DEM) techniques used in DACs, was developed to address circuit challenges encountered in the design of a high performance multibit ADC $\Delta\Sigma$ modulator [1]. Because of the choice of architecture and the process

limitations, comparator offsets proved to be a barrier to meeting the $\Delta\Sigma$ modulator's 98-dB SINAD and 105-dB SFDR targets. Comparator offset DEM provided a solution to this problem that avoided the use of additional capacitors and enabled the fabricated $\Delta\Sigma$ modulator to meet these aggressive specifications.

The remainder of this paper consists of two main sections and two appendices. Section II presents the implementation and measured performance of Comparator Offset DEM in the prototype $\Delta\Sigma$ADC. Section III presents the signal processing details of the technique. Appendix A and Appendix B give a detailed derivation of the theoretical results presented in Section III.

## II. IMPLEMENTATION IN ADC $\Delta\Sigma$ MODULATOR

The $\Delta\Sigma$ modulator mentioned above is a second order design operating at 3.072 MHz with an OSR of 64. The prototype was fabricated in a 3.3-V, 0.5-$\mu$m single-poly, triple-metal CMOS process, and it achieves 98-dB peak SINAD and 105-dB SFDR [1]. As shown in Figure 3.1, it uses two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC and a 33-level quantizer [2], [3]. The differential input quantizer was realized using a pair of single-ended 33-level flash ADCs and digital subtraction of the outputs to reject common mode noise. Noise-shaped requantization was used to reduce the 65-level difference signal to 33-levels for use in the mismatch-shaping DAC encoder [4].

The topology of a single-ended, 33-level flash ADC is shown in Figure 3.2. It consists of a unit resistor ladder to set the quantization levels and a bank of 1-bit ADCs to compare the input signal to each quantization level. A standard clocked comparator is used to implement each of the 1-bit ADCs. Each comparator's output is equal to one if the input exceeds its reference level and is zero otherwise. The 32 comparator outputs form a thermometer-coded representation of the quantized
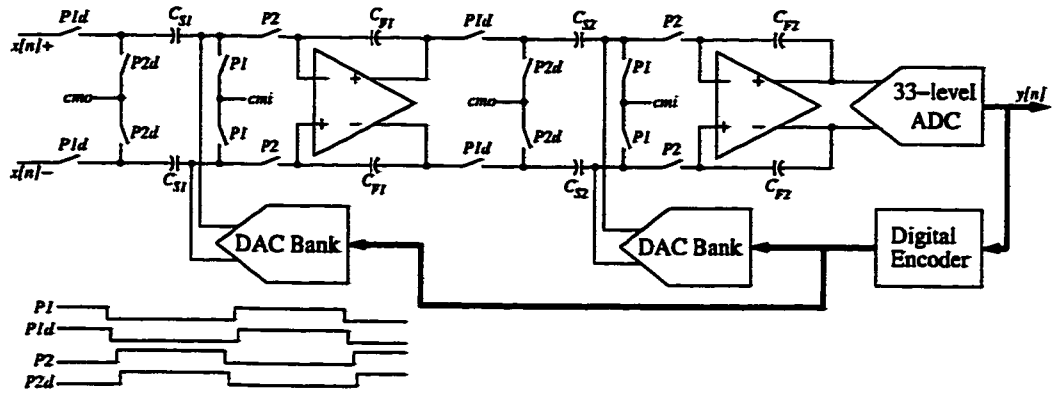
Figure 3.1: $\Delta\Sigma$ modulator circuit topology.
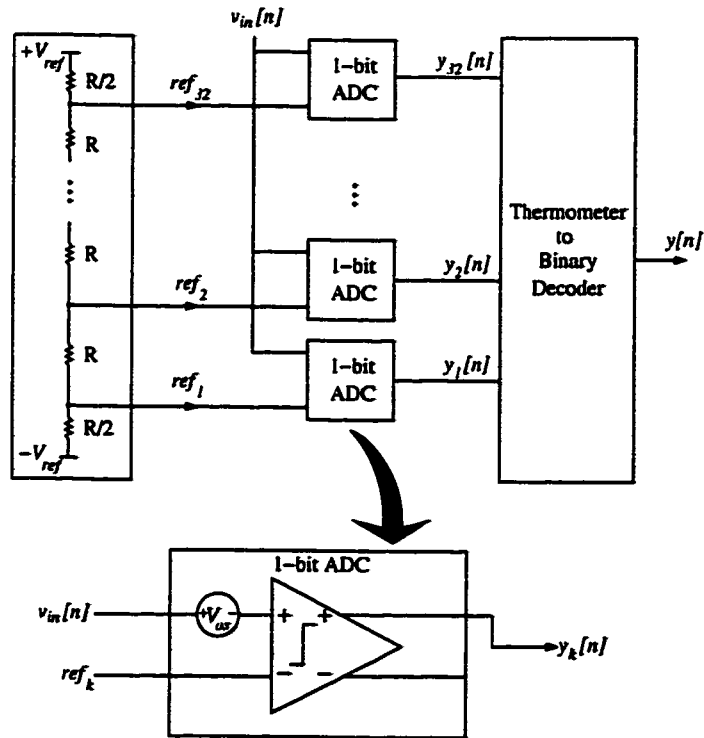


Figure 3.2: Flash ADC circuit topology.

signal. The thermometer to binary decoder in Figure 3.2 is a device that generates a binary representation equal to the number of nonzero 1-bit ADC outputs. As mentioned in the introduction, the major sources of error in the flash ADC are resistor mismatches in the unit resistor ladder and input offset errors in the comparators.

In the prototype, the expected level of device matching and the limited signal

swing implied that comparator input offsets were the dominant error source. The input range of the flash ADCs was set by the integrators' 1.5 V $\pm$ 0.5 V single-ended output swing. For 33-level quantization, the ADCs' nominal step size, $\Delta$, was 31.25 mV and their reference levels, $ref_k$, $k = 1, \ldots, 32$, ranged from 1.0 V + $\frac{\Delta}{2}$ to 2.0 V − $\frac{\Delta}{2}$. Given Gaussian-distributed offsets with a standard deviation of 10 mV, a large percentage of the comparators would be likely to have input offsets comparable to $\Delta$ in magnitude. In contrast, Gaussian-distributed resistor mismatches with a standard deviation of 1% of the unit resistance value would yield reference level errors with standard deviations below 0.9 mV. Behavioral simulations of the $\Delta\Sigma$ modulator with the expected level of comparator offsets indicated that the attenuation provided by the noise transfer function was not sufficient to guarantee meeting the 105-dB SFDR target.

Comparator offset DEM is implemented in the flash ADC using the swapper cells, $S_1$ and $S_2$, at the analog input and digital output of each comparator as shown in Figure 3.3. The control signal $r[n]$ is a 1-bit, $\pm 1$ pseudo-random sequence. When $r[n] = 1$, the direct paths through $S_1$ and $S_2$ are chosen, and

$$y_k[n] = \begin{cases} 1 & v_{in}[n] > ref_k + V_{osk}, \\ 0 & \text{otherwise}, \end{cases}$$

When $r[n] = -1$, the swapped paths through $S_1$ and $S_2$ are chosen, and

$$y_k[n] = \begin{cases} 1 & v_{in}[n] > ref_k - V_{osk}, \\ 0 & \text{otherwise}. \end{cases}$$

Thus, the swapping shown in Figure 3.3 gives rise to two quantization thresholds per comparator selected by the value of the pseudo-random sequence $r[n]$.

The comparator offset DEM circuitry was added to the $\Delta\Sigma$ modulator with minimal increase in die size. Each swapper cell was implemented using four minimum size transmission gates. The 1-bit, pseudo-random sequence was provided by
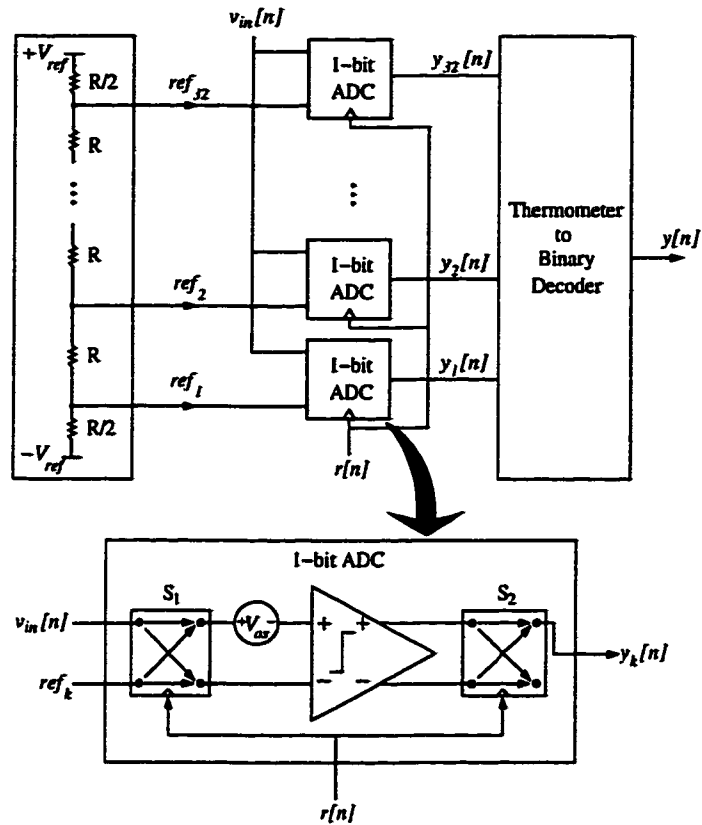
Figure 3.3: Flash ADC with comparator offset DEM.

the $\Delta\Sigma$ modulator's existing sequence generator and required no additional area. The comparator offset DEM hardware occupied only 1.5% of the total chip area and required 65% less area per comparator than the switched-capacitor offset calibration approach considered for the design [5].

Measured results show that comparator offset DEM provides a significant reduction of spurious tones in the $\Delta\Sigma$ modulator output. The $\Delta\Sigma$ modulator was tested with a variety of single-tone and two-tone inputs, and performance with and without DEM was compared by enabling and disabling the random bit. Because the errors due to comparator offsets are attenuated by the quantization noise transfer function, the most dramatic improvement in inband SFDR occurred for two-tone inputs generating spurious components near the 24-kHz passband edge. Table 1 summarizes

| Device | SFDR (dB) DEM off | SFDR (dB) DEM on | Improvement (dB) |
|--------|-------------------|------------------|------------------|
| 1 | 104.7 | 108.4 | 3.7 |
| 2 | 108.2 | 108.3 | 0.1 |
| 3 | 104.6 | 108.4 | 3.8 |
| 4 | 99.3 | 108.4 | 9.1 |
| 5 | 106.6 | 108.6 | 2.0 |
| 6 | 107.4 | 108.2 | 0.8 |

Table 3.1: Measured SFDR performance for full-scale two-tone input signal.



(a)                                    (b)
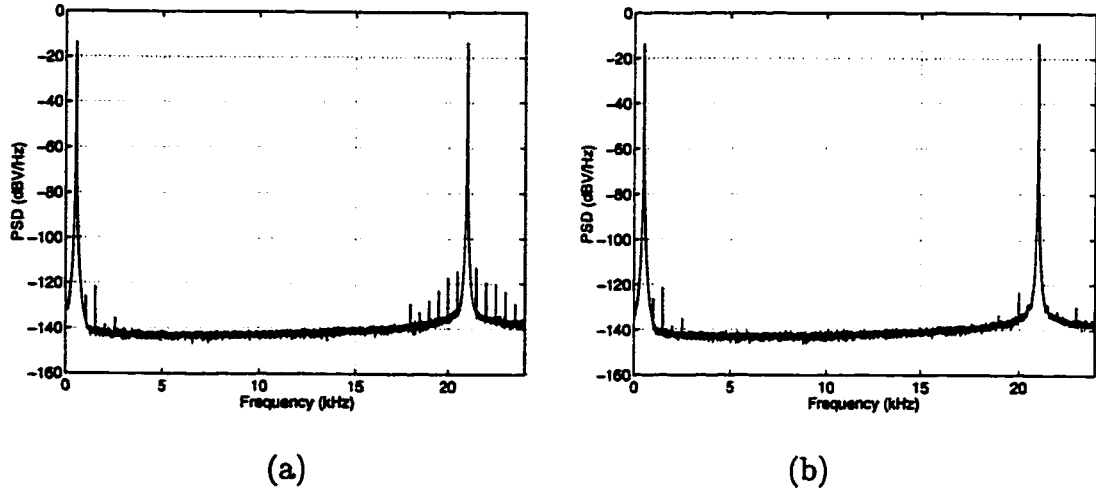
Figure 3.4: Measured $\Delta\Sigma$ modulator results: (a) DEM disabled, (b) DEM enabled.

measured SFDR performance for six randomly-chosen prototype $\Delta\Sigma$ modulators. For this test, the input is a full-scale two-tone signal with components at 500-Hz and 21-kHz. Without comparator offset DEM, the measured SFDR ranged from 99.3 dB to 108.2 dB. Comparator offset DEM improved the SFDR to over 108 dB for all six devices. Figure 3.4 shows the output power spectral density (PSD) for device 4. For this device, comparator offset DEM provided over 15-dB attenuation of the second-order intermodulation products at 20.5 kHz and 21.5 kHz.

## III. COMPARATOR OFFSET DEM SIGNAL PROCESSING DETAILS

Unlike DAC dynamic element matching techniques that fully whiten mismatch errors for arbitrary input signals, comparator offset DEM requires an input with a

random component to achieve a significant reduction in spurious tones. This random component is necessary to make both of each threshold's modulated values affect the output with nearly equal probability. When the flash ADC is used within a multibit $\Delta\Sigma$ modulator having a small amount of input-referred noise, the quantization noise present at the flash ADC's input provides this randomness [6].

To characterize the performance of comparator offset DEM, the (L+1)-level flash ADC of Figure 3.3 is analyzed with a deterministic input, $x[n]$, plus independent, identically distributed (i.i.d.) dither, $w[n]$. By appropriate choice of the dither's probability density function — e.g., uniform over $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ or triangular over $(-\Delta, \Delta)$ — the error due to ideal quantization appears as white noise at the flash ADC's output [7],[8]. As a result, spurious tones at the flash ADC output are due only to misplaced quantization thresholds.

The flash ADC is first analyzed with comparator offset DEM disabled — i.e., $r[n] = 1$ for all $n$ — then with DEM enabled to show the performance improvement relative to a conventional implementation. It is shown that comparator offset DEM causes the offset errors to appear as white noise and attenuated spurious components and that under certain conditions it completely eliminates spurious tones.

## NONIDEAL FLASH ADC MODEL

For analysis, the flash ADC shown in Figure 3.3 is modeled as a memoryless transfer function, $g_y(v_{in}, r)$, where $v_{in}$ is the instantaneous value of the flash ADC input and $r$ is the instantaneous value of the $\pm 1$ random control bit. The flash ADC output sequence, $y[n]$, is then

$$y[n] = g_y(v_{in}[n], r[n]),$$

where $v_{in}[n]$ denotes the flash ADC input sequence and $r[n]$ denotes the $\pm 1$ random control bit sequence.

The ideal resistor ladder shown in Figure 3.3 is driven with reference voltages $+V_{ref}$ and $-V_{ref}$, and the ladder provides quantization thresholds $ref_k = k\Delta - \frac{L+1}{2}\Delta$, $k = 1, 2, \ldots L$, with a quantization step size $\Delta = \frac{2V_{ref}}{L}$. Let $V_{osk}$, $k = 1, 2, \ldots L$, denote the static input offsets of the comparators within the 1-bit ADCs. By defining the unit step function, $u(x)$, as

$$u(x) = \begin{cases} 1 & x > 0, \\ 0 & \text{otherwise,} \end{cases}$$

the transfer function of the $k$th 1-bit ADC can be expressed as

$$g_{y_k}(v_{in}, r) = u(v_{in} - ref_k - r \cdot V_{osk}). \tag{1}$$

The transfer function, $g_y(v_{in}, r)$, is formed by summing the $L$ comparator outputs and adding offset of $-\frac{L}{2}$:

$$g_y(v_{in}, r) = -\frac{L}{2} + \sum_{k=1}^{L} u(v_{in} - ref_k - r \cdot V_{osk}). \tag{2}$$

The $\frac{L}{2}$ offset is added in (2) so $g_y(v_{in}, r)$ will range from $-\frac{L}{2}$ to $\frac{L}{2}$ rather than from 0 to $L$.

In the absence of comparator offsets, (2) is the transfer function of an ideal uniform quantizer. Figure 3.5a shows $g_y(v_{in}, r)$ near $ref_k$ for $r = \pm 1$. The dotted-line graph in Figure 3.5a shows the ideal flash ADC transfer function for $V_{osk} = 0$.

The flash ADC transfer function can be viewed as a linear function plus an error function. Let $\alpha_q = \frac{1}{\Delta}$ denote the quantizer's effective gain, let $g_{e_q}(v_{in})$ denote the transfer function for error due to ideal quantization, and let $g_{e_{os}}(v_{in}, r)$ denote the transfer function for error due to comparator offsets. Thus,

$$g_y(v_{in}, r) = \alpha_q v_{in} + g_{e_q}(v_{in}) + g_{e_{os}}(v_{in}, r), \tag{3}$$

where

$$g_{e_q}(v_{in}) = -\alpha_q v_{in} - \frac{L}{2} + \sum_{k=1}^{N} u(v_{in} - ref_k), \tag{4}$$

and

$$g_{e_{os}}(v_{in}, r) = \sum_{k=1}^{N} u(v_{in} - ref_k - r \cdot V_{osk}) - u(v_{in} - ref_k). \qquad (5)$$

Figure 3.5b shows the total error transfer function, $g_{e_q}(v_{in}) + g_{e_{os}}(v_{in}, r)$, for $r = \pm 1$ with $g_{e_q}(v_{in})$ shown as a dashed-line graph. The comparator offset error transfer function, $g_{e_{os}}(v_{in}, r)$, is shown in Figure 3.5c. It consists of rectangular pulses near each $ref_k$ and is nonzero in the regions where the flash ADC's output differs from that of an ideal quantizer.

Let the flash ADC input sequence be $v_{in}[n] = x[n] + w[n]$, where $x[n]$ is a deterministic input sequence and $w[n]$ is an i.i.d. dither sequence. As above, $x$ and $w$ denote the instantaneous values of the input and dither. Let the characteristic function of $w$, $\Phi_w(u)$, satisfy

$$\Phi_w\left(\frac{2\pi l}{\Delta}\right) = \begin{cases} 1 & l = 0, \\ 0 & l = \pm 1, \pm 2, \ldots \end{cases} \qquad (6)$$

where

$$\Phi_w(u) = \int_{-\infty}^{\infty} f_w(w) e^{juw} dw.$$

Provided that $|v_{in}| < V_{ref}$, the use of i.i.d. dither satisfying (6) — e.g., uniform dither on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ or triangular dither on $(-\Delta, \Delta)$ — implies that $e_q[n]$ is an i.i.d. sequence of random variables independent of $x[n]$ and uniformly distributed on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ [7],[8].

It follows from (3) that the flash ADC output sequence is

$$y[n] = \alpha_q x[n] + \alpha_q w[n] + e_q[n] + e_{os}[n],$$

where $e_q[n] = g_{e_q}(x[n] + w[n])$ and $e_{os}[n] = g_{e_{os}}(x[n] + w[n], r[n])$. It is shown in Appendix B, Claim B13, that the time average power spectral density (PSD) of the flash ADC output is given by

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + \overline{\sigma}^2 + \overline{\mu}\,\delta[m] + S'(e^{j\omega}), \qquad (7)$$
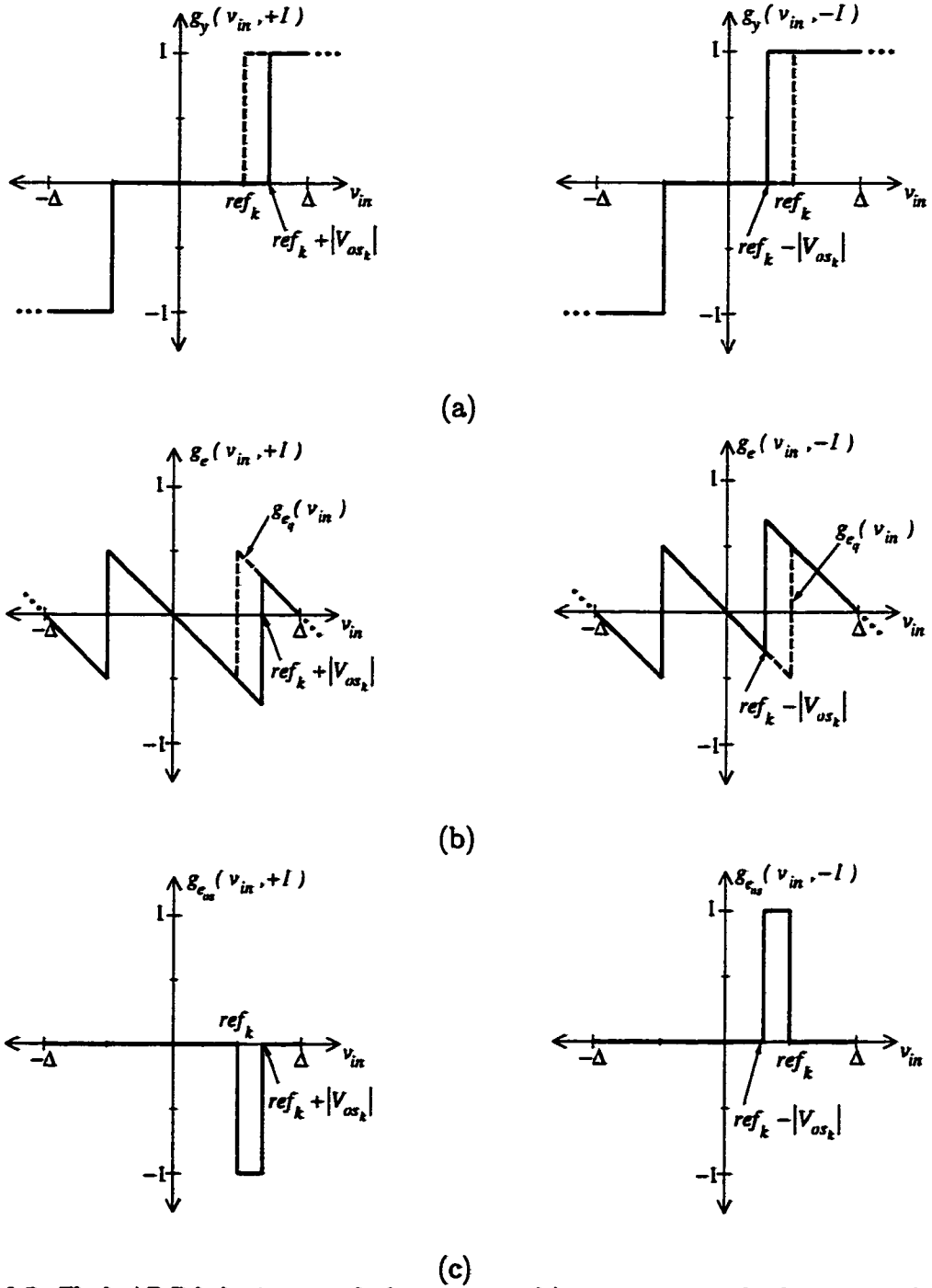
Figure 3.5: Flash ADC behavior at $ref_k$ for $r = \pm 1$: (a) quantizer transfer function, $g_y(v_{in}, r)$; (b) total quantization error, $g_e(v_{in}, r)$ (ideal shown with dashed line); (c) error due to comparator offsets, $g_{e_{os}}(v_{in}, r)$.

where $S_{xx}(e^{j\omega})$ is the time average PSD of the input, $x[n]$, $\sigma^2$ is a white noise term,

and $\bar{\mu}\delta[m]$ is a dc offset term, and

$$S'(e^{j\omega}) = \sum_{m=-\infty}^{\infty} \bar{R}'[m]e^{-j\omega m},\tag{8}$$

where

$$\bar{R}'[m] = \lim_{P\to\infty}\frac{1}{P}\sum_{n=1}^{P}\alpha_q x[n]\mathrm{E}\{e_{os}[n+m]\}+\alpha_q x[n+m]\mathrm{E}\{e_{os}[n]\}+R_{e_{os}e_{os}}[n,m].\tag{9}$$

In (9), $\mathrm{E}\{\cdot\}$ is the statistical expected value, and $R_{e_{os}e_{os}}[n,m] = \mathrm{E}\{e_{os}[n]e_{os}[n+m]\}$ is the statistical autocorrelation of $e_{os}[n]$. Thus, $S'(e^{j\omega})$ represents noise and spurious tones resulting from comparator offsets.

To evaluate (9), an expression for $\mathrm{E}\{e_{os}[n]\}$ is required, where the expectation is taken over the random dither, $w[n]$, and the random sequence, $r[n]$. Because $w[n]$ is independent of $r[n]$, the expectation can be expressed as

$$\mathrm{E}\{e_{os}[n]\} = \mathrm{E}_w\{\mathrm{E}_r\{g_{e_{os}}(x[n]+w,r)\}\},\tag{10}$$

where indices have been dropped on $w$ and $r$ because they are each i.i.d. random sequences.

Let the average offset error as a function of the deterministic input, $x[n]$, be denoted by

$$\bar{g}_{e_{os}}(x) = \mathrm{E}_w\{\mathrm{E}_r\{g_{e_{os}}(x+w,r)\}\}.\tag{11}$$

Thus, $\mathrm{E}\{e_{os}[n]\} = \bar{g}_{e_{os}}(x[n])$. Evaluating the expectation over $w$ in (11) gives

$$\bar{g}_{e_{os}}(x) = \int_{-\infty}^{\infty} \mathrm{E}_r\{g_{e_{os}}(v,r)\}f_w(v-x)dv.\tag{12}$$

Because (12) is in the form of a convolution integral, the transfer function $\bar{g}_{e_{os}}(x)$ can be computed graphically by evaluating $\mathrm{E}_r\{g_{e_{os}}(v,r)\} * f_w(-v)$.

## CONVENTIONAL FLASH ADC

Comparator offset DEM is disabled by setting $r[n] = 1$ for all $n$. For illustration purposes, $w[n]$ is assumed to be uniform dither on $(-\frac{\Delta}{2},\frac{\Delta}{2})$. The error function
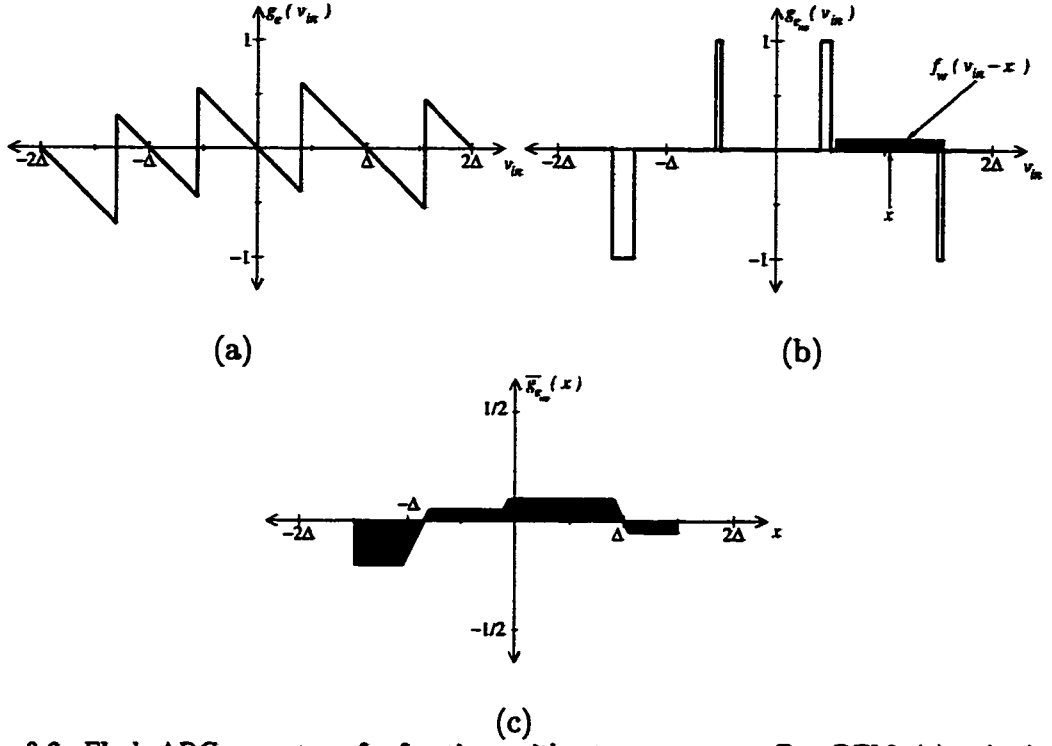
Figure 3.6: Flash ADC error transfer functions without comparator offset DEM: (a) $g_e(v_{in})$, (b) $g_{e_{os}}(v_{in})$, (c) $\bar{g}_{e_{os}}(x)$.

$g_e(v_{in}) = g_{e_{os}}(v_{in}) + g_{e_q}(v_{in})$ and comparator offset error component, $g_{e_{os}}(v_{in})$, are shown in Figure 3.6a and Figure 3.6b, respectively. The shifted dither probability density function, $f_w(v_{in} - x)$, is also shown in Figure 3.6b. Because $r[n] = 1$ for all $n$, $E_r\{e_{os}(v_{in}, r)\} = g_{e_{os}}(v_{in}, 1)$. The transfer function $\bar{g}_{e_{os}}(x)$, shown in Figure 3.6c, has been computed graphically by evaluating $g_{e_{os}}(v, 1) * f_w(-v)$.

As shown in Figure 3.6c, for $|V_{osi}| \neq |V_{osj}| \neq 0$, $\bar{g}_{e_{os}}(x)$ is nonzero for all $x$ except the points where it changes sign. Thus for almost all signals of interest, the sequence $E\{e_{os}[n]\}$ is nonzero, and $S'(e^{j\omega})$ contributes spurious tones to $S_{yy}(e^{j\omega})$. For example, consider an input $x[n]$ with period $N$. The periodicity of $x[n]$ implies that $E\{e_{os}[n + m]\}$ would be periodic in $m$ with period $N$. Therefore, $R'[m]$ would also be periodic in $m$ with period $N$, and its Fourier transform, $S'(e^{j\omega})$, would consist exclusively of spurious tones.
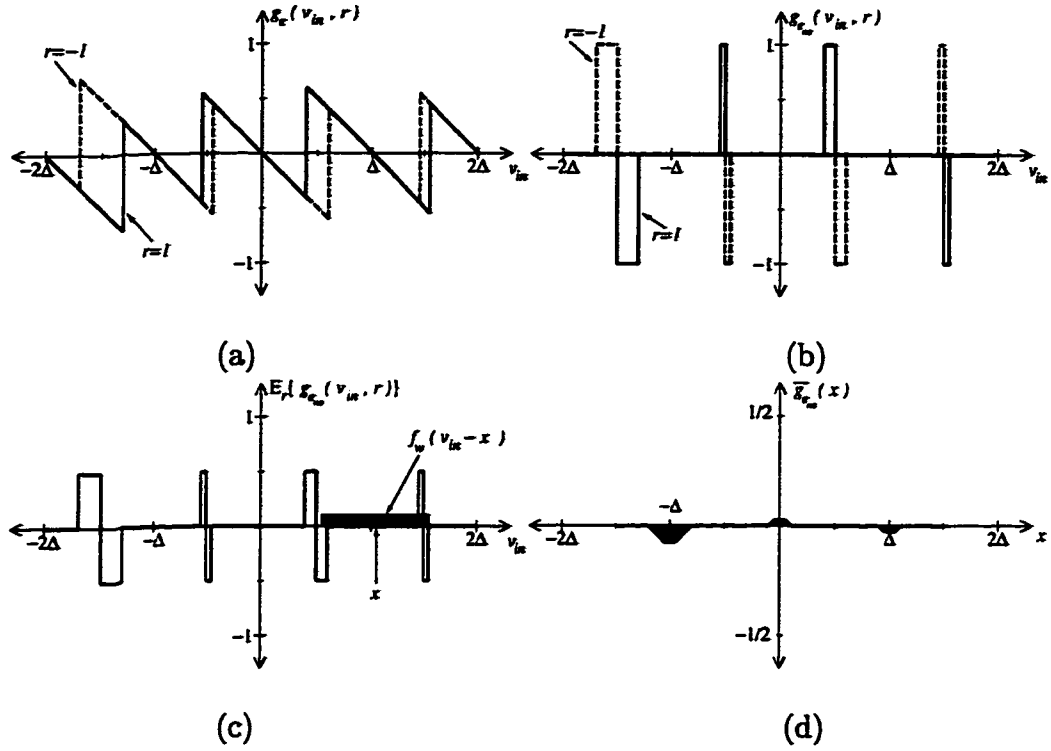
Figure 3.7: Flash ADC error transfer functions with comparator offset DEM: (a) $g_e(v_{in})$, (b) $g_{e_{os}}(v_{in}, r)$, (c) $E_r\{g_{e_{os}}(v_{in}, r)\}$, (d) $\bar{g}_{e_{os}}(x)$.

## FLASH ADC WITH COMPARATOR OFFSET DEM

Comparator offset DEM is enabled by letting $r[n]$ be an i.i.d. random sequence independent of $w[n]$ with $P\{r = 1\} = P\{r = -1\} = \frac{1}{2}$. Thus, the polarity of the comparator offsets are modulated as given by (1). As in the previous case, $w[n]$ is assumed to be uniform dither on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$.

The error transfer functions $g_e(v_{in})$ and $g_{e_{os}}(v_{in}, r)$ for $r = \pm 1$ are shown in Figure 3.7a and Figure 3.7b, respectively. The shifted dither probability density function, $f_w(v_{in} - x)$, is also shown in Figure 3.7b. The transfer function $E_r\{g_{e_{os}}(v_{in}, r)\}$, shown in Figure 3.7c, is obtained by averaging over the two states of $r$.

From $\bar{g}_{e_{os}}(x)$, shown in Figure 3.7d, it can be seen that the key benefit provided by comparator offset DEM is the creation of large zero regions in the $\bar{g}_{e_{os}}(x)$ transfer function by producing equal area positive and negative error regions in $e_{os}$ centered

at each threshold. When $f_w(-v)$ is convolved with $E_r\{g_{e_{os}}(v,r)\}$ as shown in Figure 3.7c, the positive and negative errors cancel each other for much of the flash ADC's input range. The regions where $\bar{g}_{e_{os}}(x) = 0$ correspond to those input values where the dither pdf covers both the positive and negative error regions giving equal probability of positive and negative comparator offset error. The nonzero regions centered between the quantizer thresholds correspond to input values where the dither pdf does not cover both error regions equally and the probabilities of positive and negative errors are unequal.

An input, $x[n]$, that completely avoids the nonzero regions of the transfer function $\bar{g}_{e_{os}}(x)$ has $E\{e_{os}[n]\} = 0$ for all $n$. As shown in Appendix B, Claim B8, $e_{os}[n]$ is a sequence of independent random variables for any deterministic input $x[n]$. Thus,

$$R_{e_{os}e_{os}}[n,m] = \delta[m]E\{e_{os}[n]^2\}.$$

Using this result in (9), it follows that

$$\bar{R}'[m] = \lim_{P\to\infty} \frac{1}{P} \sum_{n=1}^{P} \delta[m]E\{e_{os}[n]^2\} = \delta[m]\bar{R}'[0].$$

Thus, (7) implies

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + \bar{\sigma}^2 + (\bar{\mu} + \bar{R}'[0])\delta[m].$$

Therefore, $S_{yy}(e^{j\omega})$, consists only of a scaled version of the deterministic input signal, a dc component, and white noise. Because $\bar{\sigma}^2$ depends on $e_{os}[n]$, the power of the offset errors is still present in $y[n]$, but comparator offset DEM causes it to appear entirely as white noise.

For an input with some samples in the nonzero regions of $\bar{g}_{e_{os}}(x)$, the offset errors give rise to both white noise and attenuated spurious components in $S_{yy}(e^{j\omega})$. The attenuation of the spurious tones results from the reduction in magnitude of

(a)                                        (b)
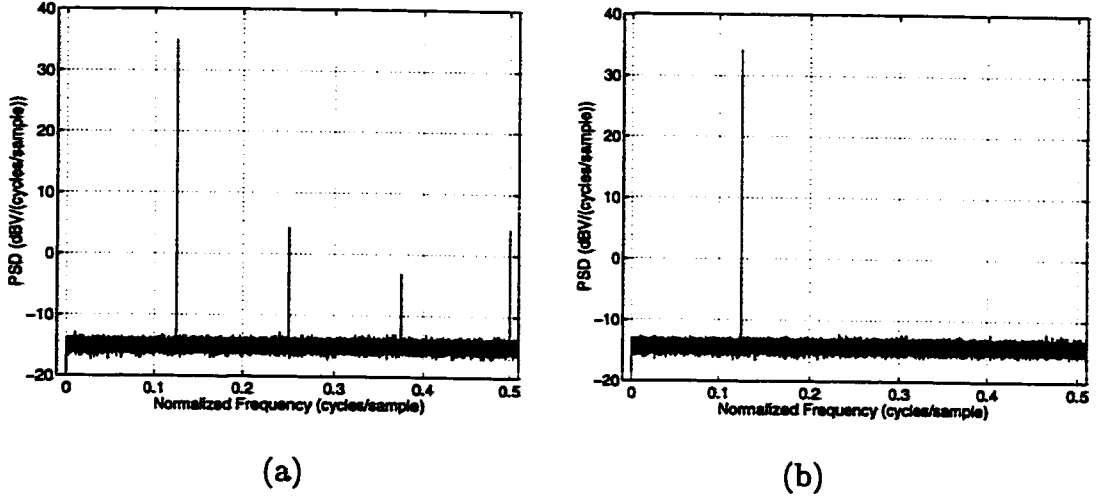
Figure 3.8: Simulation results for 5-level flash ADC with $x[n]$ in $\bar{g}_{e_{os}}(x) = 0$ regions: (a) DEM off, (b) DEM on.

$E\{e_{os}[n]\}$ provided by comparator offset DEM. Simulation results for a wide range of inputs indicate that significant spur attenuation can be achieved in this case.

For input signals falling in the nonzero regions of $\bar{g}_{e_{os}}(x)$ on every sample, there exist offset distributions such that comparator offset DEM provides little reduction of the peak spurious component. However, signals of this type are unlikely to occur in an oversampled converter.

## SIMULATION EXAMPLE

To illustrate the partial and full spur attenuation predicted by the analysis, Figure 3.8 and Figure 3.9 show simulation results for a five-level flash ADC with random errors $|V_{osk}| < \frac{\Delta}{8}$ and uniform i.i.d. dither $w[n]$. In Figure 3.8, the input signal was chosen to be $x[n] = \Delta\sin(\frac{\pi}{4}n) + \frac{\Delta}{8}$. Since the offset errors are bounded by $\frac{\Delta}{8}$, this choice of input forces every sample to land in a region where $\bar{g}_{e_{os}}(x) = 0$ resulting in $E\{e_{os}[n]\} = 0$. The PSD in Figure 3.9b shows that with DEM enabled, no spurs are visible in the output and supports the theoretical result that comparator offset errors are completely whitened.
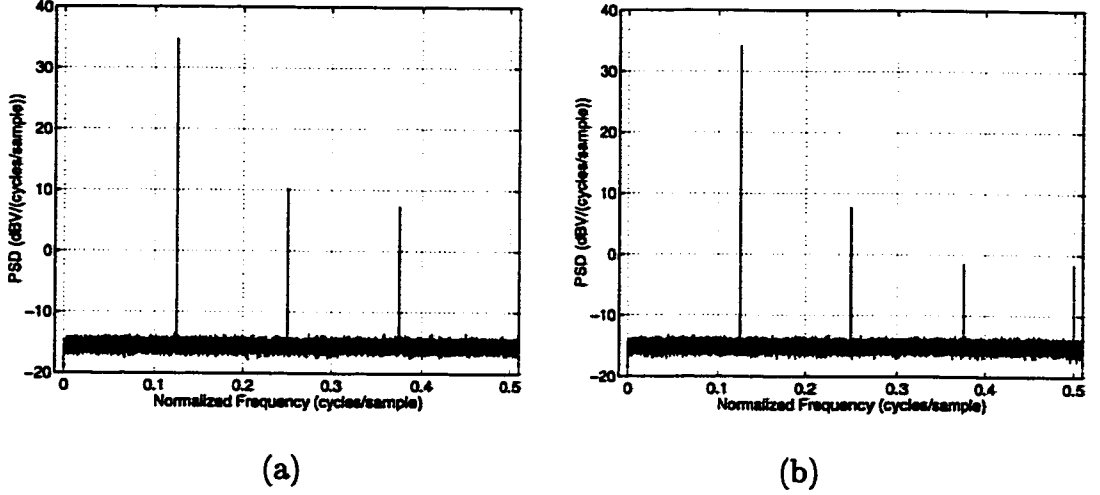
Figure 3.9: Simulation results for 5-level flash ADC with $x[n]$ in $\bar{g}_{e_{os}}(x) \neq 0$ regions: (a) DEM off, (b) DEM on.

The results for the same flash ADC with an input $x[n] = A\sin(\frac{\pi}{4}n)$ are shown in Figure 3.9. This choice of input forces half of its samples to land in the mid-threshold regions where $\bar{g}_{e_{os}}(x) \neq 0$. Without comparator offset DEM, as shown in Figure 3.8a, the flash ADC has an SFDR of 24.4 dB. With DEM enabled as shown in Figure 3.8b, the third harmonic is reduced significantly, but the SFDR is limited to 26.5 dB by the second harmonic. As predicted, the DEM attenuates the spurious tones but does not completely eliminate them.

## IV. CONCLUSION

A comparator offset DEM technique for mitigating the distortion caused by comparator offsets in the flash ADC of a multibit ADC $\Delta\Sigma$ modulator has been presented. Comparator offset DEM was implemented to solve circuit challenges encountered in developing a high performance $\Delta\Sigma$ modulator IC prototype. The DEM technique provided a significant reduction of offset-related spurious tones and enabled the $\Delta\Sigma$ modulator to meet its aggressive SINAD and SFDR targets.

Analysis of comparator offset DEM for deterministic inputs with i.i.d. dither

shows the mechanism by which it attenuates offset-related spurs and describes the conditions under which offset-related spurs are completely whitened. The combination of a random component on the flash ADC's input and random DEM switching creates regions on the quantizer's transfer characteristic where positive and negative quantizer errors occur with equal probability causing the static offset errors to appear as white noise rather than spurious tones. Though the analysis was developed in the context of comparator offsets, the result can be applied without modification to any scheme where two nonideal quantization thresholds are symmetrically modulated around the ideal quantization threshold.

## APPENDIX A

This appendix presents definitions and theorems used in Appendix B to derive the main theoretical results of the paper.

Let the *statistical mean* of a sequence $z[n]$ be defined as

$$\mu_z[n] = \mathrm{E}\{z[n]\},$$

where $\mathrm{E}\{\cdot\}$ denotes the statistical expectation operator. Let the *time average* of $z[n]$ be defined as

$$\overline{M}_z = \lim_{P \to \infty} \frac{1}{P} \sum_{n=0}^{P-1} z[n].$$

Let the *statistical autocorrelation* of $z[n]$ be defined as

$$R_{zz}[n, m] = \mathrm{E}\{z[n]z[n+m]\}, \tag{13}$$

and let the *time average autocorrelation* of $z[n]$ be defined as

$$\overline{R}_{zz}[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} z[n]z[n+m]. \tag{14}$$

Similarly, let the *statistical cross-correlation* of $v[n]$ and $z[n]$ be defined as

$$R_{vz}[n, m] = \mathrm{E}\{v[n]z[n+m]\}, \tag{15}$$

and let the *time average cross-correlation* of $v[n]$ and $z[n]$ be defined as

$$\overline{R}_{vz}[m] = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} v[n]z[n+m].$$  (16)

The *time average power spectral density*, referred to here as the *PSD*, is defined as the Fourier transform of (14):

$$S_{zz}(e^{jw}) = \sum_{m=-\infty}^{\infty} \overline{R}_{zz}[m]e^{-jwm}.$$  (17)

**Theorem A1:** Suppose $w[n]$ and $r[n]$ are sequences of independent random variables. If $g_n(w,r)$ is a sequence of memoryless, deterministic functions, then $z[n] = g_n(w[n], r[n])$ is a sequence of independent random variables.

**Proof:** Fix a positive integer $K$, and for $k = 1, \ldots, K$, choose real numbers $z_k$ and integer indices $n_k$ where $n_i \neq n_j$ for $i \neq j$. Let

$$A_k = \{((w,r) : g_{n_k}(w,r) \le z_k\},$$

for $k = 1, \ldots, K$. Because $w[n]$ and $r[n]$ are independent random sequences, the events

$$\{z[n_k] \le z_k\} = \{(w[n_k], r[n_k]) \in A_k\}$$

are independent for $k = 1, \ldots, K$. Therefore,

$$P\{z[n_1] \le z_1, \ldots, z[n_K] \le z_K\} = P\{z[n_1] \le z_1\} \ldots P\{z[n_K] \le z_K\}.$$

∎

**Theorem A2:** Suppose $w[n]$ and $r[n]$ are sequences of independent random variables. If $g_n(w,r)$ and $h_n(w,r)$ are sequences of memoryless, deterministic functions then the random variables $z[n] = g_n(w[n], r[n])$ and $v[n+m] = h_n(w[n+m], r[n+m])$ are independent for all integers $n$ and for all integers $m \neq 0$.

**Proof:** Fix an integer $n$, a nonzero integer $m$, and real numbers $z$ and $v$. Let

$$A = \{(w,r) : g_n(w,r) \leq z\}$$

and

$$B = \{(w,r) : h_{n+m}(w,r) \leq v\}$$

Because $w[n]$ and $r[n]$ are independent random sequences, the events

$$\{z[n] \leq z\} = \{(w[n], r[n]) \in A\}$$

and

$$\{v[n+m] \leq v\} = \{(w[n+m], r[n+m]) \in B\}.$$

are independent. Therefore,

$$P\{z[n] \leq z, v[n+m] \leq v\} = P\{z[n] \leq z\}P\{v[n+m] \leq v\}.$$

∎

**Theorem A3:** Given $z[n]$, a sequence of independent random variables, suppose there exists a positive real number $A$ such that $P\{|z[n]| < A\} = 1$ for all $n$. If $\overline{M}_z$ exists, then

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} E\{z[n]\} = \overline{M}_z$$

with probability 1.

**Proof:** Note that for all $n$,

$$0 \leq \text{Var}(z[n]) \leq E\{z[n]^2\} \leq E\{A^2\} = A^2.$$

Thus,

$$0 \leq \sum_{n=1}^{\infty} \frac{\text{Var}(z[n])}{n^2} < A^2 \sum_{n=1}^{\infty} \frac{1}{n^2} < \infty. \tag{18}$$

Given that $z[n]$ is independent, the Kolmogorov Criterion states that (18) is sufficient for $z[n]$ to obey the Strong Law of Large Numbers [9]:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (z[n] - \mathrm{E}\{z[n]\}) = 0$$

with probability 1. Because $\overline{M}_z$ exists,

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E}\{z[n]\} = \overline{M}_z$$

with probability 1.

■

**Lemma A:** If $z[n]$ is a sequence of independent random variables, then for all integers $m$ and for $p = 0, 1, \ldots, |m|$,

$$r_p[n] = z[n(|m| + 1) - p]z[n(|m| + 1) - p + m]$$

is a sequence of independent random variables.

**Proof:** First consider $m = 0$. Because $z[n]$ is independent, $r_0[n] = z[n]^2$ is independent by Theorem A1. (Let $g_n(z, r) = z^2$.)

Now consider $m \neq 0$. Fix $p \in \{0, 1, \ldots, |m|\}$. Fix a positive integer $K$, and for $k = 1, \ldots, K$ choose real numbers $\rho_k$ and integers $n_k$ where $n_i \neq n_j$ for $i \neq j$. To show that the events

$$\{r_p[n_k] \leq \rho_k\} = \{z[n_k(|m| + 1) - p]z[n_k(|m| + 1) - p + m] \leq \rho_k\}$$

are independent for $k = 1, \ldots, K$ it is sufficient to show that the indices are unique.

For $m = 0$, $n_i \neq n_j$ immediately implies $n_i(|m| + 1) - p \neq n_j(|m| + 1) - p$.

Now consider $m \neq 0$. Suppose for the sake of contradiction that $n_i(|m|+1)-p = n_j(|m| + 1) - p + m$. This would imply

$$n_i = n_j + \frac{m}{|m| + 1}.$$

This is a contradiction because $n_i$ and $n_j$ are integers and $m \neq 0$. Therefore, the independence of $z[n]$ and the uniqueness of the indices imply

$$P\{r_p[n_1] \leq \rho_1, \ldots, r_p[n_K] \leq \rho_K\} = P\{r_p[n_1]\} \ldots P\{r_p[n_K]\}.$$

∎

**Theorem A4:** Given, $z[n]$, a sequence of independent random variables, suppose there exists a positive real number $A$ such that $P\{|z[n]| < A\} = 1$ for all $n$. If $\overline{R}_{zz}[m]$ exists, then

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{zz}[n, m] = \overline{R}_{zz}[m]$$

with probability 1.

**Proof:** To prove the result, the sequence $z[n]z[n + m]$ is decomposed into a finite collection of infinite, independent random sequences which satisfy the Kolmogorov Criterion and therefore obey the Strong Law of Large Numbers. Summing over the finite collection completes the proof.

Fix an integer $m$. Let $p = 0, \ldots, |m|$. For each $p$, define the subsequence

$$r_p[n] = z[n(|m| + 1) - p]z[n(|m| + 1) - p + m].$$

By Lemma A, $r_p[n]$ is an independent random sequence. Note that

$$0 \leq E\{r_p[n]^2\} = E\{z[n(|m| + 1) - p]^2\}E\{z[n(|m| + 1) - p + m]^2\} < A^4,$$

and

$$0 \leq |E\{r_p[n]\}| = |E\{z[n(|m| + 1) - p]^2\}||E\{z[n(|m| + 1) - p + m]^2\}| < A^2.$$

Thus, $0 \leq \text{Var}(r_p[n]) < A^4$ and

$$0 \leq \sum_{n=1}^{\infty} \frac{\text{Var}(r_p[n])}{n^2} < A^4 \sum_{n=1}^{\infty} \frac{1}{n^2} < \infty. \tag{19}$$

Given that for each $p$, $r_p[n]$ is an independent random sequence, the Kolmogorov Criterion states that (19) is sufficient to show that $r_p[n]$ obeys the Strong Law of Large Numbers [9]:

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (r_p[n] - E\{r_p[n]\}) = 0, \quad p = 0, \ldots, |m| \tag{20}$$

with probability 1. Summing the $|m| + 1$ infinite sums in (20) gives

$$\lim_{P \to \infty} \frac{1}{P} \sum_{p=0}^{|m|} \sum_{n=1}^{P} (r_p[n] - E\{r_p[n]\}) = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} (z[n]z[n+m] - R_{zz}[n,m]) = 0,$$

with probability 1. Because $\overline{R}_{zz}[m]$ exists,

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{zz}[n,m] = \overline{R}_{zz}[m]$$

with probability 1.

■

## APPENDIX B

This appendix presents the derivation of the main theoretical results of the paper. An $(L+1)$-level flash ADC, as shown in Figure 3.3, is considered. The ideal resistor ladder is driven with reference voltages $+V_{ref}$ and $-V_{ref}$, and the ladder provides quantization thresholds $ref_k = k\Delta - \frac{L+1}{2}\Delta$, $k = 1, 2, \ldots L$ with a quantization step size $\Delta = \frac{2V_{ref}}{L}$. Each of the $L$ 1-bit ADCs within the flash ADC has an input offset error, $V_{osk}$, $k = 1, 2, \ldots L$.

Let $e(v_{in}, r) = g_{e_q}(v_{in}) + g_{e_{os}}(v_{in}, r)$ be the total error introduced by the flash ADC as a function of the input, where $e_q(v_{in})$ is the error due to ideal $(L+1)$-level quantization and $e_{os}(v_{in}, r)$ is the error due to 1-bit ADC input offset errors, and $r \in \{-1, 1\}$ is the comparator offset DEM control signal. For the conventional flash ADC, let $r[n] = 1$, and for a flash ADC with comparator offset DEM, let $r[n]$ be an i.i.d. sequence of random variables with $P\{r = -1\} = P\{r = 1\} = \frac{1}{2}$.

Let $\alpha_q = \frac{1}{\Delta}$ denote the effective gain of the flash ADC. Thus, the flash ADC output, $y[n]$, is given by

$$y[n] = \alpha_q v_{in}[n] + e[n], \tag{21}$$

where

$$e[n] = e_q[n] + e_{os}[n] = g_{e_q}(v_{in}[n]) + g_{e_{os}}(v_{in}[n], r[n]). \tag{22}$$

Let the flash ADC input be $v_{in}[n] = x[n] + w[n]$, where $x[n]$ is a deterministic input signal and $w[n]$ is a *dither signal*. It is assumed that $x[n]$ and $w[n]$ are bounded such that $v_{in}[n]$ is within the no-overload range of the quantizer. Let $w[n]$ be an i.i.d. sequence of random variables with with $\mu_w = E\{w[n]\}$ and $\sigma_w^2 = E\{w[n]^2\} - \mu_w^2$ for all $n$. Let the characteristic function of $w$, $\Phi_w(u)$, satisfy the following condition:

$$\Phi_w\left(\frac{2\pi l}{\Delta}\right) = \begin{cases} 1 & l = 0, \\ 0 & l = \pm 1, \pm 2, \ldots \end{cases} \tag{23}$$

where

$$\Phi_w(u) = \int_{-\infty}^{\infty} f_w(w) e^{juw} dw.$$

Provided that $|v_{in}| < V_{ref}$, the use of i.i.d. dither satisfying (6) — e.g., uniform dither on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ or triangular dither on $(-\Delta, \Delta)$ — implies that $e_q[n]$ is an i.i.d. sequence of random variables independent of $x[n]$ and uniformly distributed on $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ [7],[8].

From (21), the autocorrelation of the flash ADC output is

$$R_{yy}[n, m] = E\left\{ (\alpha_q v_{in}[n] + e[n])(\alpha_q v_{in}[n + m] + e[n + m]) \right\}. \tag{24}$$

Expanding $R_{yy}[n, m]$ into its component terms and expressing the expectations as as autocorrelations and cross-correlations give

$$R_{yy}[n, m] = \alpha_q^2 R_{v_{in}v_{in}}[n, m] + \alpha_q R_{v_{in}e}[n, m] + \alpha_q R_{ev_{in}}[n, m] + R_{ee}[n, m]. \tag{25}$$

Claims B1–B4 which follow derive expressions for the each of the terms on the right-hand side of (25).

**Claim B1:**

$$R_{v_{in}v_{in}}[n,m] = x[n]x[n+m] + \mu_w x[n] + \mu_w x[n+m] + \mu_w^2 + \delta[m]\sigma_w^2, \qquad (26)$$

where

$$\delta[m] = \begin{cases} 1 & m = 0, \\ 0 & \text{otherwise.} \end{cases}$$

**Proof:** Expanding $R_{v_{in}v_{in}}[n,m]$ into its component terms and noting that $x[n]$ is deterministic gives

$$R_{v_{in}v_{in}}[n,m] = x[n]x[n+m] + \mu_w x[n] + \mu_w x[n+m] + E\{w[n]w[n+m]\}. \qquad (27)$$

Because $w[n]$ is i.i.d., $E\{w[n]w[n+m]\} = \mu_w^2 + \delta[m]\sigma_w^2$. Substituting this result into (27) completes the proof.

■

**Claim B2:**

$$R_{v_{in}e}[n,m] = x[n]E\{e_{os}[n+m]\} + \mu_w E\{e_{os}[n+m]\}$$
$$+ \delta[m]\left(R_{we_q}[n,0] + R_{we_{os}}[n,0] - \mu_w E\{e_{os}[n]\}\right). \qquad (28)$$

**Proof:** Expanding $R_{v_{in}e}[n,m]$ into its component terms and noting that $x[n]$ is deterministic gives

$$R_{v_{in}e}[n,m] = x[n]E\{e_q[n+m]\} + x[n]E\{e_{os}[n+m]\}$$
$$+ E\{w[n]e_q[n+m]\} + E\{w[n]e_{os}[n+m]\}. \qquad (29)$$

The first term is zero because $e_q[n]$ is independent of $x[n]$ for all $n$ and has zero mean. By letting $g_n(w, r) = w$ and $h_n(w, r) = g_{e_q}(x[n] + w)$ in Theorem A2, it follows that $w[n]$ and $e_q[n+m]$ are independent for $m \neq 0$. Noting that $e_q[n]$ is has zero mean gives

$$E\{w[n]e_q[n + m]\} = \delta[m]E\{w[n]e_q[n]\}. \tag{30}$$

By letting $g_n(w, r) = w$ and $h_n(w, r) = g_{e_{os}}(x[n] + w, r)$, it follows from Theorem A2 that $w[n]$ and $e_{os}[n + m]$ are independent for $m \neq 0$ and

$$E\{w[n]e_{os}[n + m]\} = \mu_w E\{e_{os}[n + m]\} + \delta[m]\left(E\{w[n]e_{os}[n]\} - \mu_w E\{e_{os}[n]\}\right). \tag{31}$$

Substituting (30) and (31) into (29), expressing the expectations as correlations, and combining the $\delta[m]$ terms complete the proof.

∎

**Claim B3:**

$$R_{ev_{in}}[n, m] = x[n + m]E\{e_{os}[n]\} + \mu_w E\{e_{os}[n]\}$$
$$+ \delta[m]\left(R_{we_q}[n, 0] + R_{we_{os}}[n, 0] - \mu_w E\{e_{os}[n]\}\right). \tag{32}$$

**Proof:** Because $R_{ev_{in}}[n, m] = E\{e[n]v_{in}[n + m]\}$, this result follows from (28) by letting $n' = n + m$ and $m' = -m$ and by noting that $m' = 0$ when $\delta[m'] = 1$.

∎

**Claim B4:**

$$R_{ee}[n, m] = R_{e_{os}e_{os}}[n, m] + \delta[m]\left(E\{e_q^2\} + 2R_{e_q e_{os}}[n, 0]\right). \tag{33}$$

**Proof:** Expanding $R_{ee}[n, m]$ into its component terms gives

$$R_{ee}[n, m] = E\{e_q[n]e_q[n+m]\} + E\{e_q[n]e_{os}[n+m]\}$$

$$+ E\{e_{os}[n]e_q[n+m]\} + E\{e_{os}[n]e_{os}[n+m]\}. \tag{34}$$

Because $e_q[n]$ is i.i.d. and has zero mean, it follows that

$$E\{e_q[n]e_q[n+m]\} = \delta[m]E\{e_q^2\}. \tag{35}$$

Note that the $n$ index has been dropped in (35). By letting $g_n(w, r) = g_{e_q}(x[n]+w)$ and $h_n(w, r) = g_{e_{os}}(x[n]+w, r)$, it follows from Theorem A2 that $e_q[n]$ and $e_{os}[n+m]$ are independent for $m \neq 0$ and thus

$$E\{e_q[n]e_{os}[n+m]\} = \delta[m]E\{e_q[n]e_{os}[n]\}. \tag{36}$$

Substituting (35) and (36) into (34), expressing the expectations as correlations, and combining the $\delta[m]$ terms complete the proof.

∎

Claim B5 uses the results of Claims B1–B5 to derive an expression for (25).

**Claim B5:**

$$R_{yy}[n, m] = \alpha_q^2 x[n]x[n+m] + R'[n, m] + \delta[m]\sigma^2[n] + \mu[n, m], \tag{37}$$

where,

$$R'[n, m] = \alpha_q x[n]E\{e_{os}[n+m]\} + \alpha_q x[n+m]E\{e_{os}[n]\} + R_{e_{os}e_{os}}[n, m], \tag{38}$$

$$\sigma^2[n] = \alpha_q^2 \sigma_w^2 + 2\alpha_q R_{we_q}[n, 0] + 2\alpha_q R_{we_{os}}[n, 0]$$

$$- 2\alpha_q \mu_w E\{e_{os}[n]\} + E\{e_q^2\} + 2R_{e_q e_{os}}[n, 0], \tag{39}$$

and

$$\mu[n, m] = \alpha_q^2 \mu_w x[n] + \alpha_q^2 \mu_w x[n+m] + \alpha_q^2 \mu_w^2$$

$$+ \alpha_q \mu_w E\{e_{os}[n]\} + \alpha_q \mu_w E\{e_{os}[n+m]\}. \tag{40}$$

**Proof:** The results of Claims 1-4 — (26), (28), (32), and (33) — are applied to the terms of (25). The $\delta[m]$ terms are combined to form $\sigma^2[n]$. The terms dependent on $n$ and $m$ are combined to form $R'[n,m]$. The remaining terms other than $x[n]x[n+m]$ form $\mu[n,m]$.

■

In Claims B6–B12 which follow, it is shown that the time average means and autocorrelations converge to their ensemble values. As stated previously, it is assumed that $x[n]$ and $w[n]$ are bounded to prevent the flash ADC from overloading. Specifically, there exist real numbers $X$ and $W$ such that $|x[n]| < X$ and $P\{|w[n]| < W\} = 1$ for all $n$. By definition, $P\{|e_q[n]| \le \frac{1}{2}\} = 1$, $P\{|e_{os}[n]| \le 1\} = 1$, and $P\{|y[n]| \le \frac{L}{2}\} = 1$.

**Claim B6:**

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{yy}[n,m] = \overline{R}_{yy}[m]. \tag{41}$$

**Proof:** To show that $y[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w,r) = x[n] + w + g_{e_q}(x[n] + w) + g_{e_{os}}(x[n] + w, r).$$

Theorem A1 implies $y[n]$ is a sequence of independent random variables. Because $y[n]$ is bounded and independent, the claim follows from Theorem A4.

■

**Claim B7:**

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n] E\{e_{os}[n+m]\} = \overline{R}_{xe_{os}}[m], \tag{42}$$

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n+m] \mathrm{E}\{e_{os}[n]\} = \overline{R}_{e_{os}x}[m]. \tag{43}$$

**Proof:** Consider (42) for a fixed value of $m$, and note that $x[n]$ is a deterministic sequence. Define a new random sequence $z[n] = x[n]e_{os}[n+m]$. To show that $z[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_{os}}(x[n+m] + w, r).$$

Theorem A1 implies $z[n]$ is independent. Because $x[n]$ and $e_{os}[n]$ are bounded, $P\{|z[n]| \le X\} = 1$. By Theorem A3,

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n] \mathrm{E}\{e_{os}[n+m]\} = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} x[n]e_{os}[n+m] = \overline{R}_{xe_{os}}[m].$$

Thus (42) holds. The equality in (43) follows by the same reasoning with $z[n] = x[n+m]e_{os}[n]$.

■

**Claim B8:**

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{e_{os}e_{os}}[n, m] = \overline{R}_{e_{os}e_{os}}[m].$$

**Proof:** To show that $e_{os}[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = g_{e_{os}}(x[n] + w, r).$$

Theorem A1 implies $e_{os}[n]$ is independent. Because $e_{os}[n]$ is bounded, the claim follows from Theorem A4.

■

**Claim B9:**

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{we_q}[n, 0] = \overline{R}_{we_q}[0].$$

**Proof:** Define a new random sequence $z[n] = w[n]e_q[n]$. To show that $z[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_q}(x[n + m] + w).$$

Theorem A1 implies $z[n]$ is independent. Because $w[n]$ and $e_q[n]$ are bounded, $P\{|z[n]| \leq \frac{W}{2}\} = 1$. By Theorem A3,

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E}\{w[n]e_q[n]\} = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} w[n]e_q[n] = \overline{R}_{we_q}[0].$$

∎

**Claim B10:**

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} R_{we_{os}}[n, 0] = \overline{R}_{we_{os}}[0].$$

**Proof:** Define a new random sequence $z[n] = w[n]e_{os}[n]$. To show that $z[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w, r) = x[n]g_{e_{os}}(x[n + m] + w, r).$$

Theorem A1 implies $z[n]$ is independent. Because $w[n]$ and $e_{os}[n]$ are bounded, $P\{|z[n]| \leq W\} = 1$. By Theorem A3,

$$\lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} \mathrm{E}\{w[n]e_{os}[n]\} = \lim_{P \to \infty} \frac{1}{P} \sum_{n=1}^{P} w[n]e_{os}[n] = \overline{R}_{we_{os}}[0].$$

∎

**Claim B11:**

$$\lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} \mathrm{E}\{e_{os}[n]\} = \overline{M}_{e_{os}}.$$

**Proof:** As shown in Claim B8, $e_{os}[n]$ is independent and bounded. The claim then follows from Theorem A3.

∎

**Claim B12:**

$$\lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} R_{e_q e_{os}}[n,0] = \overline{R}_{e_q e_{os}}[0].$$

**Proof:** Define a new random sequence $z[n] = e_q[n]e_{os}[n]$. To show that $z[n]$ satisfies the hypotheses of Theorem A1, let

$$g_n(w,r) = g_{e_q}(x[n]+w)g_{e_{os}}(x[n]+w,r),$$

Theorem A1 implies $z[n]$ is independent. Because $e_q[n]$ and $e_{os}[n]$ are bounded, $P\{|z[n]| \le 1\} = 1$. By Theorem A3,

$$\lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} \mathrm{E}\{e_q[n]e_{os}[n]\} = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} e_q[n]e_{os}[n] = \overline{R}_{e_q e_{os}}[0].$$

∎

Given the results of the preceding claims, the main theoretical results of the paper can now be stated.

**Claim B13:** The autocorrelation of the flash ADC output is given by

$$\overline{R}_{yy}[m] = \alpha_q^2 \overline{R}_{xx}[m] + \overline{R}'[m] + \overline{\sigma}^2\delta[m] + \overline{\mu}, \tag{44}$$

where

$$\overline{R}'[m] = \alpha_q \overline{R}_{xe_{os}}[m] + \alpha_q \overline{R}_{e_{os}x}[m] + \overline{R}_{e_{os}e_{os}}[m], \tag{45}$$

$$\overline{\sigma}^2 = \alpha_q^2 \sigma_w^2 + 2\alpha_q \overline{R}_{we_q}[0] + 2\alpha_q \overline{R}_{we_{os}}[0] - 2\alpha_q \mu_w \overline{M}_{e_{os}} + \mathrm{E}\{e_q^2\} + 2\overline{R}_{e_q e_{os}}[0], \tag{46}$$

and

$$\overline{\mu} = 2\alpha_q^2 \mu_w \overline{M}_x + \alpha_q^2 \mu_w^2 + 2\alpha_q^2 \mu_w \overline{M}_{e_{os}}. \tag{47}$$

The PSD of the flash ADC output is given by

$$S_{yy}(e^{j\omega}) = \alpha_q^2 S_{xx}(e^{j\omega}) + S'(e^{j\omega}) + \overline{\sigma}^2 + \overline{\mu}\,\delta(e^{j\omega}), \tag{48}$$

where

$$S'(e^{j\omega}) = \sum_{m=-\infty}^{\infty} \overline{R}'[m] e^{-j\omega m}. \tag{49}$$

**Proof:** Taking time averages of (37)–(40), using the results of Claims B6 through B12, and combining terms yields (44)–(47). The PSD results in (48) and (49) follow from the definition in (17) by taking the Fourier transform of each of the terms in (44).

∎

## CHAPTER ACKNOWLEDGMENT

The text of Chapter 3 consists of material that will appear, in part or in full, as a Regular Paper in the *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*. The dissertation author was the primary researcher. Ian Galton supervised the research which forms the basis of the chapter.

## REFERENCES

1. E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB peak SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 297-307, March 2000.

2. G. Lainey, R. Saintlaurens, and P. Senn, "Switched-capacitor second-order noise-shaping coder," *Electron. Lett.*, vol. 19, pp. 149-150, Feb. 1983.

3. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 10, pp. 808-817, Oct. 1997.

4. E. Fogleman, I. Galton, and H. Jensen, "An area-efficient differential input ADC with digital common mode rejection," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2 of 6, June 1999, pp. 347-350.

5. R. Gregorian, *Introduction to CMOS OP-AMPs and Comparators*, New York, NY: John Wiley & Sons, 1999, pp. 198-199.

6. I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inform. Theory*, vol. 40, no. 3, pp. 848-859, May 1994.

7. L. Schuchman, "Dither signals and their effects on quantization noise," *IEEE Trans. Commun. Technol.*, vol. COM-12, pp. 162-165, Dec. 1964.

8. A. B. Sripad and D. L. Snyder, "A necessary and sufficient condition for quantization errors to be uniform and white," *IEEE Trans. Acoust. Speech Signal Processing*, vol. ASSP-25, pp. 442-448, Oct. 1977.

9. W. Feller, *An Introduction to Probability Theory and Its Applications*, vol. I, 3rd ed. New York: Wiley, 1950.

# Chapter 4

# A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion

Eric Fogleman, Ian Galton

Abstract—A multibit $\Delta\Sigma$ analog-to-digital converter can achieve high resolution with a lower order $\Delta\Sigma$ modulator and lower oversampling ratio than a single-bit design, but it requires a multibit internal flash analog-to-digital converter rather than a simple comparator. In an implementation with a fully-differential analog front end, the flash analog-to-digital converter must quantize a differential voltage relative to a set of differential reference voltages. Though analog techniques for differential analog-to-digital conversion exist, implementing them in a low-voltage, single-poly CMOS process is a challenging circuit design problem. This paper presents a digital common-mode rejection technique for differential analog-to-digital conversion which avoids the circuit complexity and die area requirements of analog common-mode rejection techniques. This technique was used to implement the internal quantizer in two high-performance, single-poly CMOS ADC $\Delta\Sigma$ modulator prototypes with over 98-dB peak signal-to-noise-and-distortion and 105-dB spurious-free-dynamic-range. Implementation details, die area requirements, and measured common-mode rejection are presented for the prototype. Signal processing details of digital common-mode rejection within the $\Delta\Sigma$ modulator are presented showing that injected common-mode noise results only in modulation of the quantization error power and does not create spurious tones.

## I. INTRODUCTION

THE development of mismatch-shaping multibit digital-to-analog converters (DACs) has helped make the implementation of high-resolution multibit $\Delta\Sigma$

analog-to-digital converters (ADCs) feasible. Compared to a single-bit design, a multibit $\Delta\Sigma$ADC can achieve the same signal-to-quantization-noise performance with a lower $\Delta\Sigma$ modulator order and lower oversampling ratio. The use of multibit feedback also relaxes the slew rate and settling time requirements on the analog integrators by greatly reducing the magnitude of the error signal to be integrated.

While reducing the $\Delta\Sigma$ modulator order and oversampling ratio eases the design of the analog front end, it also reduces the noise transfer function's attenuation of circuit noise introduced at the quantizer. Thus the performance of the internal quantizer, typically implemented as a flash ADC, can limit the $\Delta\Sigma$ modulator's performance. High-performance $\Delta\Sigma$ADCs use fully-differential analog circuitry to improve the their immunity to noise coupled through the bias nodes, power supplies, and substrate. To preserve the noise rejection benefits of the differential architecture, the flash ADC must quantize the loop filter's differential output and reject its common-mode component.

Conventional analog circuit techniques for implementing differential input flash ADCs present significant design challenges in a 3.3-V, single-poly CMOS process optimized for digital circuits. One approach uses a pair of switched capacitors per comparator to sample the input and reference levels on alternating clock phases [1], [2]. This technique can require a prohibitively large area for a multibit $\Delta\Sigma$ modulator implemented in a CMOS process in which large-area metal-metal capacitors are the only linear capacitor structures. Because the reference ladder is sampled in the switched-capacitor approach, its design is complicated by the requirement that the capacitors must be fully charged at the oversampled clock rate. An alternate common-mode rejection circuit, referred to as a differential differencing amplifier (DDA), uses two differential pairs per comparator to subtract the common-mode

component in the current domain [3]. This approach is challenging given the limited supply voltage because it requires the design of a differential pair with a wide linear input range, low input-referred offset, and high transconductance. In addition, modulation of the differential pairs' transconductances by the common-mode signal can give rise to intermodulation of the differential-mode signal and the common-mode noise.

This paper presents a digital common-mode rejection (DCMR) flash ADC and noise-shaped requantizer used as the internal quantizer in a pair of high-performance, single-poly CMOS $\Delta\Sigma$ modulator IC prototypes [4], [5]. The DCMR flash ADC and requantizer together perform 33-level differential mode quantization without the area penalty and circuit complications of the switched-capacitor or DDA approaches. The DCMR flash ADC uses a pair of single-ended, 33-level flash ADCs to quantize the positive and negative portions of the loop filter's differential output and digitally subtracts the single-ended outputs to cancel the common-mode component. Because the subtraction results in a 65-level difference signal, a dithered, first-order shaped requantizer reduces the DCMR flash ADC output to 33 levels. The requantizer allows the use of a 33-level mismatch-shaping DAC encoder rather than a more complex 65-level encoder. Theoretical results are presented which show that the DCMR flash ADC provides a quantized representation of the differential signal with quantization error power less than or equal to that of a conventional 33-level flash ADC even in the presence of common-mode noise. The prototype implementation details show that the DCMR flash ADC required less area than the switched-capacitor and DDA implementations considered for the prototype. The measured common-mode rejection performance of the prototype shows that the DCMR flash ADC can reject a 200-mV common-mode sinusoid with only 0.4 dB

Figure 4.1: The high-level circuit topology of the prototype ADC $\Delta\Sigma$ modulator.

degradation in the $\Delta\Sigma$ modulator's signal-to-noise-and-distortion.

The paper consists of two main sections and an Appendix. Section II presents the implementation of the DCMR flash ADC in the ADC $\Delta\Sigma$ modulator prototype IC initially presented in [4], simulated common-mode rejection of the DCMR flash ADC, and measured common-mode rejection of the DCMR flash ADC in the prototype IC. Section III presents the signal processing details of the DCMR flash ADC and noise-shaped requantizer used within a multibit $\Delta\Sigma$ modulator. The Appendix presents detailed derivations of results used in Section III.

## II. DCMR IMPLEMENTATION IN THE $\Delta\Sigma$ MODULATOR PROTOTYPE

The $\Delta\Sigma$ modulator described in the introduction is a second-order design operating at a clock rate of 3.072 MHz with an oversampling ratio of 64. The prototype was fabricated in a 3.3-V, 0.5-$\mu$m single-poly, triple-metal CMOS process, and it achieves 98-dB peak signal-to-noise-and-distortion (SINAD) and 105-dB spurious-free-dynamic-range (SFDR) in a 24-kHz signal bandwidth [4]. As shown in Figure 4.1, it was implemented with two delaying switched-capacitor integrators, a 33-level mismatch-shaping DAC and a 33-level DCMR flash ADC [4],[6],[7]. The single-ended flash ADCs within the DCMR flash ADC use a comparator offset dynamic
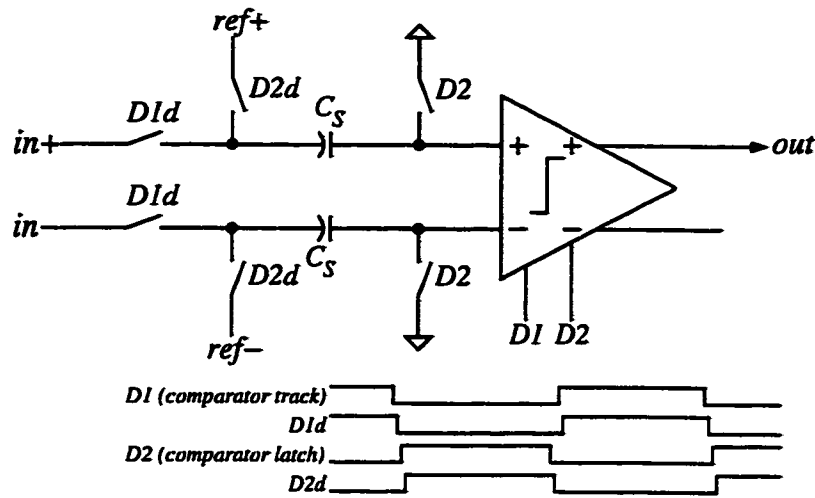
Figure 4.2: The switched-capacitor common-mode rejection approach applied to a comparator within the flash ADC.

element matching (DEM) technique to attenuate distortion caused by comparator input offset errors [8].

While the $\Delta\Sigma$ modulator's noise transfer function does provide some attenuation of circuit noise introduced at the quantizer, it provides only 52 dB of attenuation at the 24 kHz passband edge. For example, if the common-mode to differential-mode conversion gain ($A_{cm-dm}$) of flash ADC's input stage is 0 dB, the converter's common-mode rejection ratio (CMRR) will be 54 dB at 24 kHz and at multiples of 3.072 MHz $\pm$ 24 kHz. In this case, a 30-mV, 24-kHz common-mode sinusoid at the quantizer's input will limit the $\Delta\Sigma$ADC's peak SFDR to 82 dB. Thus, the quantizer must provide additional common-mode rejection to preserve the benefits of the fully-differential analog front end and to ensure meeting the 105-dB SFDR target.

## CONVENTIONAL APPROACHES

Two conventional approaches to implementing a 33-level, differential input flash ADC were considered for the $\Delta\Sigma$ modulator prototype, but the die area requirements and circuit design challenges motivated the search for an alternative solution.
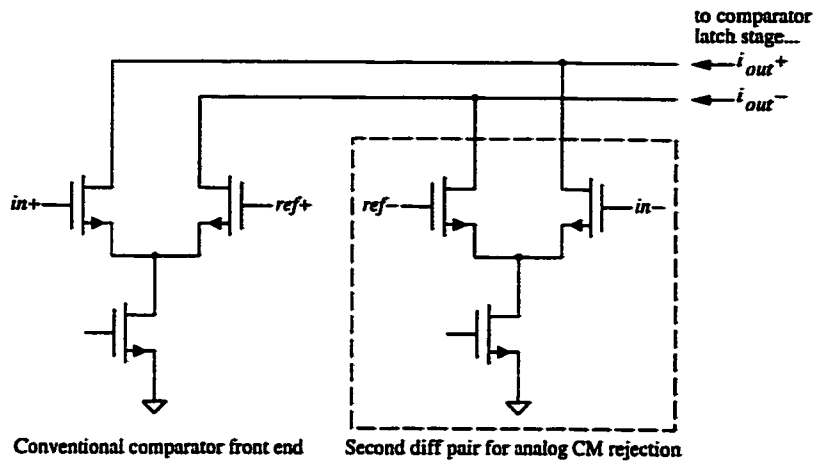
Figure 4.3: DDA common-mode rejection applied to a comparator within the flash ADC.

The switched-capacitor common-mode rejection approach, shown in Figure 4.2, uses a pair of switched capacitors for each comparator in the flash ADC to sample the differential input signal, $(in_+ - in_-)$, and differential reference, $(ref_+ - ref_-)$, on alternate clock phases [1]. A 33-level switched-capacitor flash ADC would require a bank of 32 comparators, an array of 64 capacitors, and a 33-level thermometer-to-binary decoder. To keep the sampling capacitor large relative to the comparators' input capacitance, it must be on the order of 100 fF. With the parallel-plate metal interconnect capacitors used in the design, the sampling capacitor array would have required an area of approximately 0.40 mm$^2$. Thus, the sampling capacitors would have dominated the 0.59-mm$^2$ total die area required for the flash ADC with switched-capacitor common-mode rejection. In addition, each of the 32 sampling capacitors would have a bottom plate parasitic capacitance to the substrate on the order of 50-100 fF. These parasitic capacitances would be switched between the second integrator's output and the reference ladder on alternate clock phases, so the reference ladder would need to be capable of fully charging them to avoid signal-dependent settling errors that would give rise to distortion. The references' source resistance could have been reduced by using low resistance values in the ladder, but
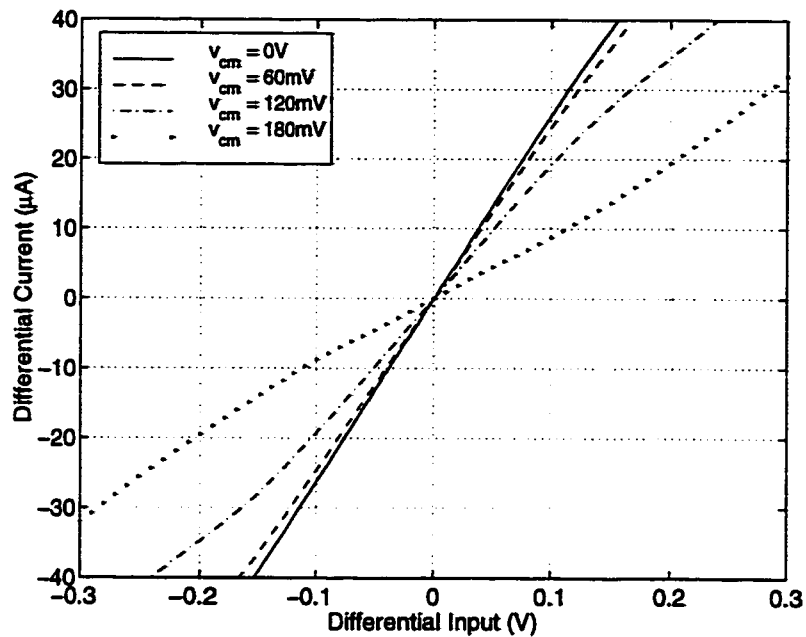
Figure 4.4: Simulation results illustrating the modulation of the DDA transconductance by the common-mode signal.

this would have increased power dissipation and would have required fast-settling, high current buffers to drive the ends of the resistor ladder. Source-followers could have been used on each reference tap to reduce the source resistance as in [9], but threshold voltage mismatches among devices would have introduced an additional distortion mechanism.

The DDA approach, shown in Figure 4.3, uses two differential pairs per comparator to convert the signals $(in_+ - ref_+)$ and $(in_- - ref_-)$ to currents which are subtracted to reject the common-mode component [3]. The challenge in implementing this technique is that the differential pairs must have a sufficiently wide linear input range to accommodate the expected common-mode offset and common-mode noise. For a fixed tail current, increasing the input range would imply reduced transconductance and reduced attenuation of offsets in the latching stage. For a fixed transconductance, increasing the input range would imply increased tail current and thus increased power dissipation. A second problem results from the

modulation of the differential pairs' transconductance by the input common-mode level. Figure 4.4 shows the differential output current of a DDA input stage as a function of the differential input voltage for several common-mode levels. In this simulation, $(ref_+ - ref_-) = 0$ V. The change in slope near zero differential input indicates the degree of change in the transconductance. In a comparator, this effect would cause the input-referred offset of the latching stage to be modulated by the common-mode signal and would lead to a mechanism for the intermodulation of the common-mode and differential-mode signals.

Though it would be possible to use the comparator offset dynamic element matching (DEM) technique presented in [8] with the DDA approach to spectrally-whiten the effects of static offsets due to the differential pairs and latching stage, the offsets dependent on the common-mode signal could still lead to spurious tones. Therefore, with the DDA approach it is best to use large-area, well-matched devices to minimize the magnitude of these signal-dependent offsets. Thus, even though the DDA approach does not require capacitors, it would result in increased die area because minimum-size devices could not be used in the 32 comparators [10].

## THE DCMR APPROACH

The DCMR flash ADC shown in Figure 4.5, was implemented in the $\Delta\Sigma$ modulator to avoid the area requirements and circuit difficulties of the conventional approaches described above. The DCMR flash ADC implemented in the $\Delta\Sigma$ modulator prototype uses a pair of 33-level, single-ended flash ADCs with a shared reference ladder to quantize the positive and negative portions of the second integrator's differential output.

In the absence of common-mode noise, the DCMR flash ADC output would take on only even values, and the least significant bit (LSB) could simply be dropped to
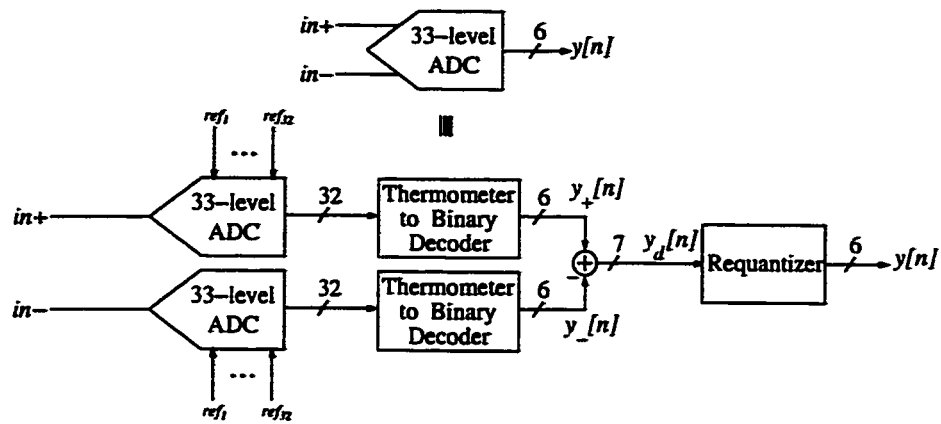
Figure 4.5: The high-level circuit topology of the digital common mode rejection flash ADC architecture.
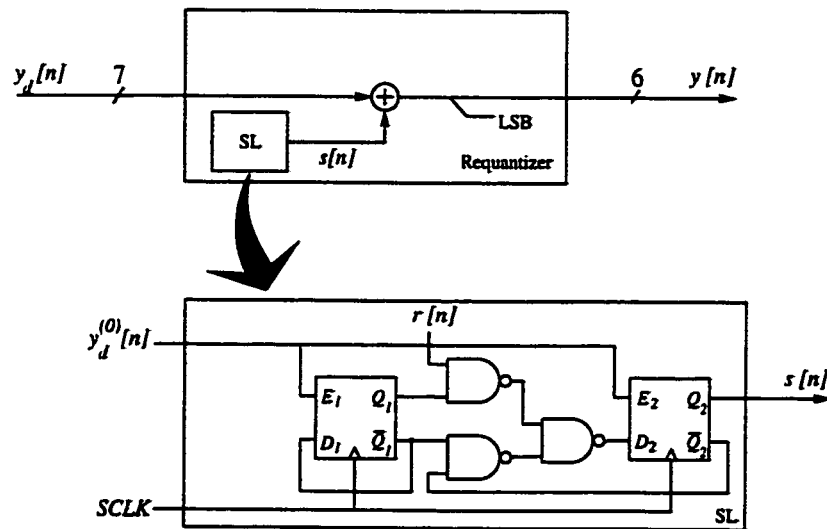


Figure 4.6: High-level view of the requantization algorithm.

yield a 33-level quantized representation of the differential input. However, when common-mode noise is present, the difference signal takes on both even and odd values. One could use a 65-level mismatch-shaping DAC encoder rather than a 33-level encoder to accommodate the additional quantization levels, but this would nearly double its die area. Truncating the LSB in this case to yield a 33-level signal would create spurious tones because truncation is a form of undithered quantization. To reduce the difference signal to 33 levels without introducing spurious tones,

the requantizer shown in Figure 4.6 was used. The sequencing logic (SL) shown in Figure 4.6 is analogous to a first-order digital $\Delta\Sigma$ modulator. It generates a dithered, first-order shaped sequence which determines whether $y_d[n]$ is rounded up or down. Thus, the error due to requantization is uncorrelated from the input and has a first-order, highpass-shaped power spectral density (PSD).

By avoiding the use of capacitors, the DCMR approach eliminates the area overhead of the metal-metal capacitors needed to implement switched-capacitor common-mode rejection. While both the DDA common-mode rejection approach and the DCMR approach require 64 differential pairs, these devices can be made nearly minimum-size in the DCMR flash ADC if comparator offset DEM is used to spectrally whiten the input-referred offsets of each comparator [8]. This advantage offsets the fact that the DCMR flash ADC requires additional digital logic — a second 33-level thermometer-to-binary encoder, an adder and requantization logic.

Behavioral simulation results for the $\Delta\Sigma$ modulator with a -6-dB sinusoidal input are shown in Figure 4.7. In the absence of common-mode noise, the $\Delta\Sigma$ modulator achieves 101.9 dB SINAD, as shown in the PSD plot in Figure 4.7a. Figure 4.7b–Figure 4.7d show simulated performance with a 200-mV peak, 20.7 kHz common-mode sinusoid superimposed on the second integrator's output. The PSD for the $\Delta\Sigma$ modulator using a single-ended flash ADC with no common-mode rejection is shown in Figure 4.4b to emphasize that the noise transfer function alone does not provide sufficient attenuation to ensure meeting the 105-dB SFDR target. In this case, the SINAD is limited to 56.9 dB by the 20.7-kHz spurious component. Figure 4.4c shows the output PSD when the DCMR flash ADC is used and the difference signal is reduced to 33 levels by truncation. As noted previously, undithered truncation generates significant spurious tones. The configuration used
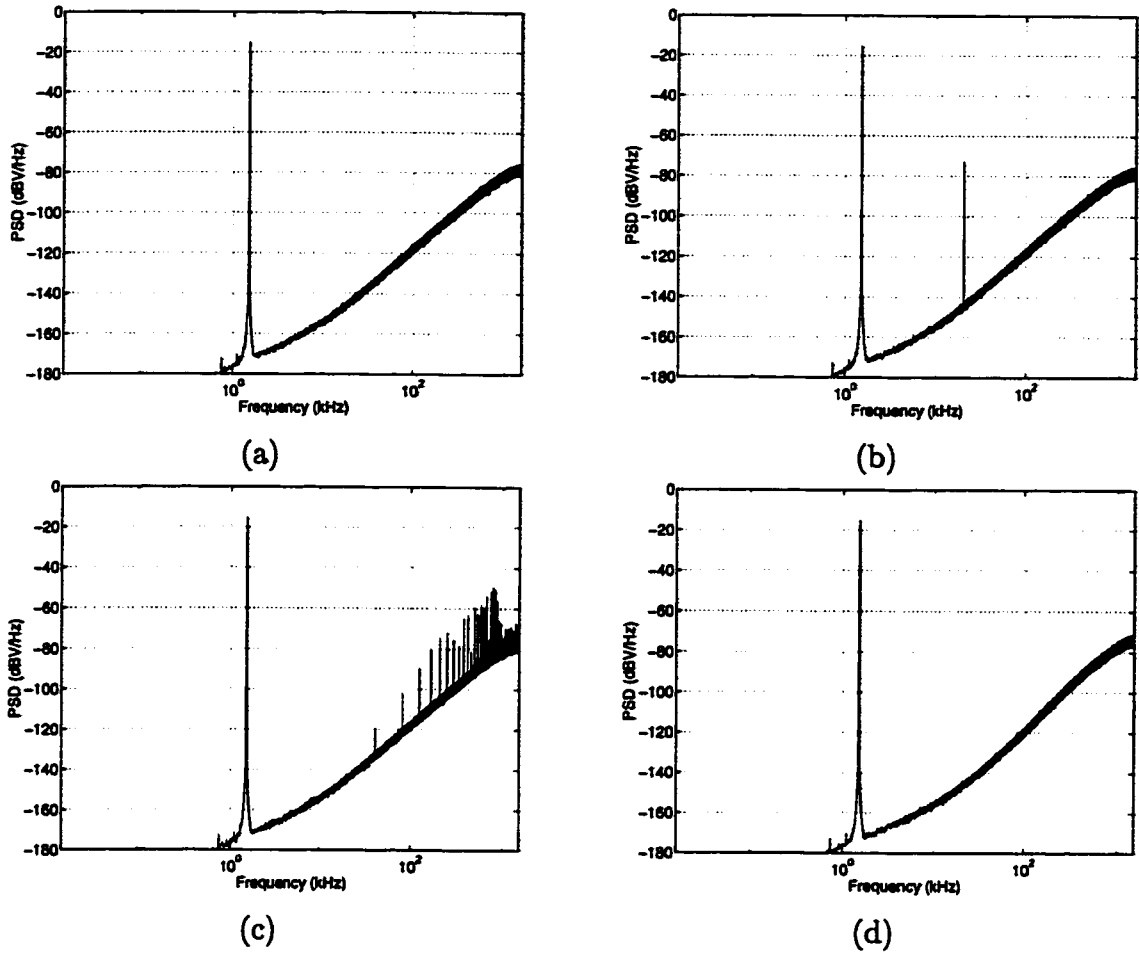
Figure 4.7: Comparison of simulated results for a -6-dB, 1.5-kHz input signal and 200-mV, 20.7-kHz common-mode noise: (a) no common-mode noise, (b) no common-mode rejection, (c) DCMR with truncation, and (d) DCMR with shaped requantization.
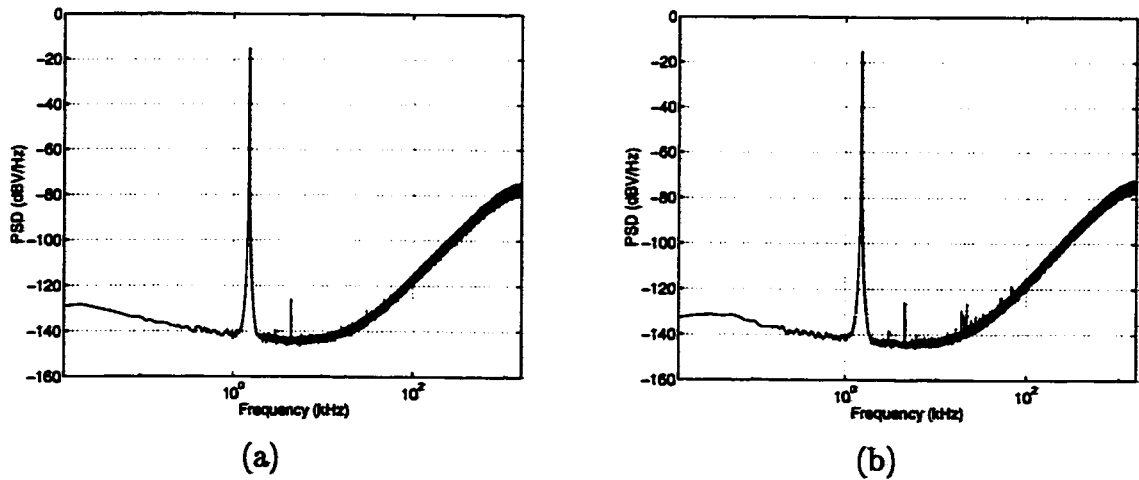


Figure 4.8: Measured performance of DCMR in the $\Delta\Sigma$ modulator prototype: (a) no common-mode noise, (b) 200-mV peak 20.7-kHz common-mode sinusoid injected on reference ladder to flash ADCs.

in the $\Delta\Sigma$ modulator prototype — the DCMR flash ADC and the dithered, first order shaped requantizer — is shown in Figure 4.7d. Despite the presence of a significant common-mode signal, the $\Delta\Sigma$ modulator achieves 104.1 dB SINAD. As will be shown in the next section, the presence of common-mode noise can in some cases *reduce* the quantization error power in the DCMR flash ADC.

Measured common-mode rejection results for the $\Delta\Sigma$ modulator prototype IC in Figure 4.8 show that the DCMR flash ADC effectively eliminates common-mode noise. With -6-dB, 1.5-kHz input and no common-mode noise, as shown in Figure 4.8a, the SINAD is 96.2 dB. With a 200-mV peak, 20.7-kHz sinusoid injected on the flash ADC's reference ladder, as shown in Figure 4.8b, the SINAD is 95.8 dB. The SFDR in each case is 110.8 dB and is limited by the third-harmonic distortion of the switched-capacitor circuitry rather than the performance of the DCMR flash ADC.

By avoiding the use of capacitors, the DCMR flash ADC resulted in significant area savings in a single-poly CMOS implementation. Figure 4.9 shows the layout of the prototype $\Delta\Sigma$ modulator using the DCMR flash ADC and requantizer presented in [5]. The 33-level DCMR flash ADC die area in a 0.5-$\mu$m[†] single-poly CMOS process is 0.42 mm$^2$. Even though switched-capacitor common-mode rejection would have reduced the number of comparators by a factor of two, it would have required a 0.40 mm$^2$ capacitor array — approximately the size of $C_{DAC_2}$ in Figure 4.9 — making its total area 0.59 mm$^2$. Thus, the DCMR approach provided a 30% reduction in die area relative to the switched-capacitor approach.

The die area of the DCMR flash ADC also compares favorably to that required for the DDA approach. In [10], a 17-level flash ADC was implemented in a 0.65-$\mu$m CMOS process using the DDA approach with a die area of approximately 0.22 mm$^2$.

---

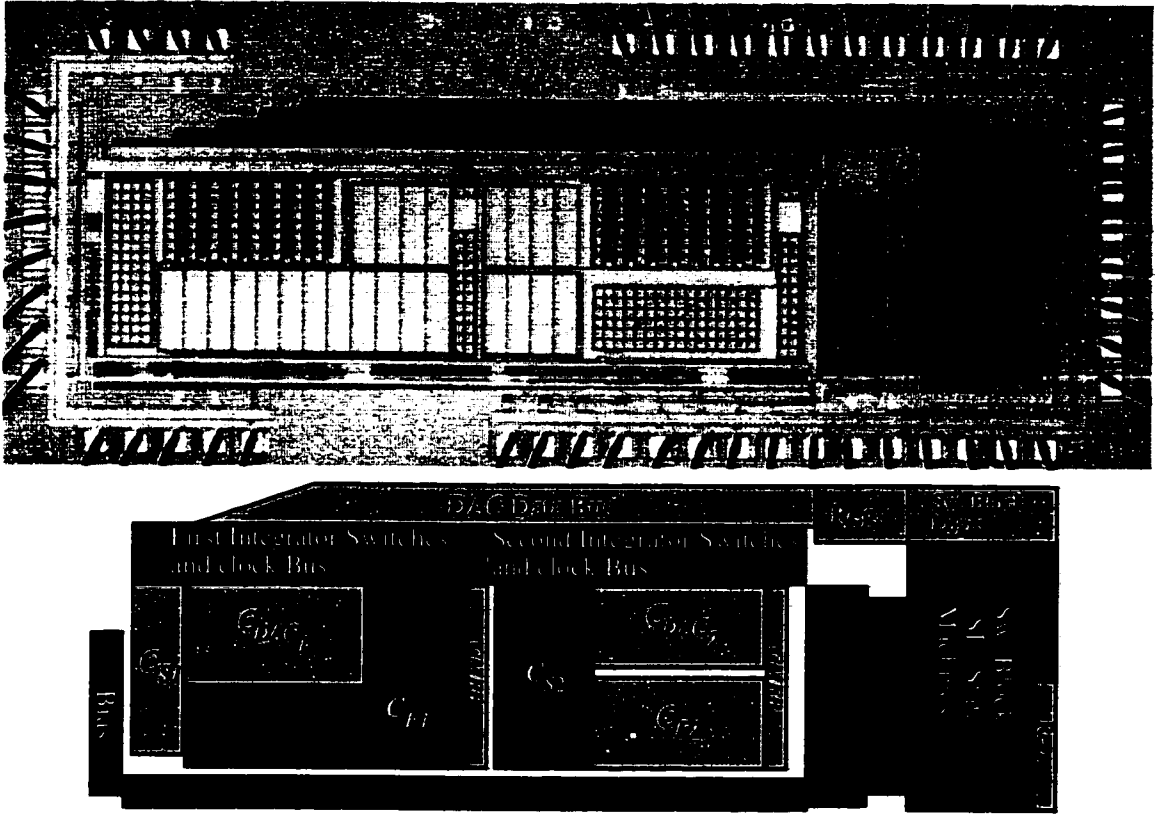[†] Minimum drawn gate length in this process is 0.6$\mu$m.

Figure 4.9: Layout of the 33-level DCMR flash ADC within the $\Delta\Sigma$ modulator prototype.

Assuming that extending this design to 33 levels would double its area, this design would require roughly the same area as the DCMR flash ADC. As future generations of CMOS fabrication processes are developed with even smaller device dimensions and further reduced supply voltages, the DCMR approach will be even more attractive because it minimizes the requirements on the analog circuits and capitalizes on the strengths of a digital-optimized fabrication process.

### III. SIGNAL PROCESSING DETAILS

Each single-ended flash ADC within the DCMR flash ADC is implemented as shown in Figure 4.10. The *positive flash ADC* quantizes the positive half of the second integrator's differential output, and the *negative flash ADC* quantizes the negative half of the differential output. Each flash ADC implements a mid-step
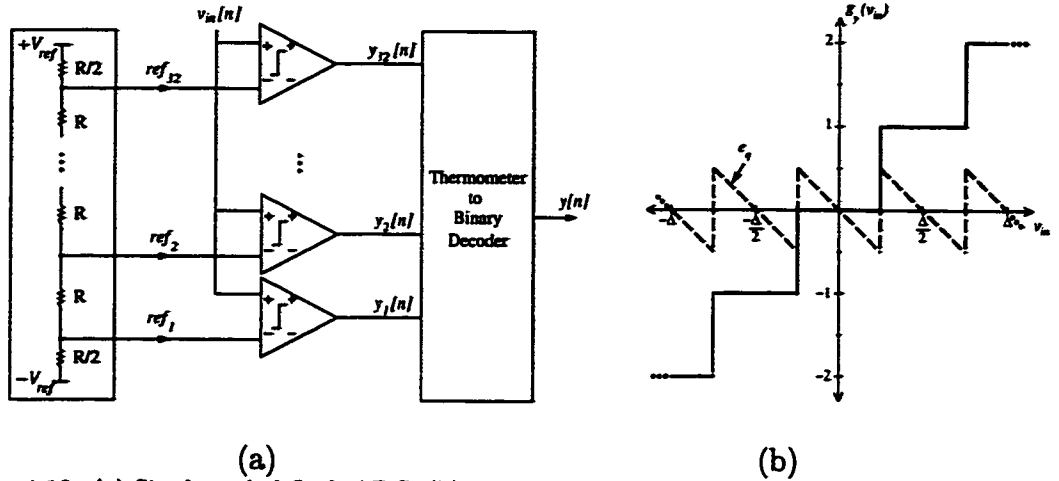
(a)            (b)

Figure 4.10: (a) Single-ended flash ADC. (b) Transfer function of single-ended flash ADC.

quantizer with step size $\frac{\Delta}{2}$, where $\Delta$ is the step size of the overall DCMR flash ADC. Let $g_{y_+}(v)$ denote the input-output transfer function of the positive flash ADC, where the output sequence is $y_+[n] = g_{y_+}(v[n])$. The input-output transfer function is given by

$$g_{y_+}(v) = \frac{1}{\Delta/2}v + g_{e_{q_+}}(v),\tag{1}$$

and the quantization error is given by

$$g_{e_{q_+}}(v) = \frac{1}{2} - \left\langle \frac{v}{\Delta/2} + \frac{1}{2} \right\rangle,\tag{2}$$

where $\langle x \rangle$ denotes the fractional part of $x$. Similarly, the negative flash ADC's input-output transfer function is given by

$$g_{y_-}(v) = \frac{1}{\Delta/2}v + g_{e_{q_-}}(v),\tag{3}$$

where,

$$g_{e_{q_-}}(v) = -\frac{1}{2} + \left\langle -\frac{v}{\Delta/2} + \frac{1}{2} \right\rangle.\tag{4}$$

For convenience in the analysis that follows, the values of (1) and (3) at the quantization thresholds have been assigned differently. For physical analog signals, the

probability of the input landing exactly on a quantization threshold is zero. Therefore, this choice does not affect the final results.

Let $v_{in}$ denote the DCMR flash ADC's differential-mode input signal, and let $v_{cm}$ denote its common-mode input signal. The DCMR flash ADC's input-output transfer function, $g_{y_d}(v_{in}, v_{cm})$, is formed by subtracting the outputs of the positive and negative flash ADCs and is given by

$$g_{y_d}(v_{in}, v_{cm}) = \frac{2v_{in}}{\Delta} + g_{e_{q+}}\left(\frac{v_{in}}{2} + v_{cm}\right) - g_{e_{q-}}\left(-\frac{v_{in}}{2} + v_{cm}\right), \tag{5}$$

where $g_{e_{q+}}(v)$ and $g_{e_{q-}}(v)$ are given by (2) and (4), respectively.

Figure 4.11–Figure 4.13 show how the common-mode signal affects the quantization error at the output of the DCMR flash ADC. In Figure 4.11, $v_{cm} = 0$, and the resulting quantization error is that of a 33-level quantizer followed by a gain of two. As noted previously, the DCMR flash ADC produces only even outputs when $v_{cm} = 0$. As the common-mode voltage is increased to $\frac{\Delta}{16}$, as shown in Figure 4.12, the positive flash ADC's transfer function moves to the left and the negative flash ADC's transfer function moves to the right. Though this results in non-uniform quantization, the input-output transfer function is still a periodic function of $v_{in}$ with period $\Delta$. For $v_{cm} = \frac{\Delta}{8}$ as in Figure 4.13, the DCMR flash ADC's transfer function is effectively that of a 65-level quantizer. Thus, a side-effect of the DCMR flash ADC is that the correlation between the error of the positive and negative flash ADCs tends to reduce the overall quantization error for inputs with a non-zero common-mode component.

Because of the relationship between the quantization errors noted above, the negative flash ADC's quantization error is completely determined given the positive flash ADC's quantization error and the common-mode signal according to

$$g_{e_{q-}}(e_{q+}, v_{cm}) = -\frac{1}{2} + \left\langle -e_{q+} - \left\langle \frac{4v_{cm}}{\Delta} \right\rangle + \frac{1}{2} \right\rangle, \tag{6}$$
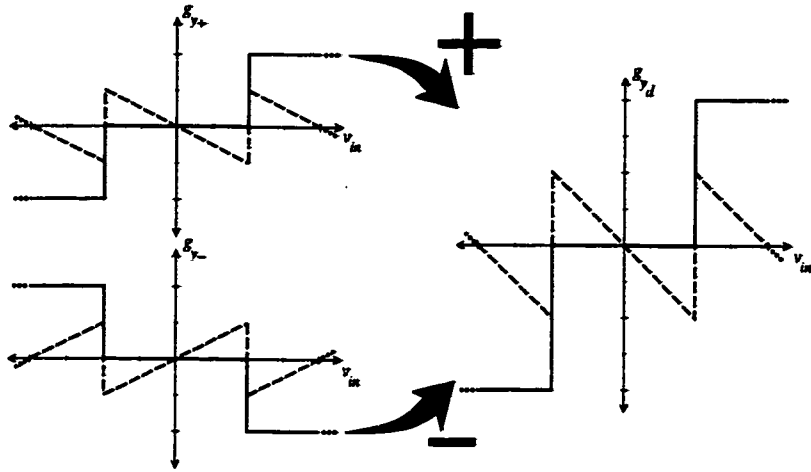
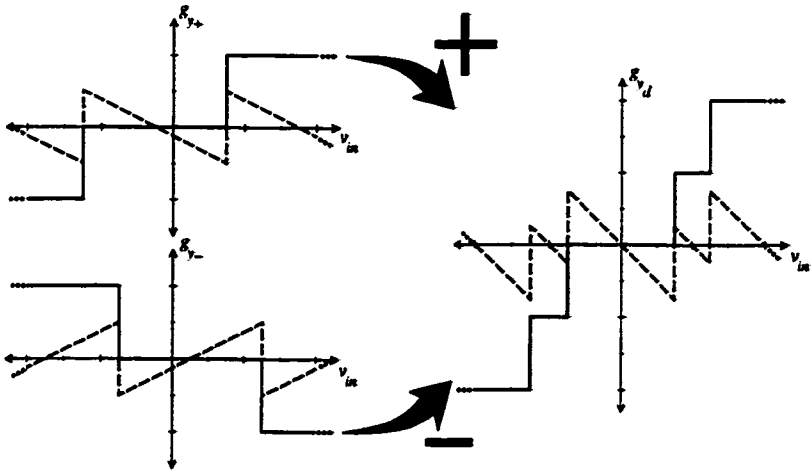Figure 4.11: DCMR flash ADC output and quantization error transfer functions with $v_{cm} = 0$.



Figure 4.12: DCMR flash ADC output and quantization error transfer functions with $v_{cm} = \frac{\Delta}{16}$.
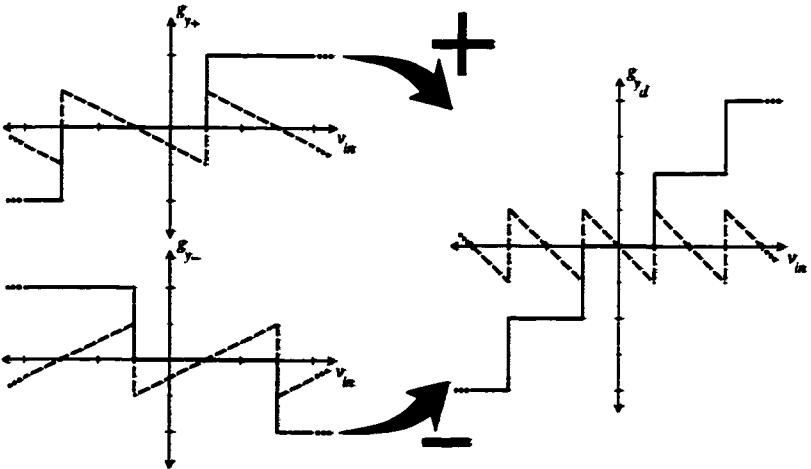


Figure 4.13: DCMR flash ADC output and quantization error transfer functions with $v_{cm} = \frac{\Delta}{8}$.
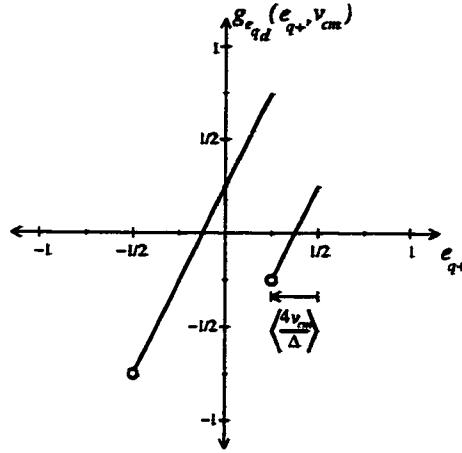
Figure 4.14: The DCMR flash ADC's quantization error in terms of that of the positive flash ADC and the common-mode signal; note that $-\frac{\Delta}{2} < e_{q_+} \leq \frac{\Delta}{2}$.
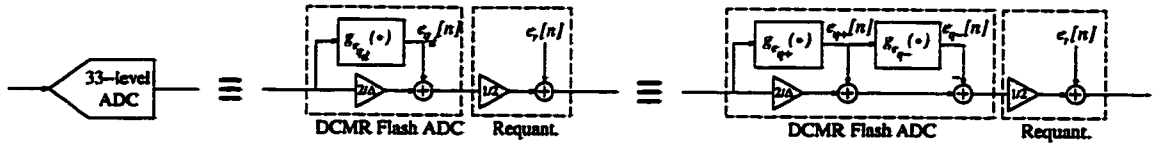


Figure 4.15: Equivalent block diagram representations of the DCMR flash ADC.

where $e_{q_+}$ is the quantization error of the positive flash ADC. Thus, the quantization error of the DCMR flash ADC can be viewed as a memoryless transformation of the positive flash ADC's quantization error which depends on the common-mode signal with

$$g_{e_{q_d}}\left(e_{q_+}, v_{cm}\right) = e_{q_+} - g_{e_{q_-}}\left(e_{q_+}, v_{cm}\right). \tag{7}$$

The transformation of $e_{q_+}$ to $e_{q_d}$ performed by (7) is illustrated in Figure 4.14 for $v_{cm} = \frac{\Delta}{16}$. The equivalent block diagram representation of the DCMR flash ADC implied by (7) is shown in Figure 4.15.

## BEHAVIOR OF THE DCMR FLASH ADC WITHIN THE $\Delta\Sigma$ MODULATOR

In [11], it has been shown that the time average PSD of the output of the second-order ADC $\Delta\Sigma$ modulator of Figure 4.1 with an ideal 33-level quantizer is that of the input signal plus white noise shaped by a $(1 - z^{-1})^2$ filter provided the input has a noise component. In practice, this condition is satisfied because

of the inevitable thermal noise present at the input of an ADC $\Delta\Sigma$ modulator. As the $\Delta\Sigma$ modulator operates, the accumulation of the input noise within the loop filter effectively decorrelates successive values of the quantization error and decorrelates the quantization error from the input signal. Thus, as $n \to \infty$, the injected quantization error, $e_q[n]$, converges to an uncorrelated sequence of random variables with a uniform probability density on $(-\frac{1}{2}, \frac{1}{2}]$. In practice, the convergence occurs so quickly that the measured (i.e. time average) autocorrelations and PSDs of the $\Delta\Sigma$ modulator's output are indistinguishable from those that would result from white noise passed through a $(1 - z^{-1})^2$ filter.

Despite the fact that the DCMR flash ADC behaves in general as a non-uniform quantizer, the analysis in [11] is applied below to show that its quantization error is asymptotically a sequence of pairwise independent random variables with a distribution that depends on the common-mode noise. It is also shown that the presence of common-mode noise actually reduces the power of the quantization error signal.

The prototype $\Delta\Sigma$ modulator's block diagram is shown in Figure 4.16a, and it can be verified that it is functionally equivalent to the block diagram of Figure 4.16b with

$$F(z) = \frac{z^{-2}}{(1 - z^{-1})^2},$$ (8)

and

$$G(z) = -\frac{z^{-2}}{(1 - z^{-1})^2} - \frac{2z^{-1}}{(1 - z^{-1})}.$$ (9)

Because the impulse response of $G(z)$ takes on only integer values for all $n$, the feedback signal to the quantizer only changes the quantizer's input by an integer multiple of $\Delta$, the quantization step. In [11], it is noted that when the quantizer is not overloaded, the quantization error transfer function is periodic in $\Delta$ and therefore the $G(z)$ feedback signal has no effect on the value of the quantization

(a)

(b)

(c)
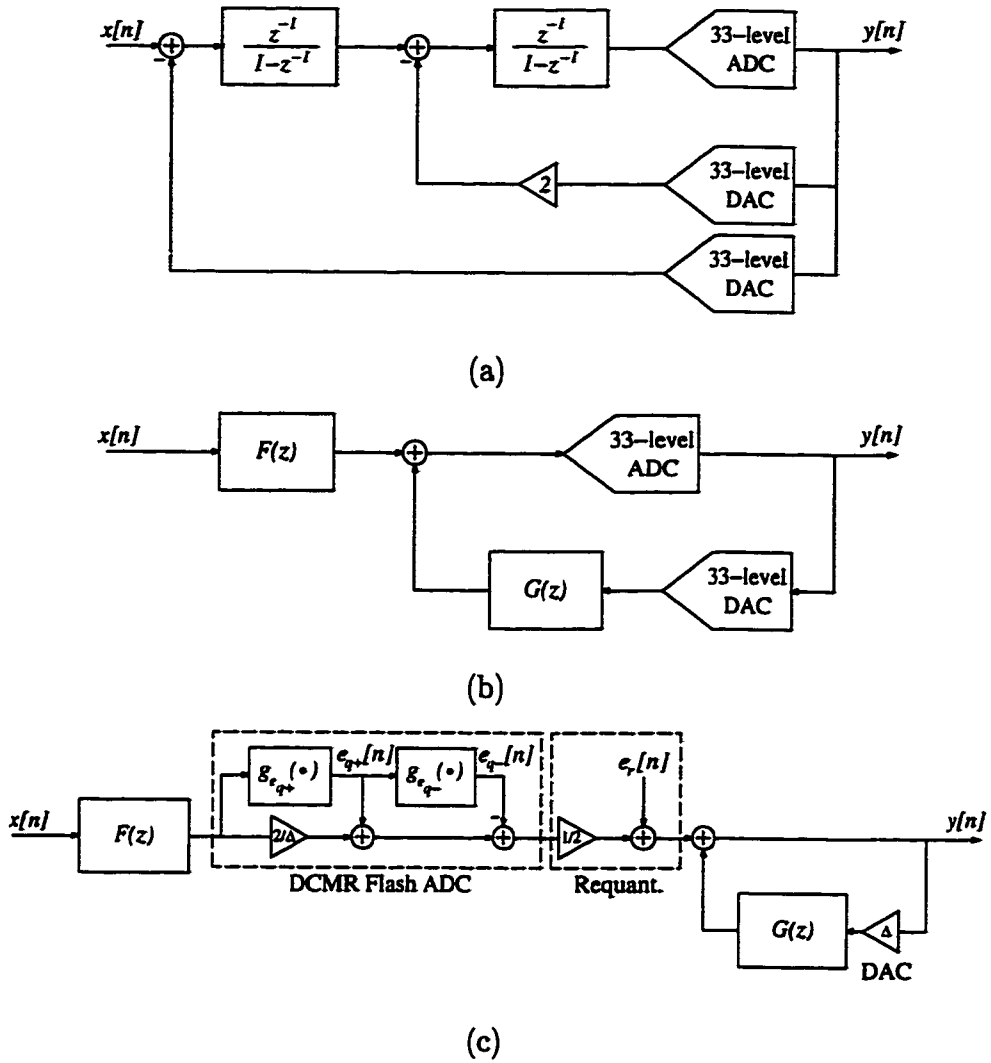
Figure 4.16: Equivalent block diagram representations of the prototype $\Delta\Sigma$ modulator showing that DCMR flash ADC and requantizer can be viewed as additive noise sources outside the $G(z)$ feedback loop.

error.

Provided that the $\Delta\Sigma$ modulator input and common-mode noise do not overload the single-ended flash ADCs, (2), (4), and (5) imply that the DCMR flash ADC's transfer function is periodic function of $v_{in}$ with period $\Delta$ and therefore can be moved outside the feedback loop as shown in Figure 4.16c. Using (7), the DCMR flash ADC's quantization error, $e_{q_d}$, can be viewed as the quantization error of positive flash ADC followed by a transformation of the positive ADC's quantization

Figure 4.17: A graphical representation of the transformation of $f_{e_{q+}}(e_{q+})$ to $f_{e_{qd}}(e_{qd})$ for $v_{cm} = \frac{\Delta}{16}$.

error according to (6). It is shown in the next section that the requantizer can also be moved outside the $G(z)$ feedback loop as illustrated in Figure 4.16c.
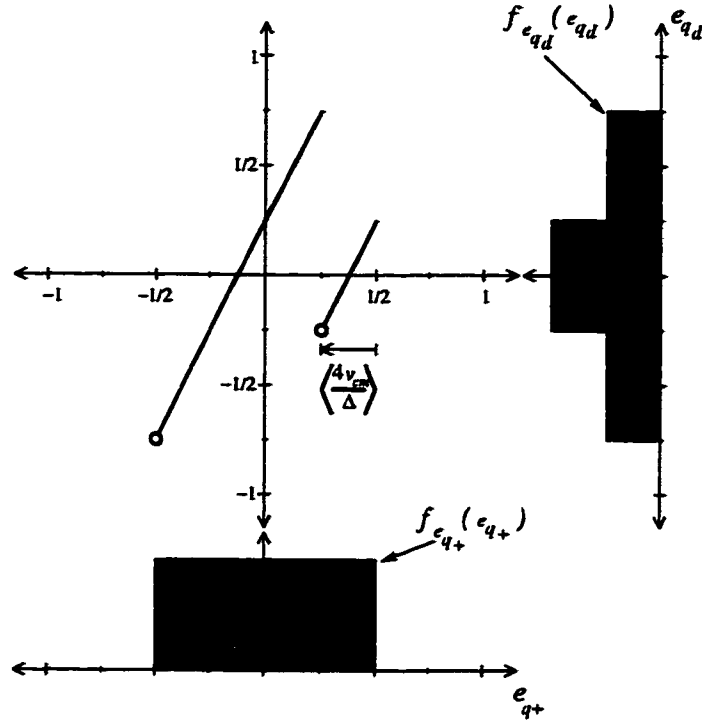
With the DCMR flash ADC removed from the $G(z)$ feedback loop, the input to the positive flash ADC is the input signal plus thermal noise passed through $F(z)$, a cascade of two discrete-time integrators. This gives rise to the decorrelation of successive samples of the quantization error mentioned earlier. Specifically, as $a \to -\infty$, where $a$ is the time at which the $\Delta\Sigma$ modulator is started from reset, $e_{q+}[n]$ converges to a sequence of uniformly distributed random variables independent of the input signal, where $e_{q+}[n_1]$ and $e_{q+}[n_2]$ are independent for any $n_1 \neq n_2$. Details of this result are presented in Theorem 1 and Corollary 2 of the Appendix. It is also shown in Theorem 3 of the Appendix that the ensemble limits and time average limits converge to the same value. Thus, the asymptotic behavior of the quantization error can be observed by measuring the time average autocorrelations

**(a)**          **(b)**          **(c)**

Figure 4.18: Simulated probability densities for $v_{cm} = 0$: (a) $(e_{q_+}[n],\ e_{q_+}[n+1])$, (b) $(e_{q_-}[n],\ e_{q_-}[n+1])$, (c) $(e_{q_d}[n],\ e_{q_d}[n+1])$.



**(a)**          **(b)**          **(c)**

Figure 4.19: Simulated probability densities for $v_{cm} = \frac{\Delta}{16}$: (a) $(e_{q_+}[n],\ e_{q_+}[n+1])$, (b) $(e_{q_-}[n],\ e_{q_-}[n+1])$, (c) $(e_{q_d}[n],\ e_{q_d}[n+1])$.



**(a)**          **(b)**          **(c)**
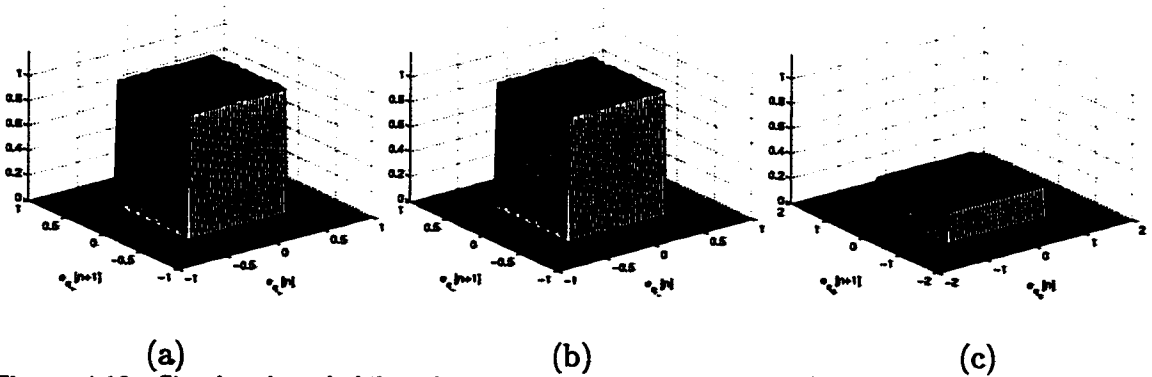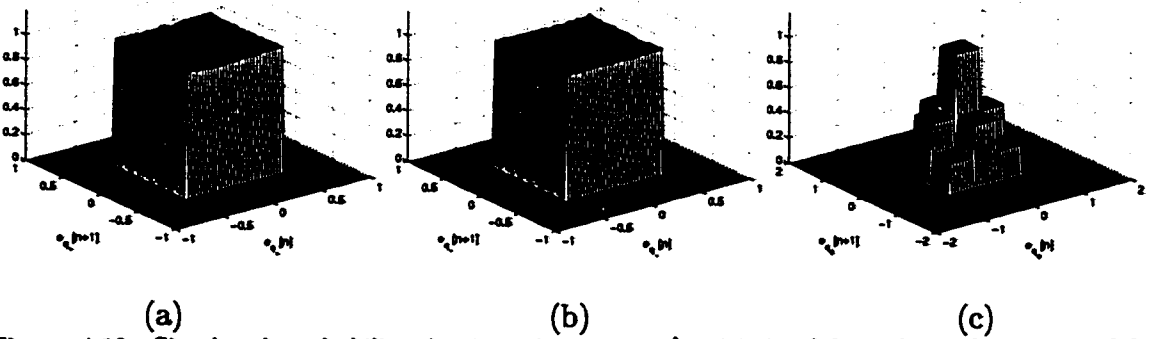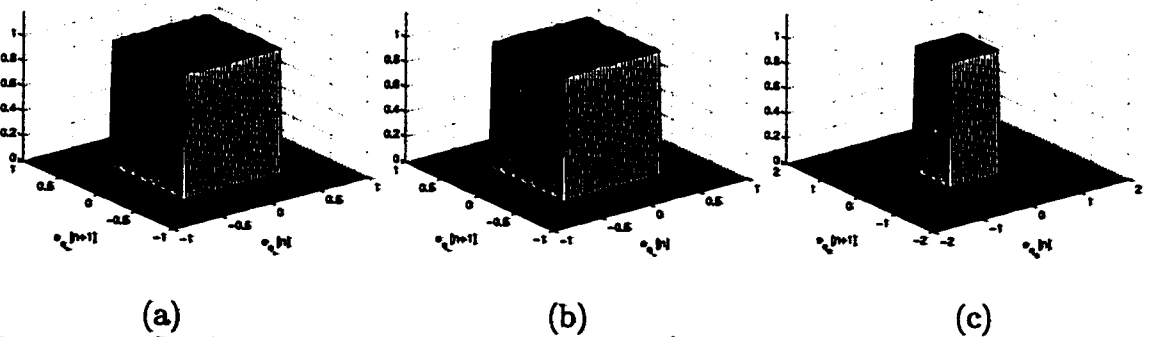
Figure 4.20: Simulated probability densities for $v_{cm} = \frac{\Delta}{8}$: (a) $(e_{q_+}[n],\ e_{q_+}[n+1])$, (b) $(e_{q_-}[n],\ e_{q_-}[n+1])$, (c) $(e_{q_d}[n],\ e_{q_d}[n+1])$.

and PSDs.

Because $e_{q_d}[n]$ is a memoryless transformation of $e_{q_+}[n]$, it follows that $e_{q_d}[n]$ is also asymptotically a pairwise independent sequence of random variables indepen-

dent of the $\Delta\Sigma$ modulator's input and that $e_{q_d}[n_1]$ and $e_{q_d}[n_2]$ are asymptotically independent for $n_1 \neq n_2$. A graphical representation of the transformation of $f_{e_{q_+}}(e_{q_+})$ to $f_{e_{q_d}}(e_{q_d})$ by (7) is shown in Figure 4.17 for $v_{cm} = \frac{\Delta}{16}$. It follows from (6) and (7) that the probability density of the DCMR flash ADC's quantization error for arbitrary values of $v_{cm}$ is given by

$$f_{e_{q_d}}(e_{q_d}|v_{cm}) = \begin{cases} \frac{1}{2} & -1 + \left\langle \frac{4v_{cm}}{\Delta} \right\rangle < e_{q_d} \leq -\left\langle \frac{4v_{cm}}{\Delta} \right\rangle, \\ 1 & -\left\langle \frac{4v_{cm}}{\Delta} \right\rangle < e_{q_d} \leq \left\langle \frac{4v_{cm}}{\Delta} \right\rangle, \\ \frac{1}{2} & \left\langle \frac{4v_{cm}}{\Delta} \right\rangle < e_{q_d} \leq 1 - \left\langle \frac{4v_{cm}}{\Delta} \right\rangle, \\ 0 & \text{otherwise.} \end{cases} \quad (10)$$

It can be verified using (10) that the power of the DCMR flash ADC's quantization error given $v_{cm}$ is given by

$$E\{e_{q_d}^2|v_{cm}\} = \left\langle \frac{4v_{cm}}{\Delta} \right\rangle^2 - \left\langle \frac{4v_{cm}}{\Delta} \right\rangle + \frac{1}{3}. \quad (11)$$

This implies that $\frac{1}{12} \leq E\{e_{q_d}^2\} \leq \frac{1}{3}$. Note that the DCMR quantizer is followed by an effective gain of $\frac{1}{2}$ in the requantizer. Thus, the quantization error injected into the $\Delta\Sigma$ modulator loop by the DCMR quantizer is

$$\frac{1}{48} \leq \frac{1}{4} \cdot E\{e_{q_d}^2\} \leq \frac{1}{12}.$$

The maximum quantization error power occurs for $\left\langle \frac{4v_{cm}}{\Delta} \right\rangle = 0$ and the minimum occurs for $\left\langle \frac{4v_{cm}}{\Delta} \right\rangle = \frac{1}{2}$.

Behavioral simulation results for the $\Delta\Sigma$ modulator of Figure 4.1 support these analytical results. The $\Delta\Sigma$ modulator was run for 67 million samples, which is equivalent to 21 seconds of operation at a 3.072-MHz clock rate. Figure 4.18–Figure 4.20 show simulated probability densities for $(e_{q_+}[n], e_{q_+}[n+1])$, $(e_{q_-}[n], e_{q_-}[n+1])$, and $(e_{q_d}[n], e_{q_d}[n+1])$ created by taking a histogram of the quantization errors over the entire simulation run. For all values of $v_{cm}$, the distribution of $(e_{q_+}[n], e_{q_+}[n+1])$ is consistent with that of two independent, uniformly-distributed random variables

over $(-\frac{1}{2}, \frac{1}{2}]$. This supports the analytical results that $e_{q+}[n]$ converges to a uniformly distributed random variable distributed on $(-\frac{1}{2}, \frac{1}{2}]$ and that $e_{q+}[n]$ is independent of $e_{q+}[n+1]$. The same results hold for $(e_{q-}[n], e_{q-}[n+1])$ because the roles of the positive and negative flash ADCs could be reversed in the preceding analysis.

Note that the simulated probability densities for $(e_{q_d}[n], e_{q_d}[n+1])$ shown in Figure 4.18c–Figure 4.20c are consistent with those of pairs of independent random variables with marginal probability densities given by (10). For $\langle \frac{4v_{cm}}{\Delta} \rangle = 0$, $e_{q_d}[n]$ has a uniform distribution over $(-1, 1]$, and for $\langle \frac{4v_{cm}}{\Delta} \rangle = \frac{1}{2}$, $e_{q_d}[n]$ has a uniform distribution over $(-\frac{1}{2}, \frac{1}{2}]$. For $\langle \frac{4v_{cm}}{\Delta} \rangle = \frac{1}{4}$, shown in Figure 4.19c, the joint probability density is the product of two identical distributions given by (10). These results support the analysis that shows the quantization error injected by the DCMR flash ADC at time $n$ and $n+1$ are asymptotically independent.

## NOISE-SHAPED REQUANTIZER

As indicated by (5), the DCMR flash ADC implements a quantizer with step size $\Delta$ followed by a gain of two. Therefore, a gain of $\frac{1}{2}$ is required to obtain an overall quantizer gain of $\frac{1}{\Delta}$. As seen in Figure 4.11c, the DCMR flash ADC takes on only even values when $v_{cm} = 0$. In this case, the gain of $\frac{1}{2}$ could be implemented by truncating the LSB. However when common-mode noise is present, as in Figure 4.12c, the output takes on even and odd values, and truncation alone results in additional quantization error.

The requantization circuit shown in Figure 4.6 reduces the 65-level signal, $y_d[n]$, to a 33-level signal, $y[n]$, by adding a signal, $s[n]$, before truncating the LSB, where

$$s[n] = \begin{cases} \pm 1 & y_d[n] \text{ odd,} \\ 0 & y_d[n] \text{ even.} \end{cases} \tag{12}$$

This implies that the error due to requantization, $e_r[n]$, is

$$e_r[n] = \frac{s[n]}{2}.$$

Therefore, the power spectrum of of $e_r[n]$ can be spectrally shaped through the appropriate choice of $s[n]$. By choosing the $\pm 1$ randomly when $y_d[n]$ is odd, the requantization error can be made to have a white power spectrum. Alternatively, the requantization error can be spectrally shaped out of the signal passband by making $s[n]$ a first-order spectrally-shaped sequence obeying (12). This is a more appropriate choice in an oversampled ADC. Therefore, the dithered first-order switching block from the mismatch-shaping DAC encoder of [4] was used to generate $s[n]$. As a result, the requantization error lies predominantly outside the signal band and is uncorrelated with the requantizer's input sequence[6].

Changing the DCMR flash ADC's input by $\Delta$ does not change the parity of the quantization error because (2) and (4) are periodic functions of $v_{in}$ with period $\Delta$. Thus, the requantizer can also be moved outside the $G(z)$ feedback loop as shown in Figure 4.11c. Given a common-mode signal, $v_{cm}[n]$, the total noise power injected by the DCMR flash ADC and requantizer, $e_q^2[n]$, is therefore:

$$\mathrm{E}\{e_q^2[n]\} = \frac{1}{4} \cdot \mathrm{E}\{e_{q_d}^2[n]\} + \mathrm{E}\{e_r^2[n]\},$$

where $\mathrm{E}\{e_{q_d}^2[n]\}$ is given by (11). As indicated by the simulation results and the measured results from the $\Delta\Sigma$ modulator prototype, the combination of the DCMR flash ADC and noise-shaped requantizer provide equivalent 33-level quantization even in the presence of significant common-mode noise. The effect of the noise-shaped requantizer can be seen in the simulated and measured results where common-mode noise is present. The slightly elevated noise power near $\frac{F_s}{2}$, in Figure 4.7d and Figure 4.8b is due to requantization of odd values at the DCMR flash ADC output.
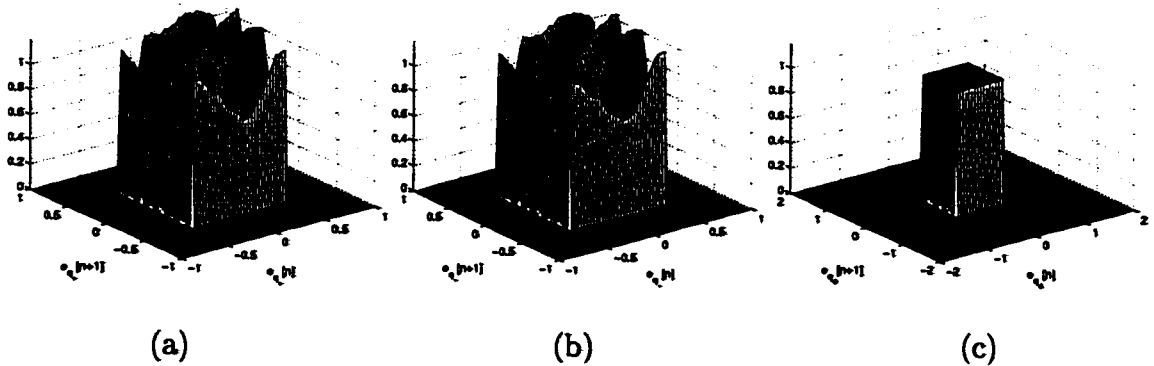
(a)                     (b)                     (c)

Figure 4.21: Simulated probability densities with no requantizer, 65-level feedback for $v_{cm} = \frac{\Delta}{8}$: (a) $(e_{q_+}[n], e_{q_+}[n+1])$, (b) $(e_{q_-}[n], e_{q_-}[n+1])$, (c) $(e_{q_d}[n], e_{q_d}[n+1])$.



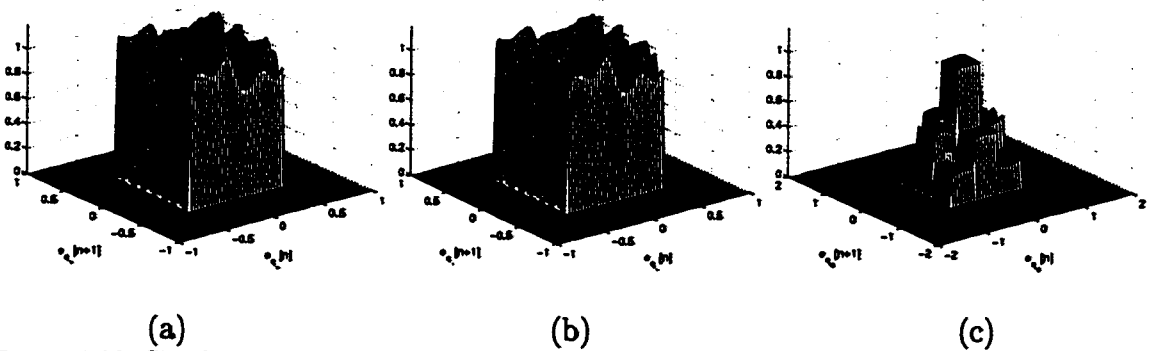(a)                     (b)                     (c)

Figure 4.22: Simulated probability densities with no requantizer and 65-level feedback for $v_{cm} = \frac{\Delta}{16}$: (a) $(e_{q_+}[n], e_{q_+}[n+1])$, (b) $(e_{q_-}[n], e_{q_-}[n+1])$, (c) $(e_{q_d}[n], e_{q_d}[n+1])$.

Because (11) implies that a deliberately introduced common-mode offset can reduce the power of the quantization error by 6 dB, an interesting question is whether a pair of 33-level flash ADCs with $v_{cm} = \frac{\Delta}{8}$ could be used to implement 65-level quantization with a 65-level feedback DAC. Without the requantizer, it seems this approach would yield a one-bit improvement in signal-to-quantization-noise ratio.

Unfortunately, this arrangement violates one of the assumptions used to move the quantizer outside the $G(z)$ feedback loop and prove that the quantization error becomes asymptotically white. With 65-level feedback and 33-level positive and negative flash ADCs, the $G(z)$ feedback signal in Figure 4.16 is no longer an integer

multiple of the flash ADCs' step size. In this case, the $G(z)$ feedback signal does affect the quantization error, and the quantizers must be analyzed within the $G(z)$ feedback loop.

Simulation results shown in Figure 4.21 for the $\Delta\Sigma$ modulator with 65-level feedback and no requantizer indicate that for $v_{cm} = \frac{\Delta}{8}$, the DCMR flash ADC's quantization error is white despite the fact that the quantization error sequences of the individual flash ADCs are not white. However as shown in Figure 4.22 for $v_{cm} = \frac{\Delta}{16}$, the surface of the joint distribution of $(e_{q_d}[n], e_{q_d}[n+1])$ has "waves" on its surface indicating that $e_{q_d}[n+1]$ depends on the value of $e_{q_d}[n]$. This effect cancels in the distribution of $(e_{q_d}[n], e_{q_d}[n+1])$ only if $v_{cm}$ is exactly $\frac{\Delta}{8}$. If this condition could be achieved, this technique would be useful, though common-mode offset or noise will lead to spurious tones in the $\Delta\Sigma$ modulator's output.

## IV. CONCLUSION

A digital common-mode rejection (DCMR) technique with noise-shaped requantization has been presented for implementing an area-efficient, differential input flash ADC and has been demonstrated in the context of a multibit ADC $\Delta\Sigma$ modulator. The use of digital common-mode rejection avoids the die area penalty and circuit design challenges of analog common-mode rejection techniques in a 3.3-V, single-poly CMOS fabrication process. Simulation results and measured performance of the ADC $\Delta\Sigma$ modulator IC prototype demonstrate that the DCMR flash ADC provides high common-mode rejection and enables the $\Delta\Sigma$ modulator to achieve an SFDR of 105 dB.

Analysis of the DCMR flash ADC shows that it can be viewed as a conventional quantizer followed by a memoryless transfer function which transforms the quantization error probability density. Previously derived results in [11] are applied to

show that the quantization error is asymptotically a sequence of pairwise indepen-
dent random variables and that the quantization error power is actually reduced
by a nonzero common-mode voltage. Thus, the 33-level DCMR flash ADC does
not introduce spurious tones in the presence of common-mode noise, and its quan-
tization error power is less than or equal to that of a conventional 33-level flash
ADC. The noise-shaped requantizer reduces the 65-level DCMR output signal to a
33-level signal and causes the requantization error to lie predominantly outside the
signal band.

## APPENDIX

This Appendix presents a derivation of the properties of the positive flash ADC's
quantization error referenced in section III using the theorems proven in [11]. The
$\Delta\Sigma$ modulator shown in Figure 4.16 is considered with $F(z)$ and $G(z)$ given by (8)
and (9), respectively. Let the input to the $\Delta\Sigma$ modulator be $x[n] = x_d[n] + \eta[n]$,
where $x_d[n]$ is the desired input signal and $\eta[n]$ is an i.i.d. noise sequence. The noise
sequence $\eta[n]$ models the thermal noise present at the input of any practical ADC
$\Delta\Sigma$ modulator. The results presented below hold no matter how low the power of
the thermal noise. Let $a$ represent the time at which the $\Delta\Sigma$ modulator is started
with zero initial conditions, and let $x[n] = 0$ for $n < a$.

Claim 1: The following conditions hold for the $\Delta\Sigma$ modulator of Figure 4.16 with
the DCMR flash ADC and requantizer where $F(z)$ is given by (8) and $G(z)$ is given
by (9):

1. The positive flash ADC behaves as a uniform, mid-step quantizer with quanti-
   zation step size $\Delta$.

2. The impulse response of $G(z)$ is integer-valued for all $n$.

3. The impulse response of $F(z)$ does not converge to zero as $n \to \infty$.

4. For each $p \neq 0$, the sequence $t_0 f[n] + t_1 f[n+p]$ does not converge to zero as $n \to \infty$ for any nonzero $(t_0, t_1)$.

**Proof:** By design, the positive flash ADC is a uniform, mid-step quantizer with step size $\frac{\Delta}{2}$. As shown in Figure 4.16, the requantizer's gain of $\frac{1}{2}$ cancels the gain of two in the DCMR flash ADC and makes the effective quantization gain $\frac{1}{\Delta}$. Thus, the positive flash ADC can be viewed as a uniform mid-step quantizer with step size $\Delta$.

The impulse response of $G(z)$ is $g[n] = (3 - n)u[n]$, where

$$u[n] = \begin{cases} 1 & n \geq 0, \\ 0 & \text{otherwise.} \end{cases}$$

Thus, $g[n]$ is integer-valued for all $n$.

The impulse response of $F(z)$ is $f[n] = (n-1)u[n-2]$. Thus it does not converge to zero as $n \to \infty$. Let $z[n] = t_0 f[n] + t_1 f[n+p]$ for $p \neq 0$. For $n > \max(2, 2-p)$,

$$z[n] = (t_0 + t_1)(n - 1) + t_1 p.$$

Therefore, $(t_0, t_1) \neq (0, 0)$ implies $z[n]$ does not converge to 0.

∎

**Theorem 1:** For each pair of integers $n_1$, $n_2$, $(e_{q+}[n_1], x[n_2])$ converges in distribution to $(e'_{q+}[n_1], x[n_2])$ as $a \to -\infty$, where $e'_{q+}[n_1]$ and $x[n_2]$ are independent and $e'_{q+}[n_1]$ is uniformly distributed on $(-\frac{1}{2}, \frac{1}{2}]$.

If $n_1 \neq n_2$ and part 4 of Claim 1 holds, then $(e_{q+}[n_1], e_{q+}[n_2])$ converges in distribution to $(e'_{q+}[n_1], e'_{q+}[n_2])$ as $a \to -\infty$, where $e'_{q+}[n_1]$ and $e'_{q+}[n_2]$ are independent.

**Proof:** Let $e_{q_+}[n_1] = \frac{1}{2} - U_{n_1-a}$, where

$$U_p = \left\langle \mu_p + \sum_{m=0}^{p} c_m \alpha_m \right\rangle,$$

$$\mu_p = \frac{2c[p+a]}{\Delta} + \frac{1}{2} + \frac{1}{\Delta} \sum_{m=0}^{p} f[m] x_d[p+a-m],$$

$$c_m = \frac{f[m]}{\Delta}, \qquad \alpha_m = \eta[p+a-m].$$

Define

$$V_p = \left\langle \nu_p + \sum_{m=0}^{p} d_m \alpha_m \right\rangle, \quad \nu_p = 0, \quad d_m = c_m^2.$$

By condition 3 of Claim 1, $\lim_{m\to\infty} f[m] \neq 0$. This implies $\{t_0 c_m + t_1 d_m\} \not\to 0$ unless $(t_0, t_1) = (0,0)$. Therefore, $U_p$ and $V_p$ satisfy the hypotheses of Lemmas A1 and A2 of [11] and

$$\left( e_{q_+}[n_1] x[n_2] \right) \to \left( \frac{1}{2} - U, x[n_2] \right),$$

where $U$ and $x[n_2]$ are independent and $U$ is uniformly distributed on $[0,1)$. Therefore, $e'_{q_+}[n_1] = \frac{1}{2} - U$ and is uniformly distributed on $(-\frac{1}{2}, \frac{1}{2}]$.

To prove the second result, let $e_{q_+}[n_1]$ be defined as above. Let $e_{q_+}[n_2] = \frac{1}{2} - V_{n_2-a}$, where

$$V_p = \left\langle \nu_p + \sum_{m=0}^{p} d_m \alpha_m \right\rangle,$$

$$\nu_p = \frac{2c[p+a]}{\Delta} + \frac{1}{2} + \frac{1}{\Delta} \sum_{m=0}^{p} f[m] x_d[p+a-m],$$

$$d_m = \frac{f[m]}{\Delta}, \quad \alpha[m] = \eta[p+a-m].$$

As above, $\{t_0 c_m + t_1 d_m\} \not\to 0$ unless $(t_0, t_1) = (0,0)$. Therefore, $U_p$ and $V_p$ satisfy the hypotheses of Lemma A1 and

$$\left( e_{q_+}[n_1] e_{q_+}[n_2] \right) \to \left( \frac{1}{2} - U, \frac{1}{2} - V \right),$$

where $U$ and $V$ are independent.

■

**Corollary 2:**

$$R_{e_{q+}e_{q+}}[n,m] = \lim_{a \to -\infty} E\{e_{q+}[n]e_{q+}[n+m]\} = \frac{1}{12}\delta[m],$$

$$R_{x_d e_{q+}}[n,m] = \lim_{a \to -\infty} E\{x_d[n]e_{q+}[n+m]\} = 0.$$

The final theorem shows that the statistical averages in Corollary 2 converge to the corresponding time averages. In particular, for each $m$, the time averages of $e_{q+}[n]$, $e_{q+}[n]x_d[n+m]$, and $e_{q+}[n]e_{q+}[n+m]$ converge in probability to their corresponding statistical averages.

**Theorem 3:** As $N \to \infty$,

$$\frac{1}{N}\sum_{n=0}^{N-1} e_{q+}[n] \to 0 \qquad \frac{1}{N}\sum_{n=0}^{N-1} x_d[n]e_{q+}[n+m] \to R_{e_{q+}e_{q+}}[m].$$

If part 4 of Claim 1 holds, then

$$\frac{1}{N}\sum_{n-0}^{N-1} e_{q+}[n]e_{q+}[n+m] \to \frac{1}{12}\delta[m].$$

**Proof:** Proof is identical to that presented for Theorem 3 in [11].

■

## CHAPTER ACKNOWLEDGMENT

*and Digital Signal Processing.* The dissertation author was the primary researcher. Ian Galton supervised the research which forms the basis of the chapter.

## REFERENCES

1. S. H. Lewis, P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits,* vol. SC-22, no. 6, pp. 954-961, Dec. 1987.

2. T. Shih, L. Der, S. H. Lewis, and P. J. Hurst, "A fully differential comparator using a switched-capacitor differencing circuit with common-mode rejection," *IEEE J. Solid-State Circuits,* vol. 32, no. 2, pp. 250-253, Feb. 1997.

3. E. Säckinger, W. Güggenbuhl, "A versatile building block: the CMOS differential difference amplifier," *IEEE J. Solid State Circuits,* vol. SC-22, no. 2, pp. 287-294, April 1987.

4. E. Fogleman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB peak SFDR," *IEEE J. Solid-State Circuits,* vol. 35, no. 3, pp. 297-307, March 2000.

5. E. Fogleman, J. Welz, and I. Galton, "An audio ADC delta-sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC," in *IEEE Custom Integrated Circuits Conf.,* May 2000, pp. 17-20.

6. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II,* vol. 44, no. 10, pp. 808-817, Oct. 1997.

7. E. Fogleman, I. Galton, and H. Jensen, "An area-efficient differential input ADC with digital common mode rejection," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 2 of 6, June 1999, pp. 347-350.

8. E. Fogleman, I. Galton, and H. Jensen, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADCs," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 2 of 6, June 1999, pp. 290-293.

9. B. P. Brandt, B. A. Wooley, "A 50 MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion," *IEEE J. Solid-State Circuits,* vol. 26, no. 12, pp. 1746-1756, Dec. 1991.

10. Y. Geerts, M. Steyaert, W. Sansen, "A 2.5MSample/s multi-bit $\Delta\Sigma$ CMOS ADC with 95dB SNR," in *IEEE ISSCC Dig. Tech. Papers,* vol. 43, Feb. 2000, pp. 336-337.

11. I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inform. Theory*, vol. 40, no. 3, pp. 848-859, May 1994.

12. E. Fogleman and I. Galton, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADCs," in preparation: *IEEE Trans. Circuits Syst. II*.

13. G. Lainey, R. Saintlaurens, and P. Senn, "Switched-capacitor second-order noise-shaping coder," *Electron. Lett.*, vol. 19, pp. 149-150, Feb. 1983.