31.9 A 14b 100MS/s DAC with Fully Segmented Dynamic Element Matching

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A 14b 100MS/s Nyquist-rate DAC is demonstrated that achieves high linearity across its Nyquist band enabled by a DEM technique called fully segmented DEM (FSDEM). In contrast to previous high-resolution DACs wherein DEM, trimming, calibration, or special layout techniques are applied just to a subset of large current steering DAC elements [1, 2, 3, 4], harmonic distortion from pulse-shape and timing mismatches among DAC elements is avoided because FSDEM manipulates all the DAC elements simultaneously. This relaxes several design and layout constraints on the current steering circuits. Unlike previous DEM techniques, the complexity of FSDEM does not grow exponentially with resolution; therefore, involving all the DAC elements in the proposed DEM algorithm is practical.

As shown in Fig. 31.9.1, the DAC contains 28 1b *DAC elements* each of which consists of a switch driver and a weighted current-steering (CS) cell. During the nth sample interval, $nT_s \le t < (n+1)T_s$, the differential output current from the rth DAC element is either $A_r\Delta_{pos\ r}(t-nT_s)/2$ or $-A_r\Delta_{neg\ r}(t-nT_s)/2$ depending on the value of $x_r[n]$, where A_r is the CS cell *weighting factor* (i.e., $A_1 = A_2 = 8192$, $A_3 = A_4 = 4096$, etc.), and $\Delta_{pos\ r}(t)$ and $\Delta_{neg\ r}(t)$ are return-to-zero (RZ) pulses that are zero for $t < 0$ and $t \ge T_s$. The RZ pulses are modeled as $\Delta_{pos\ r}(t) = \Delta(t) + e_{pos\ r}(t)$ and $\Delta_{neg\ r}(t) = \Delta(t) + e_{neg\ r}(t)$, where $\Delta(t)$ is the *ideal LSB DAC pulse* and $e_{pos\ r}(t)$ and $e_{neg\ r}(t)$ are *DAC element mismatch pulses* caused by DAC element pulse shape, timing, and amplitude errors.

The purpose of the FSDEM encoder is to make the error introduced by the DAC element mismatch pulses and the desired signal uncorrelated and thereby avoiding harmonic distortion. For each DAC input sample, $x[n]$, where $x[n]$ is an integer between –8192 and 8192, there are multiple sets of 28 DAC element input bits that would yield the correct overall DAC output pulse in the absence of DAC element mismatch pulses. At each sample time, the FSDEM encoder chooses one of these sets pseudo-randomly. The functional details are shown in Fig. 31.9.2. The FSDEM encoder consists of a tree of digital *switching blocks* that each use a pseudo-random sequence, $s_{k,r}[n]$, called the *switching sequence,* to calculate its two output sequences. By design, the switching sequences are uncorrelated with $x[n]$ and each other, and are white.

It can be shown that the differential output current of the DAC for $nT_s \le t < (n+1)T_s$ is

$$I_{out}(t) = \alpha(t - nT_s)x[n] + \beta(t - nT_s) + e(n, t - nT_s),$$

where $\alpha(t)$, $\beta(t)$, and $e(n, t)$ are RZ pulses that depend on the DAC element mismatch pulses. Both $\alpha(t)$ and $\beta(t)$ are signal-independent, so they do not introduce noise or harmonic distortion. The $e(n, t)$ term has the form

$$e(n,t) = \Delta_{1,1}(t)s_{1,1}[n] + \sum_{i=2}^{14}\left(\Delta_{i,1}(t)s_{i,1}[n] + \Delta_{1,i}(t)s_{1,i}[n]\right),$$

where the $\Delta_{k,r}(t)$ terms are signal-independent RZ pulses that depend only on the DAC element mismatch pulses. Hence, $e(n,t)$ is an RZ pulse whose shape during each sample interval depends on the switching sequences. The train of these pulses in $I_{out}(t)$ is called DAC noise. The above-mentioned switching sequence properties ensure that the DAC noise is uncorrelated with the signal, and that the nth DAC noise pulse is uncorrelated from the mth DAC noise pulse for every $n \ne m$.

Consequently, DAC element pulse shape, timing, and amplitude mismatches and the glitches they cause do not introduce harmonic distortion. This eases several circuit design issues because linearity no longer depends on good component matching and low glitch power; mismatch becomes a secondary concern so the DAC elements can be optimized for low parasitic capacitance and high output impedance to improve linearity at high frequencies. It also obviates the need for glitch reduction techniques such as having a single high-linearity RZ switch circuit following the summed CS cell outputs [5]. Instead, each DAC element in the present design contains its own RZ switch driver. Furthermore, as indicated in Fig. 31.9.1, the switch drivers are not even scaled linearly with the CS cell weights; this property saves circuit area. Without FSDEM, this alone would have seriously degraded the linearity of the DAC. Despite these benefits there is a drawback to FSDEM: twice the number of CS cells are required relative to a 14b binary-weighted DAC. Hence, FSDEM is most appropriate for applications in which maximizing linearity is more critical than minimizing current consumption.

A simplified circuit diagram of one of the 28 DAC elements is shown in Fig. 31.9.3. It consists of a switch driver and a CS cell. The switch driver consists of a flip-flop to retime the $x_r[n]$ bit and NAND gates to generate the CS cell switch signals. The CS cell is a pMOS cascode current source with current steering switches. The non-overlapping two-phase clock signal and NAND gate circuitry are designed to achieve a low current-steering crossover point. The RZ design ensures signal-independent switch driver activity and DAC element supply current. The remaining dominant sources of high-frequency CS cell nonlinearity are nonlinear capacitances associated with the common source nodes of the switches, and nonlinear, finite current source output impedances [1]. The CS cell circuits are designed and laid out to minimize these sources of nonlinearity without considering the matching.

The DAC is fabricated in a 0.18μm CMOS process and is packaged in a QFN 64 package with ground down-bonding. The emphasis of the floor plan is to ensure that the coupling from digital to analog circuits is minimized or data-independent. Wide supply and ground lines, and multiple supply pins with double bonding are used to minimize parasitic resistance and inductance in the supply lines. All ground lines are down-bonded to the exposed paddle of the QFN package to reduce parasitic inductance. ESD protection is implemented on all pads of the IC.

For testing the DAC its output is differentially coupled to a spectrum analyzer through a wideband transformer. The measured SFDR of the DAC versus input frequency is shown Fig. 31.9.4, and representative PSD plots with and without FSDEM enabled are shown in Fig. 31.9.5. With FSDEM enabled, the worst-case SFDR values across the Nyquist bands are 74.4dB and 78.9dB for sample-rates of 100MS/s and 70MS/s, respectively. As expected, and in contrast to other high-resolution DACs, the measured SFDR values show little dependence on signal frequency. With FSDEM disabled, these values drop to less than 54dB which is expected given the lack of attention paid to the DAC element matching. A full performance summary and the die micrograph are shown in Figs. 31.9.6 and 31.9.7.

References:

[1] W. Schofield et al., "A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz Noise Power Spectral Density," *ISSCC Dig. Tech. Papers,* pp. 126-127, Feb., 2003.

[2] B. Jewett et al., "A 1.2 GS/s 15b DAC for Precision Signal Generation," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2005.

[3] J. Hyde et al., "A 300-MS/s 14-bit Digital-to-Analog Converter in Logic CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no, 5, pp. 734-740, May, 2003.

[4] G. A. M. Van-Der-Plas et al., "A 14-bit Intrinsic Accuracy Q² Random Walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1708-1718, Dec., 1999.

[5] Q. Huang et al., "A 200MS/s 14b 97mW DAC in 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 364-365, Feb., 2004.

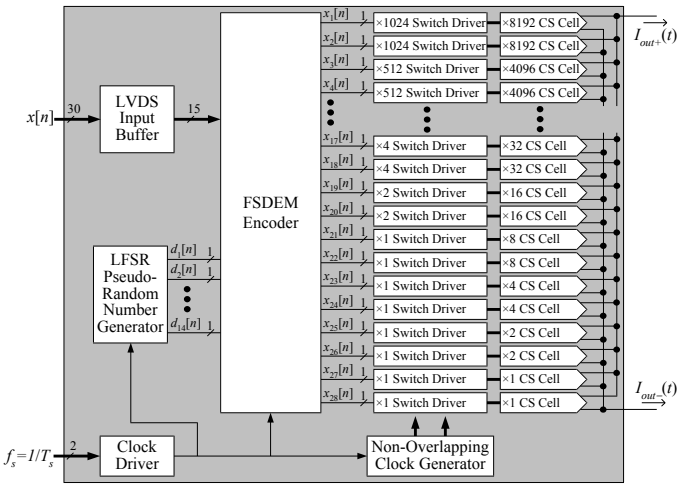


Figure 31.9.1: Block diagram of the DAC.

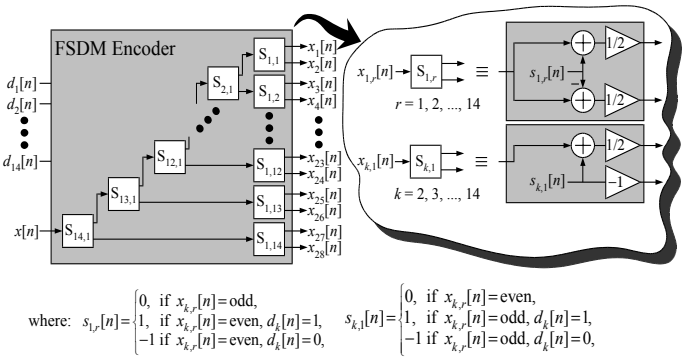


Figure 31.9.2: Signal processing details of the FSDEM encoder.

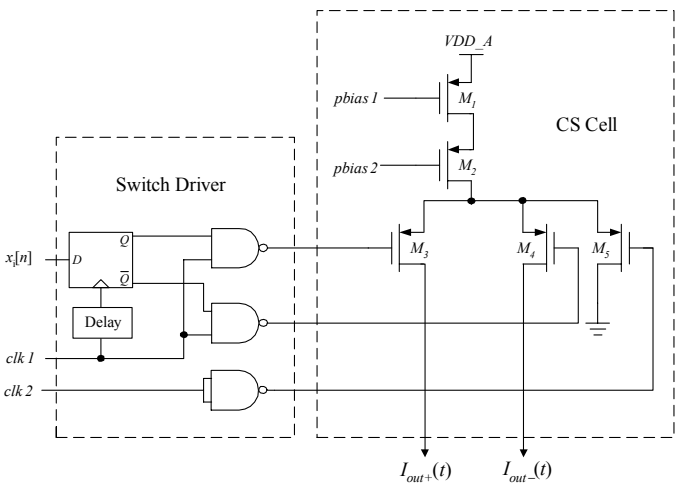


Figure 31.9.3: DAC element circuit details.

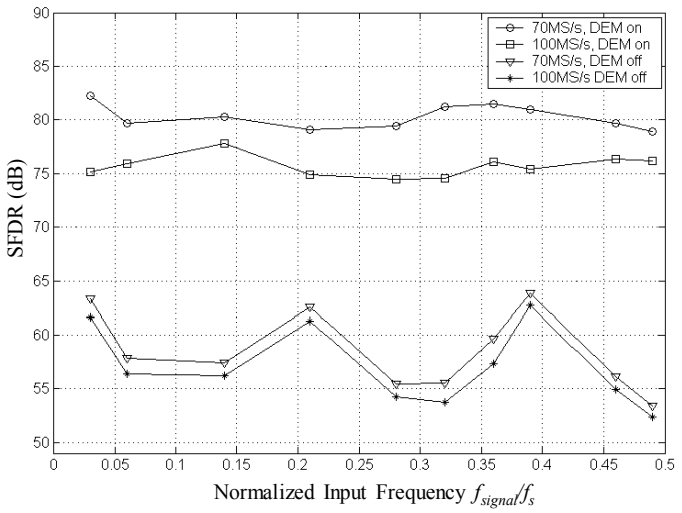


Figure 31.9.4: Measured SFDR versus frequency.

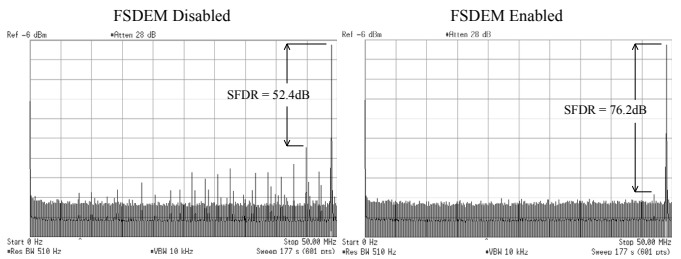


Figure 31.9.5: Representative measured PSD plots.

Technology	TSMC 0.18μm CMOS
Update Rate	100MS/s
Package	QFN 64 with exposed paddle
Single-Tone SFDR @ 70MS/s, 0dBFS	78.9 to 82.3dB across Nyquist
Single-Tone SFDR @ 100MS/s, 0dBFS	74.4 to 77.8dB across Nyquist
Two-Tone SFDR @ 100MS/s, -6dBFS	82.1dB, $f_{signal\ 1}$=13.97MHz, $f_{signal\ 2}$=14.94MHz 82.8dB, $f_{signal\ 1}$=27.98MHz, $f_{signal\ 2}$=28.95MHz 80.6dB, $f_{signal\ 1}$=45.99MHz, $f_{signal\ 2}$=46.97MHz
Full-Scale Current	16mA
Supply Voltages	Analog: 1.8V; Digital: 2.3V
Current Consumption @ 100MS/s	Analog: 30mA; Digital: 53.5mA
Area (including bond pads)	4.8mm x 2.4mm
Active Area	3.18mm^2

Figure 31.9.6: Performance summary.

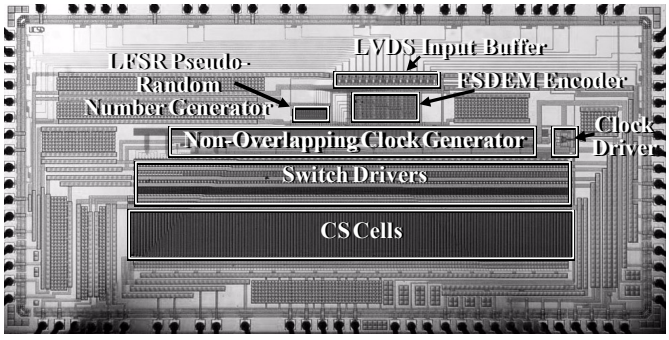
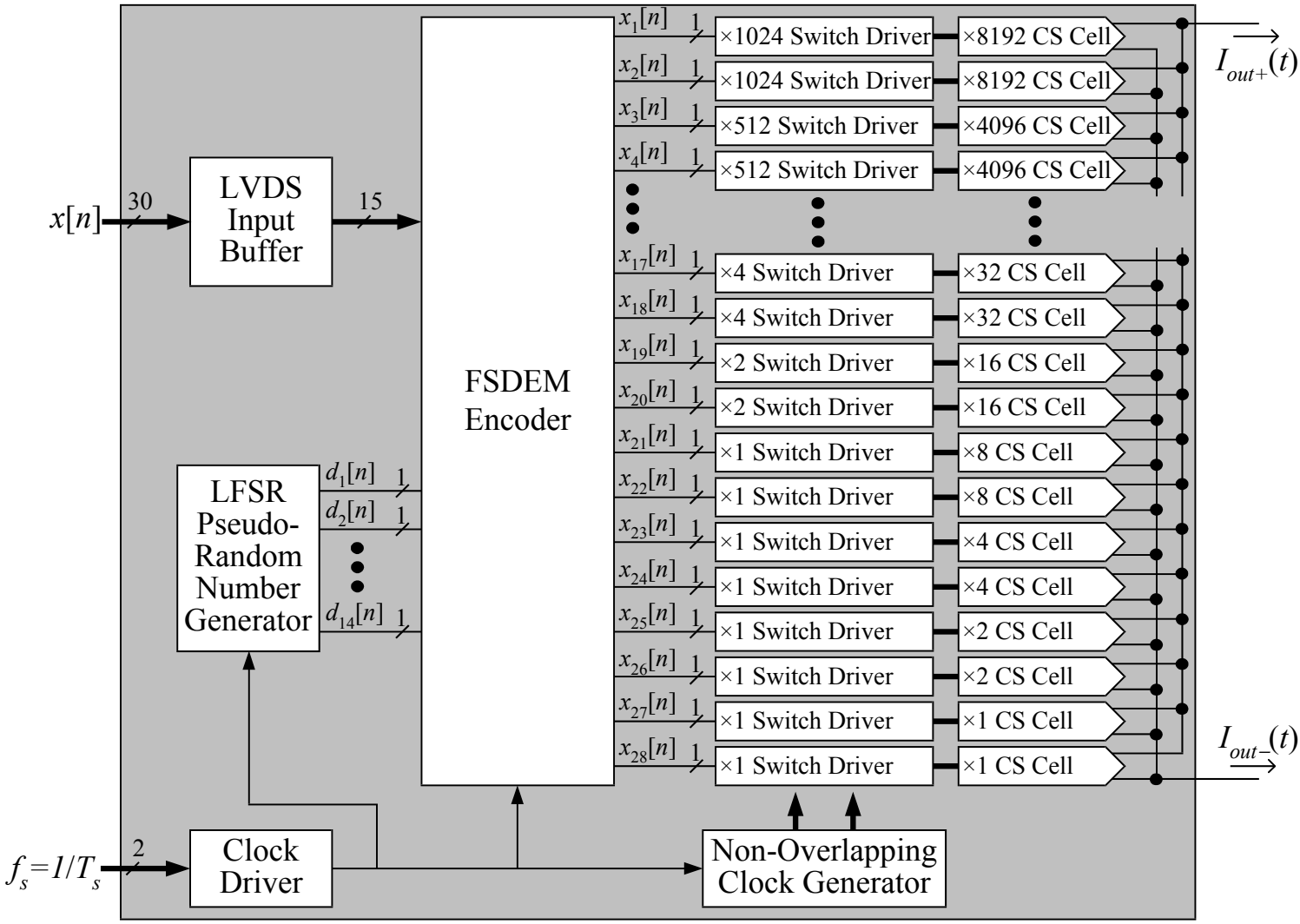


Figure 31.9.7: Die micrograph.



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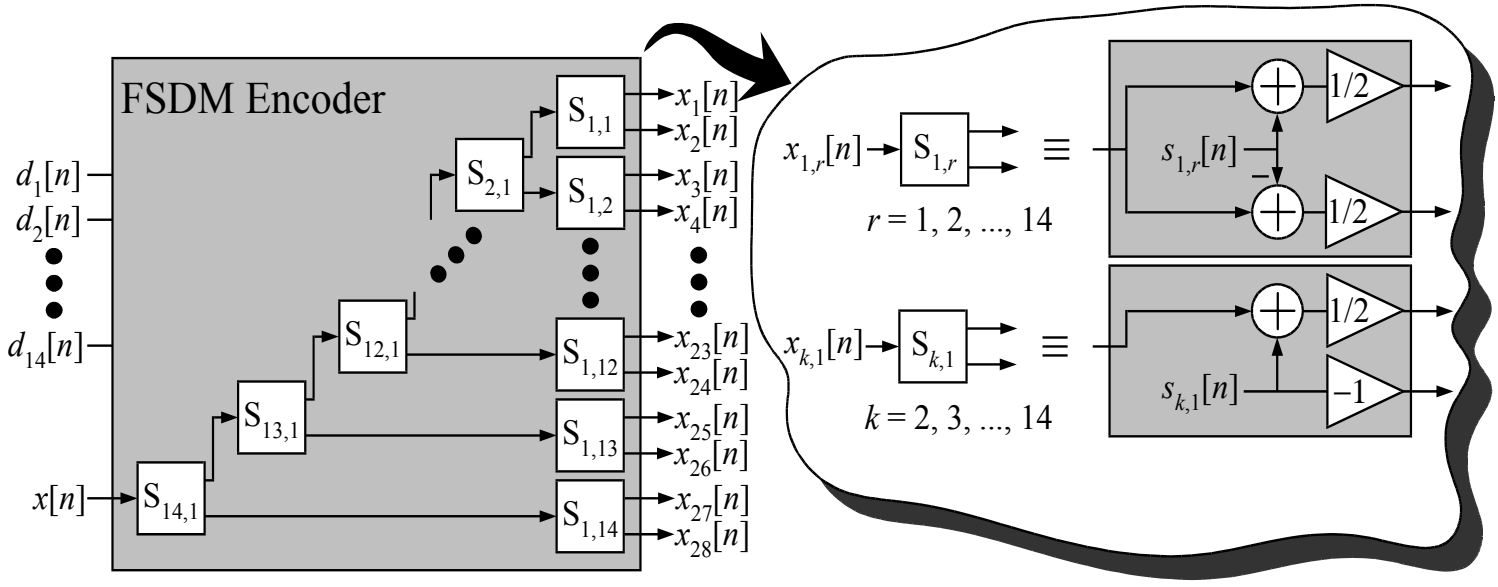

$$\text{where: } s_{1,r}[n]=\begin{cases}0, & \text{if } x_{k,r}[n]=\text{odd},\\ 1, & \text{if } x_{k,r}[n]=\text{even},\ d_k[n]=1,\\ -1 & \text{if } x_{k,r}[n]=\text{even},\ d_k[n]=0,\end{cases} \qquad s_{k,1}[n]=\begin{cases}0, & \text{if } x_{k,r}[n]=\text{even},\\ 1, & \text{if } x_{k,r}[n]=\text{odd},\ d_k[n]=1,\\ -1 & \text{if } x_{k,r}[n]=\text{odd},\ d_k[n]=0,\end{cases}$$

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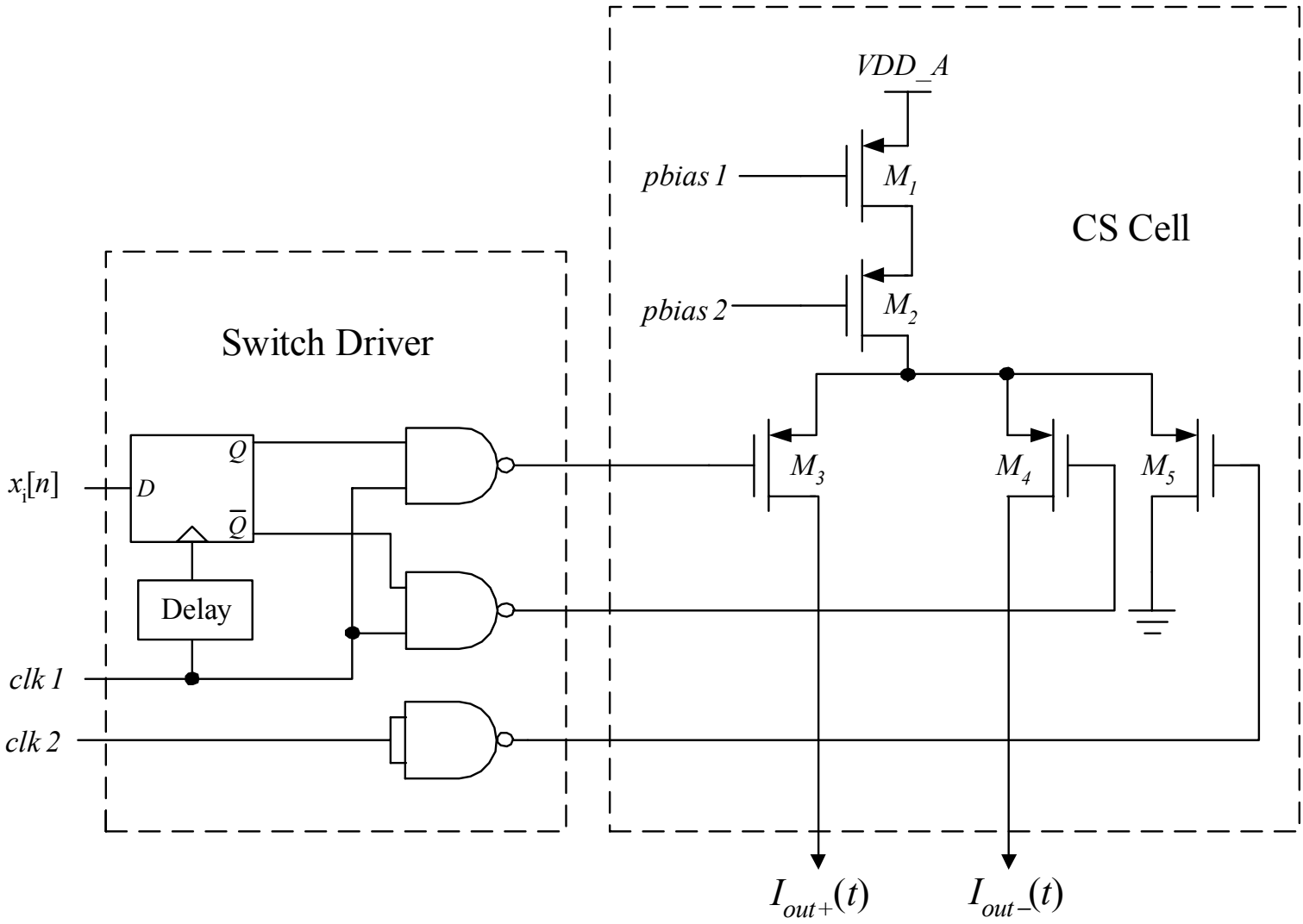

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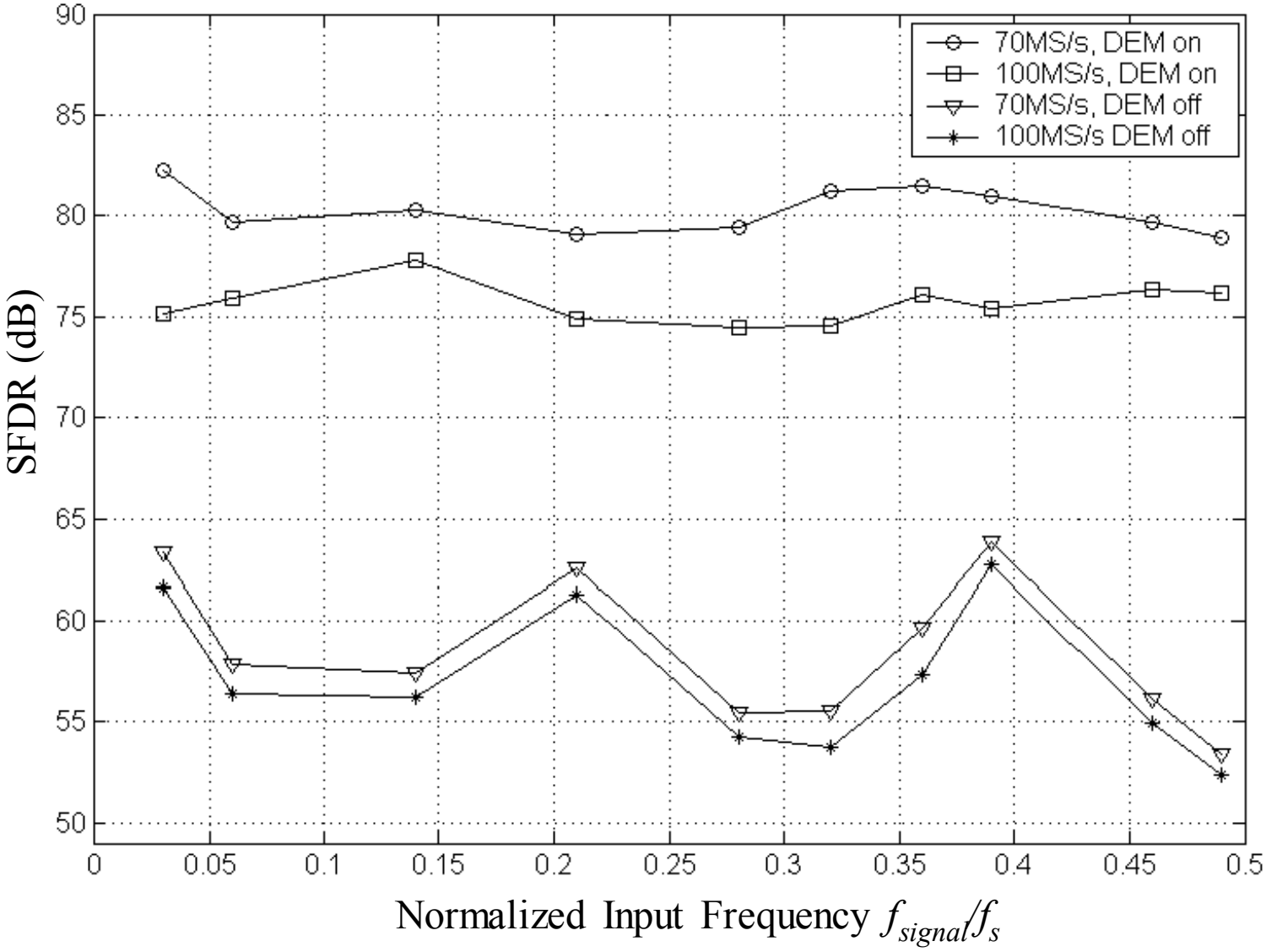

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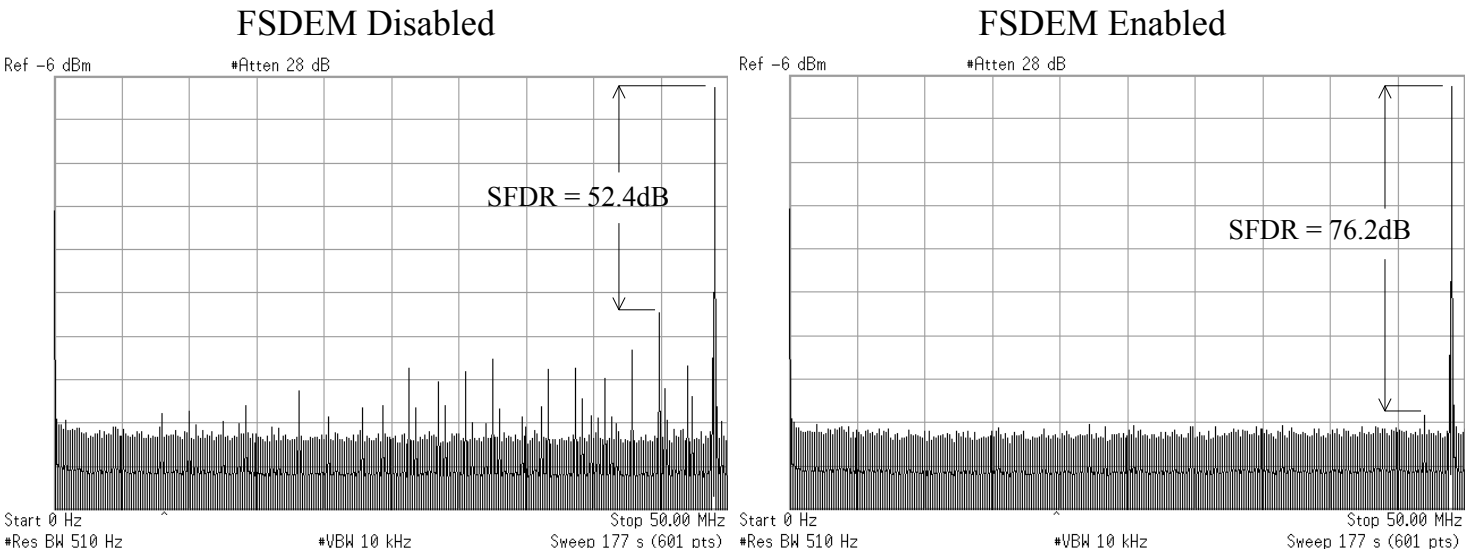

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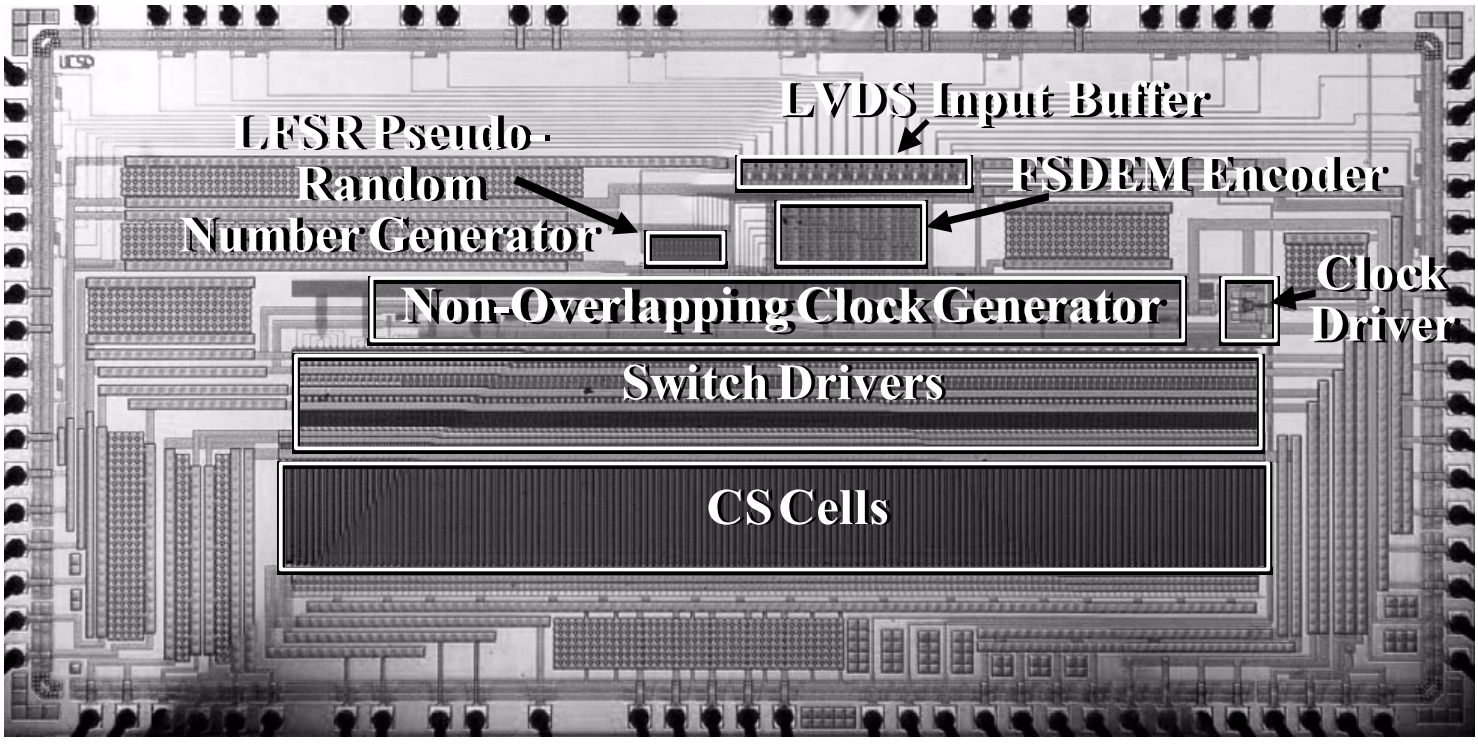

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