# Delta–Sigma Data Conversion in Wireless Transceivers

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*Invited Paper*

***Abstract*—High-performance analog-to-digital converters, digital-to-analog converters, and fractional-$N$ frequency synthesizers based on delta–sigma ($\Delta\Sigma$) modulation—collectively referred to as $\Delta\Sigma$ data converters—have contributed significantly to the high level of integration seen in recent commercial wireless handset transceivers. This paper presents a tutorial on $\Delta\Sigma$ data converters and their uses and implications with respect to wireless transceiver architectures.**

***Index Terms*—ADC, DAC, delta–sigma, fractional-$N$ PLL, sigma–delta, wireless transceiver.**

## I. Introduction

THE relentless progress in very large-scale integration (VLSI) silicon technology optimized for digital circuitry generally has made it economically advantageous to trade analog signal processing for digital signal processing wherever possible in wireless transceivers. However, shifting from analog to digital signal processing generally increases the burden on the *data converters* that provide the interfaces between the analog and digital circuits. For example, if it is desired that much of the channel filtering in the receiver be performed by digital filters, the digital filters must be preceded by analog-to-digital converters (ADCs) with sufficient dynamic range and bandwidth to digitize not only the desired signal but also the interfering signals to be removed by the digital filters. This creates a potential problem because high-performance data converters often require high-precision analog processing.

Fortunately, it is often the case that the bandwidth of an analog signal of interest in a wireless transceiver is narrow compared to practical data converter sample-rates and digital filter clock rates, so high analog precision only is necessary within the narrow band of interest. Delta–sigma data converters exploit this by converting between analog and digital formats at rates that are much higher than the bandwidth of the desired signal and employing noise shaping techniques that cause most of their analog circuit error to be spectrally shaped away from the band of interest. These techniques have made high-precision ADCs, digital-to-analog converters (DACs), and digitally controlled frequency synthesizers feasible in VLSI technology optimized for digital circuitry and have contributed significantly to the high level of integration enjoyed by modern commercial wireless transceivers.

This paper presents a tutorial on $\Delta\Sigma$ data converters and their application to wireless communication transceivers. It consists of two main sections. Section II presents a detailed overview of the principles underlying $\Delta\Sigma$ ADCs, $\Delta\Sigma$ DACs, mismatch-shaping DACs, and fractional-$N$ frequency synthesizers in the context of specific examples. Section III describes the key issues associated with data conversion for modulation and demodulation in wireless transceivers and shows, via numerous examples, how $\Delta\Sigma$ data converters have proven to be enabling components in highly integrated commercial handset transceivers.

## II. Overview of $\Delta\Sigma$ Data Conversion

The basic concept underlying $\Delta\Sigma$ data converters is that of using a coarse quantizer (e.g., a coarse ADC) within a feedback loop such that the power of the resulting quantization error is suppressed within some frequency band of interest. This technique is known as *quantization noise shaping* and is also referred to as *delta–sigma modulation* for historic reasons [1]. Devices that perform $\Delta\Sigma$ modulation are referred to as $\Delta\Sigma$ modulators. Delta–sigma modulators form the basis of $\Delta\Sigma$ ADCs, $\Delta\Sigma$ DACs, and an important class of fractional-$N$ phase-locked loops (PLLs). A closely related technique referred to as mismatch noise shaping is widely used to suppress in-band errors associated with component mismatches in DACs.

### A. Delta–Sigma Modulation

As mentioned above, a $\Delta\Sigma$ modulator performs coarse quantization in such a way that the inevitable error introduced by the quantization process, i.e., the *quantization noise*, is attenuated in a specific narrow frequency band of interest. There are many different $\Delta\Sigma$ modulator architectures, and, depending upon the application, each may be implemented as an all-digital circuit or a mixed-signal circuit. However, most $\Delta\Sigma$ modulators use coarse uniform quantizers to perform the quantization and use feedback around the quantizers to suppress the quantization noise in particular frequency bands. Therefore, to illustrate the $\Delta\Sigma$ modulator concept, a specific uniform quantizer example first is considered in isolation, and then a specific $\Delta\Sigma$ modulator architecture that incorporates the uniform quantizer is presented.

*1) An Example Uniform Quantizer:* The input–output characteristic of the example uniform quantizer is shown in Fig. 1. It

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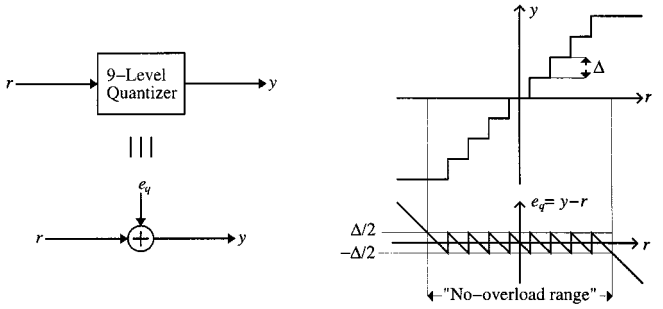


Fig. 1. Ideal nine-level uniform quantizer.

is a nine-level quantizer with a *quantization step-size* of $\Delta$. For each input value with a magnitude less than $9\Delta/2$, the quantizer generates the corresponding output sample by rounding the input value to the nearest multiple of $\Delta$. For each input value greater than $9\Delta/2$ or less than $-9\Delta/2$, the quantizer sets its output to $4\Delta$ or $-4\Delta$, respectively; such values are said to *overload* the quantizer. By defining the quantization noise as $e_q[n] = y[n] - r[n]$, the quantizer can be viewed without approximation as an additive noise source as illustrated in the figure.

To illustrate some properties of the example quantizer, consider a 48-Msample/s input sequence, $x[n]$, consisting of a 48-kHz sinusoid with an amplitude of $1.7\Delta$ plus a small amount of white noise such that the input signal-to-noise ratio (SNR) is 100 dB. Fig. 2(a) shows the power spectral density (PSD) plot of the resulting quantizer output sequence, and Fig. 2(b) shows a time-domain plot of the quantizer output sequence over two periods of the sinusoid. Given the coarseness of the quantization, it is not surprising that the quantizer output sequence is not a precise representation of the quantizer input sequence. As evident in Fig. 2(a), the quantization noise for this input sequence consists primarily of harmonic distortion as represented by the numerous spurious tones distributed over the entire discrete-time frequency band. Even in the relatively narrow frequency band below 500 kHz, significant harmonic distortion corrupts the desired signal. To illustrate this in the time domain, Fig. 2(c) shows the sequence obtained by passing the quantizer output sequence through a sharp lowpass discrete-time filter with a cutoff frequency of 500 kHz. The significant quantization noise power in the 0–500-kHz frequency band causes the sequence shown in Fig. 2(c) to deviate significantly from the sinusoidal quantizer input sequence.

*2) An Example $\Delta\Sigma$ Modulator:* The example $\Delta\Sigma$ modulator architecture shown in Fig. 3 can be used to circumvent this problem. The structure incorporates the same nine-level quantizer presented above, but in this case the quantizer is preceded by two delaying discrete-time integrators and surrounded by two feedback loops [2]. Each discrete-time integrator has a transfer function of $z^{-1}/(1 - z^{-1})$ which implies that its $n$th output sample is the sum of all its input samples for times $k < n$. With the quantizer represented as an additive noise source as depicted in Fig. 1, the $\Delta\Sigma$ modulator can be viewed as a two-input, single-output linear time-invariant discrete-time system. It is straightforward to verify that

$$y[n] = x[n-2] + e_{q\Delta\Sigma}[n] \tag{1}$$

where $e_{q\Delta\Sigma}[n]$ is the overall quantization noise of the $\Delta\Sigma$ modulator and is given by

$$e_{q\Delta\Sigma}[n] = e_q[n] - 2e_q[n-1] + e_q[n-2]. \tag{2}$$

To illustrate the behavior of the $\Delta\Sigma$ modulator, suppose that the same 48-Msample/s input sequence considered above is applied to the input of the $\Delta\Sigma$ modulator, and that the discrete-time integrators in the $\Delta\Sigma$ modulator are clocked at 48 MHz. Fig. 4(a) shows the PSD plot of the resulting $\Delta\Sigma$ modulator output sequence, $y[n]$, and Fig. 4(b) shows a time-domain plot of $y[n]$ over two periods of the sinusoid. Two important differences with respect to the uniform quantization example shown in Fig. 2 are apparent: the quantization noise PSD is significantly attenuated at low frequencies, and no spurious tones are visible anywhere in the discrete-time spectrum. For instance, the SNR in the 0–500-kHz frequency band is approximately 84 dB for this example as opposed to 14 dB for the uniform quantization example of Fig. 2.[1] Consequently, subjecting the $\Delta\Sigma$ modulator output sequence to a sharp lowpass filter with a cutoff frequency of 500 kHz results in a sequence that is very nearly equal to the $\Delta\Sigma$ modulator input sequence as demonstrated in Fig. 4(c).

Below about 120 kHz, the PSD shown in Fig. 4(a) is dominated by the two components of the $\Delta\Sigma$ modulator input sequence: the 48-kHz sinusoid component, and the input noise component. Above 120 kHz, the PSD is dominated by the $\Delta\Sigma$ modulator quantization noise, $e_{q\Delta\Sigma}[n]$, and rises with a slope of 40 dB per decade. It follows from (2) that $e_{q\Delta\Sigma}[n]$ can be viewed as the result of passing the additive noise from the quantizer, $e_q[n]$, through a discrete-time filter with transfer function $(1 - z^{-1})^2$. Since this filter has two zeros at dc, the smooth 40-dB per decade increase of the PSD of $e_{q\Delta\Sigma}[n]$ indicates that $e_q[n]$ is very nearly white noise, at least for the example shown in Fig. 4.

It can be proven that $e_q[n]$ is indeed white noise; it has a variance of $\Delta^2/12$ and is uncorrelated with the $\Delta\Sigma$ modulator input sequence [3]. Moreover, this situation holds in general for the example $\Delta\Sigma$ modulator architecture provided that the input sequence satisfies two conditions: the first condition is that its magnitude is sufficiently small that the quantizer within the $\Delta\Sigma$ modulator never overloads, and the second condition is that it consists of a signal component plus a small amount of independent white noise. It can be shown that the first condition is satisfied if the input signal is bounded in magnitude by $3\Delta$ [4]. Input sequences with values even slightly exceeding $3\Delta$ in magnitude generally cause the quantizer to overload with the result that $e_q[n]$ contains spurious tones, and the SNR in the frequency band of interest is degraded. For this reason, the range between $-3\Delta$ and $3\Delta$ is said to be the *input no-overload range* of the $\Delta\Sigma$ modulator. For the second condition to be satisfied, the power of the $\Delta\Sigma$ modulator input sequence's white noise component may be arbitrarily small, but if it is absent altogether $e_q[n]$ is not guaranteed to be white. For instance, in the example shown in Fig. 4 the input sequence contains a white noise component with 100 dB less power than the signal component. If this tiny noise component were not present, the resulting $\Delta\Sigma$ mod-

[1]In these cases, the noise to which the SNR refers is the quantization noise.

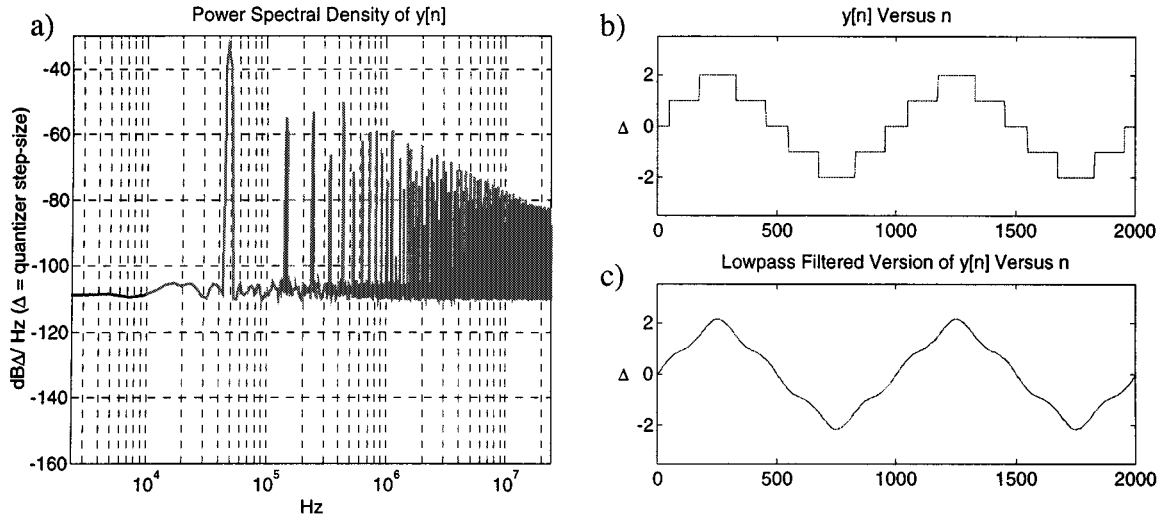


Fig. 2. (a) PSD plot of the quantizer output in decibels, relative to the quantization step-size, per hertz. (b) Time-domain plot of the quantizer output. (c) Time-domain plot of the quantizer output filtered by a sharp lowpass filter with a cutoff frequency of 500 kHz.

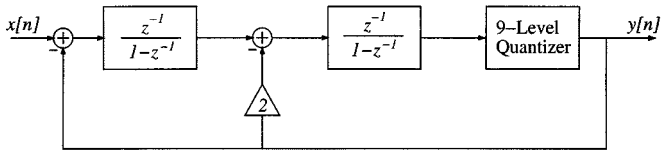


Fig. 3. Second-order $\Sigma\Delta$ modulator architecture.

ulator output PSD would contain numerous spurious tones. In mixed-signal $\Delta\Sigma$ modulators, thermal noise in the analog input sequence provides the necessary independent noise component. As discussed below, in all-digital $\Delta\Sigma$ modulators, the necessary small amount of noise can be added digitally.

*3) Dynamic Range:* Throughout this paper, the *dynamic range* of a $\Delta\Sigma$ modulator or data converter within a particular band of interest is defined as the ratio of the sinusoidal input signal power that yields the maximum output SNR over the band of interest to that which results in an SNR of zero over the band of interest. For the example $\Delta\Sigma$ modulator architecture, the dynamic range in a given frequency band of interest can be increased only in two ways: the sample-rate of the $\Delta\Sigma$ modulator can be increased, or the number of quantizer levels can be increased (thereby allowing the quantization step size to be reduced without changing the input no-overload range of the $\Delta\Sigma$ modulator). If an $M$-level uniform quantizer is used in the example $\Delta\Sigma$ modulator architecture where $M \geq 4$, the input no-overload range of the $\Delta\Sigma$ modulator extends from $-(M-3)\Delta/2$ to $(M-3)\Delta/2$, and the dynamic range of the $\Delta\Sigma$ modulator is given by

$$\text{Dynamic Range} = 20\log(M-3) + 50\log\left(\frac{f_s}{2f_{\text{bw}}}\right) - 11.1 \text{ dB} \tag{3}$$

where $f_s$ is the sampler rate of the $\Delta\Sigma$ modulator, and $f_{\text{bw}}$ is the bandwidth of the low-frequency band over which the SNR is evaluated [4], [5]. For instance, in the example $\Delta\Sigma$ modulator architecture with a nine-level quantizer and a 48-MHz sample-rate, the dynamic range evaluated from zero to $f_{\text{bw}} = 500$ kHz is 88.5 dB. The quantity $f_s/(2f_{bw})$ often is referred to as the *oversampling ratio* because it is equal to the ratio of the $\Delta\Sigma$ modulator's sample-rate to the minimum frequency at which a continuous-time signal bandlimited to frequencies below $f_{\text{bw}}$ would have to be sampled to avoid aliasing. It follows from (3) that each time the oversampling ratio is doubled for the example $\Delta\Sigma$ modulator, the dynamic range increases by 15 dB which corresponds to 2.5 bits of extra precision.

### *B. Delta–Sigma ADCs*

The discussion of $\Delta\Sigma$ modulation up to this point has been from a signal processing point of view without regard to whether the sequences within a $\Delta\Sigma$ modulator are represented as analog or digital quantities. When used within a $\Delta\Sigma$ ADC, the purpose of the $\Delta\Sigma$ modulator is not only to perform coarse quantization such that the quantization noise is attenuated in a desired band of interest as described above, but also to convert the format of the quantized output sequence to digital form. Therefore, the coarse quantizers in $\Delta\Sigma$ modulators for A/D conversion are implemented as coarse ADCs, and the feedback loops contain coarse DACs.

Fig. 5(a) shows a high-level functional diagram of a $\Delta\Sigma$ ADC. It consists of a sample-and-hold operation, a mixed-signal $\Delta\Sigma$ modulator, and a digital lowpass decimation filter.[2] To illustrate its operation, suppose that the $\Delta\Sigma$ modulator is a mixed-signal version of the example $\Delta\Sigma$ modulator architecture of Fig. 3 as shown in Fig. 5(b). Continuing with the example presented in Section II-A, further suppose that the desired component of the continuous-time analog input signal to be digitized is bandlimited to frequencies below 500 kHz, that the sample-and-hold and $\Delta\Sigma$ modulator are both clocked at 48 MHz, and that the passband of the decimation filter is 500 kHz. The $\Delta\Sigma$ modulator, therefore, generates a 48-Msample/s nine-level digital output sequence. The decimation filter removes undesired input signal components and quantization noise above 500 kHz from this sequence, and

[2]In most implementations the sample-and-hold is built into the delta–sigma modulator.

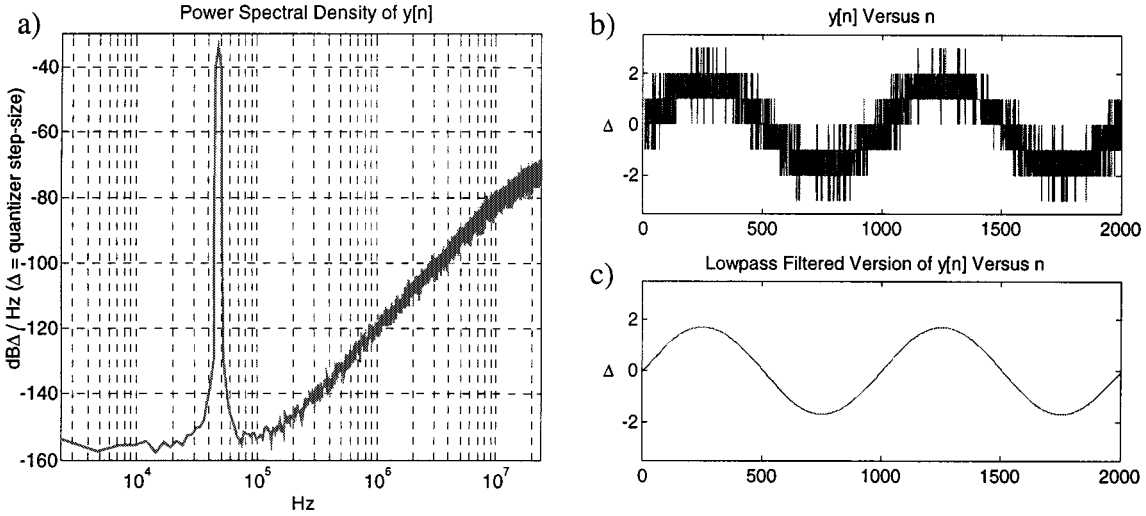


Fig. 4. (a) PSD plot of the $\Delta\Sigma$ modulator output in decibels, relative to the quantization step-size, per hertz. (b) Time-domain plot of the $\Delta\Sigma$ modulator output. (c) Time-domain plot of the $\Delta\Sigma$ modulator output filtered by a sharp lowpass filter with a cutoff frequency of 500 kHz.

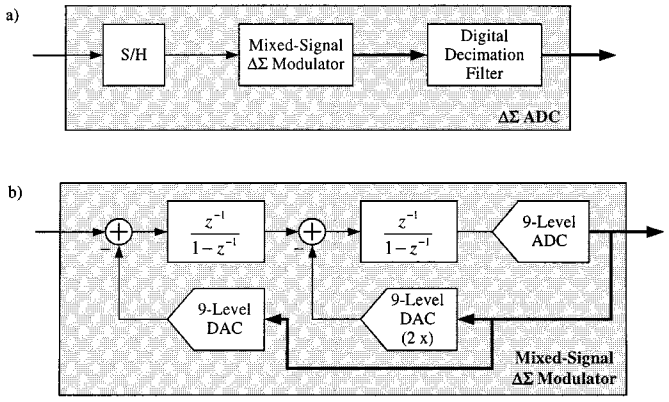


Fig. 5. (a) Functional diagram of a general $\Delta\Sigma$ ADC. (b) Functional diagram of an applicable mixed-signal $\Delta\Sigma$ modulator based on the architecture of Fig. 3.

(optionally) decimates the output rate to 1 Msample/s. As described above, although highly quantized, the nine-level $\Delta\Sigma$ modulator output sequence contains very little error within the 500-kHz passband of the decimation filter. Therefore, the output of the decimation filter is a highly accurate 1-Msample/s digital representation of the desired component of the continuous-time analog input signal. Specifically, the dynamic range of the $\Delta\Sigma$ ADC is nearly that of the $\Delta\Sigma$ modulator evaluated from zero to 500 kHz (assuming a well-designed decimation filter), which, from the discussion above, is 88.5 dB. In the absence of nonideal circuit behavior and other noise sources, this corresponds to better than 14 bits of A/D conversion precision. Thus, although the input to the decimation filter is restricted to nine levels, its output has more than $2^{14}$ levels.

A differential switched-capacitor implementation of the $\Delta\Sigma$ modulator is shown in Fig. 6. It consists of two delaying switched-capacitor integrators, a nine-level flash ADC, and a pair of nine-level switched-capacitor DACs. The signals labeled $P1$ and $P2$ are nonoverlapping clock signals at the $\Delta\Sigma$ modulator sample-rate (e.g., 48 MHz), and those labeled $P1d$ and $P2d$ are delayed versions of $P1$ and $P2$, respectively, as shown in the figure. The nine-level differential input flash ADC can be implemented using eight comparators, each of which compares the differential input voltage against one of eight evenly spaced differential reference voltages. The output of the ADC is an 8-bit *thermometer code* wherein the value of each bit is taken to be $\Delta/2$ when the bit is high and $-\Delta/2$ when the bit is low where $\Delta$ is the quantization step-size of the flash ADC and is equal to the difference between adjacent comparator reference voltages. For example, if six of the bits in the thermometer code are high and the remaining two bits are low, then the flash ADC output is interpreted to have a numerical value $2\Delta$. As shown in Fig. 6(b), each nine-level DAC consists of eight one-bit switched capacitor DAC elements each of which is driven by one of the thermometer code bits from the flash ADC.

In practice, nonideal circuit behavior causes the various analog components within the $\Delta\Sigma$ modulator to introduce noise and distortion. However, because of the decimation filter following the $\Delta\Sigma$ modulator, only noise and distortion components in the low-frequency passband give rise to significant A/D conversion error. Furthermore, the A/D conversion accuracy tends to be insensitive even to in-band noise and distortion introduced by the second switched-capacitor integrator, the flash ADC, and the right-most nine-level DAC because the resulting errors are subjected to highpass transfer functions by the $\Delta\Sigma$ modulator prior to the lowpass transfer function of the decimation filter. For example, the $\Delta\Sigma$ modulator subjects thermal noise introduced by the flash ADC to the same $(1 - z^{-1})^2$ transfer function applied to the additive noise from the quantization process, so it is significantly attenuated in the low-frequency passband of the decimation filter. Similarly, it can be shown that noise and distortion introduced by the right-most nine-level DAC and input-referred noise and distortion from the second switched-capacitor integrator are subjected to a $1 - z^{-1}$ transfer function, which also provides significant attenuation in the low-frequency passband of the decimation filter. Similar comments apply to most of the popular $\Delta\Sigma$ modulator implementations, which is why $\Delta\Sigma$ ADCs generally tend to be amenable to implementation in

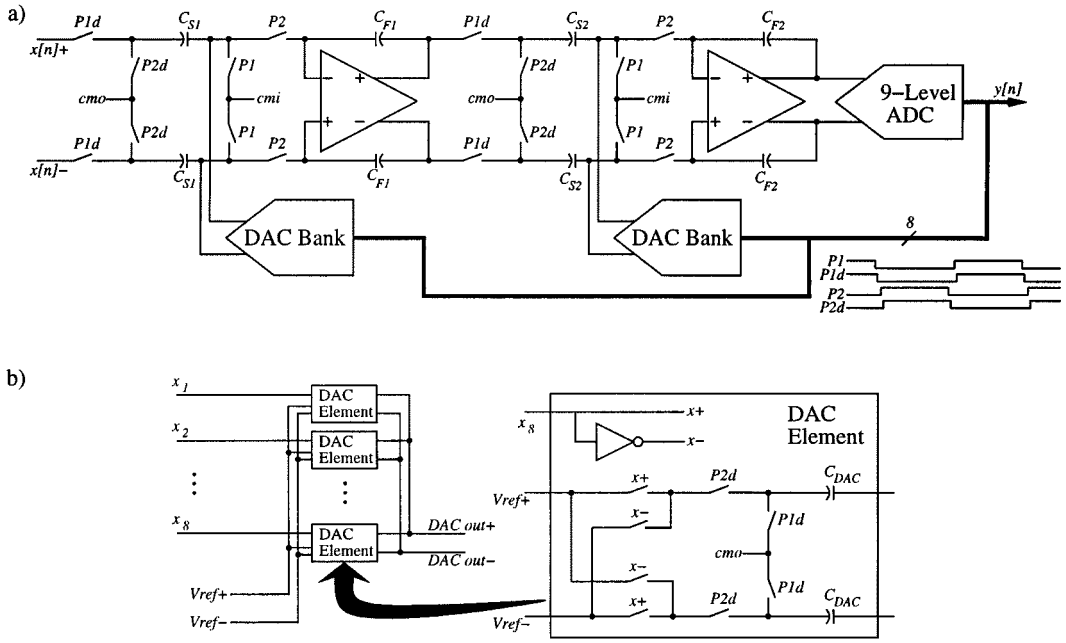


Fig. 6. (a) Switched capacitor implementation of the example $\Delta\Sigma$ modulator in Fig. 5(b). (b) Details of the nine-level DACs.

VLSI processes optimized for digital circuitry at the expense of analog performance.

### C. Other $\Delta\Sigma$ Modulator Options

To this point, the $\Delta\Sigma$ modulation concept has been illustrated via the particular example $\Delta\Sigma$ modulator architecture shown in Fig. 3, namely a second-order multi-bit $\Delta\Sigma$ modulator. While this type of $\Delta\Sigma$ modulator is widely used to perform data conversion in wireless systems, there exist several other types of $\Delta\Sigma$ modulators that also enjoy widespread use in wireless systems [1]. A thorough discussion of these other published $\Delta\Sigma$ modulator architectures and their tradeoffs is beyond the scope of this paper, although a brief overview of their primary features is presented below, and specific examples of all the main $\Delta\Sigma$ modulator architectures are referenced in the context of commercial wireless handset receivers in the next section.

Most of the other architectures are *higher order* $\Delta\Sigma$ *modulators* that perform higher than second-order quantization noise shaping thereby reducing the oversampling ratio or number of quantization levels required to achieve a given dynamic range relative to the example second-order $\Delta\Sigma$ modulator. Some of these higher order $\Delta\Sigma$ modulators incorporate a higher than second-order loop filter (e.g., more than two integrators) and a single quantizer surrounded by one or more feedback loops [6]. In many cases, these $\Delta\Sigma$ modulators are designed specifically to allow one-bit quantization for reasons explained in Section II-E [7], [8]. Others of these higher order $\Delta\Sigma$ modulators, often referred to as MASH, cascaded, or multistage $\Delta\Sigma$ modulators, are comprised of multiple lower order $\Delta\Sigma$ modulators, such as the second-order $\Delta\Sigma$ modulator presented above, cascaded to obtain the equivalent of a single higher order $\Delta\Sigma$ modulator [9], [10].

Some $\Delta\Sigma$ modulators, referred to as *bandpass* $\Delta\Sigma$ modulators, suppress their quantization noise in frequency bands not centered at dc [11]–[14]. For example, if each delay element in the second-order $\Delta\Sigma$ modulator presented above is replaced by two delay elements and a sign inversion, i.e., if each $z^{-1}$ is replaced by $-z^{-2}$ in Fig. 3, then the result is a bandpass $\Delta\Sigma$ modulator that suppresses its quantization noise in a frequency band centered at $f_s/4$ instead of dc [1]. In this case, the sample-rate would be chosen so that the signal of interest after sampling is centered at $f_s/4$. As with *lowpass* $\Delta\Sigma$ modulators, i.e., $\Delta\Sigma$ modulators that suppress quantization noise in a band centered around dc, provided the bandwidth of the desired signal is low relative to the sample-rate, the dynamic range of the $\Delta\Sigma$ modulator in the band of interest is high. Therefore, bandpass $\Delta\Sigma$ modulators are useful in situations where an analog input signal of interest is not centered at dc; rather than downconverting the real and imaginary components of the desired signal to dc and digitizing the resulting two signals with a pair of lowpass $\Delta\Sigma$ modulators, a single bandpass $\Delta\Sigma$ modulator can be used instead. However, for comparable performance the bandpass $\Delta\Sigma$ modulator would be required to have twice the order, and, thus, twice the complexity, of each lowpass $\Delta\Sigma$ modulator, and the bandwidth of the sample-and-hold circuitry must be high enough to handle the increased center frequency.

Although $\Delta\Sigma$ modulators inherently generate sampled output sequences, they can be implemented using continuous-time loop filters in place of discrete-time loop filters [15], [16]. Such $\Delta\Sigma$ modulators are referred to as *continuous-time* $\Delta\Sigma$ *modulators*. For example, if the discrete-time integrators in the second-order $\Delta\Sigma$ modulator presented above were replaced by continuous-time integrators and a sample-and-hold operation were added prior to the quantizer, then the theoretical performance of the $\Delta\Sigma$ modulator in the band of interest would be preserved. However, continuous-time loop filters offer several implementation tradeoffs relative to discrete-time filters that can be exploited in certain applications. While the majority of present-day $\Delta\Sigma$ modulators are implemented with discrete-time loop filters because of the ease with which

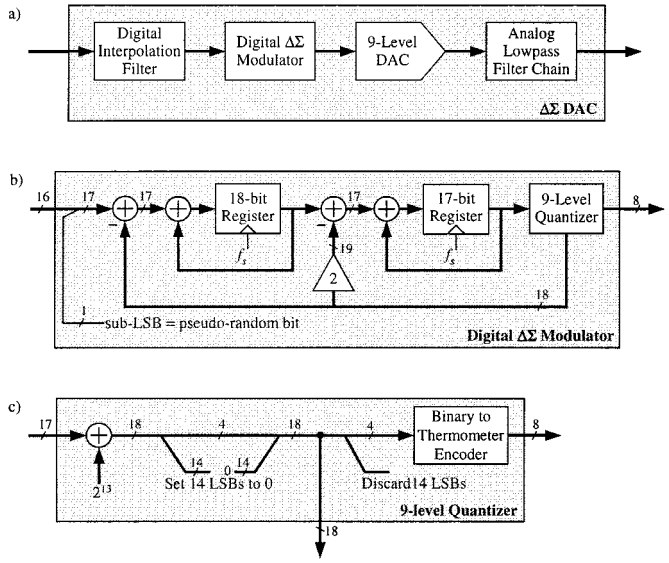


Fig. 7. (a) Functional diagram of a general $\Delta\Sigma$ DAC. (b) Implementation details of an applicable digital $\Delta\Sigma$ modulator based on the architecture of Fig. 3. (c) Implementation details of the nine-level quantizer within the $\Delta\Sigma$ modulator.

such filters can be implemented in CMOS circuit technology, continuous-time $\Delta\Sigma$ modulators have been shown to offer advantages in very low-power applications and very high-speed applications [17], [18].

### *D. Delta–Sigma DACs*

Fig. 7(a) shows a high-level functional diagram of a $\Delta\Sigma$ DAC. It consists of a digital interpolation filter, an all-digital $\Delta\Sigma$ modulator, a coarse DAC with a number of levels equal to that of the $\Delta\Sigma$ modulator output, and an analog filter chain with a sharp lowpass response. To illustrate its operation, suppose that a digital logic implementation of the $\Delta\Sigma$ modulator architecture of Fig. 3 is used in the $\Delta\Sigma$ DAC. Again continuing with the example from Section II-A, suppose that the digital input sequence has a sample-rate of 1 MHz, that the interpolation filter increases the sample-rate to 48 MHz, that the sample-rate of the digital $\Delta\Sigma$ modulator and 9-level DAC is 48 MHz, and that the analog filter chain implements a sharp lowpass filter with a cutoff frequency of 500 kHz. By virtue of the Nyquist sampling theorem, the digital input sequence can be viewed as a sampled version of a unique continuous-time signal bandlimited to frequencies below 500 kHz. Although it is an all-digital structure, the interpolation filter generates a sequence identical to a 48-MHz sampled version of the continuous-time signal corresponding to the input sequence (up to an accuracy limited only by the order of the digital filter implementation) [19]. Thus, the discrete-time spectrum of the $\Delta\Sigma$ DAC's input sequence is completely contained within the 0-500-kHz frequency band of the interpolation filter's output sequence. As discussed in Section II-A, the $\Delta\Sigma$ modulator quantizes this sequence to nine levels such that most of the quantization noise power resides *outside* the 0-500-kHz band. The lowpass analog filter chain subsequently removes the out-of-band quantization noise along with any out-of-band noise and distortion introduced by the nine-level DAC. As in the case of the $\Delta\Sigma$ ADC presented in Section II-B, in the absence of nonideal circuit behavior the dynamic range of the $\Delta\Sigma$ DAC is 88.5 dB.

Fig. 7(b) shows an example digital logic implementation of the $\Delta\Sigma$ modulator at the register transfer level, and Fig. 7(c) shows the details of the nine-level quantizer. Except for the 8-bit thermometer coded output sequence, all quantities are represented as two's complement numbers with the bus widths shown in the figures. The implemented architecture is that of Fig. 3 with the addition of a 1-bit sub-LSB independent white noise sequence at the input node. As described in Section II-A, the purpose of the input noise sequence is to ensure that the quantization noise introduced by the nine-level quantizer is uncorrelated with the input sequence and white with a variance of $\Delta^2/12$. In practice, a pseudorandom noise sequence is typically used in place of a truly random noise sequence. Such a sequence can be generated easily using a linear feedback shift register, and tends to have the desired result with respect to the quantization noise despite not being truly random.

### *E. Mismatch-Shaping DACs*

In the $\Delta\Sigma$ ADC example presented above, one of the nine-level DAC outputs is subtracted directly from the input of the $\Delta\Sigma$ modulator as shown in Fig. 5(b). Any error introduced by this DAC adds directly to the $\Delta\Sigma$ modulator input sequence, so the portion of this error within the passband of the decimation filter directly degrades the overall A/D conversion accuracy. In the $\Delta\Sigma$ DAC example, the nine-level DAC directly precedes the lowpass analog filter chain as shown in Fig. 7(a), so any error it introduces within the passband of the analog filter chain similarly degrades the overall D/A conversion accuracy. Similar observations apply to the other commonly used $\Delta\Sigma$ data converter architectures. Thus, the accuracy of any given $\Delta\Sigma$ ADC or DAC is only as high as the accuracy of one of its constituent coarse DACs over the passband of the data converter.

Very often, the dominant sources of error in a coarse DAC are mismatches among nominally identical components. For example, the capacitors in the eight one-bit DAC elements of the nine-level DAC shown Fig. 6(b) each have a nominal value of $C_{DAC}$. However, VLSI fabrication errors result in mismatches among these capacitors with a standard deviation rarely lower than 0.1% in practice. Such mismatches give rise to fixed errors in the nine output levels of the DAC, and these errors give rise to data-dependent nonlinear distortion. In the data converter examples presented above, uncorrelated random DAC element capacitor mismatches with a standard deviation of 0.1% limit the data conversion SNR to approximately 65 dB, a significant reduction from the 88.5 dB achieved with ideal circuit behavior.

A common method of avoiding this problem is to use $\Delta\Sigma$ modulators with single-bit (i.e., two-level) quantization which allows for the use of single-bit DACs. Any single-bit DAC with fixed errors in its two output levels is equivalent an error-free DAC followed by a fixed gain error and a fixed offset error. Therefore, component mismatches in a single-bit DAC do not cause nonlinear distortion; they simply give rise to fixed gain and offset errors, and the accuracy of a $\Delta\Sigma$ data converter is typically not sensitive to such gain and offset errors.

Unfortunately, $\Delta\Sigma$ modulators with single-bit quantization tend not to perform as well as $\Delta\Sigma$ modulators with multi-bit

(i.e., more than two-level) quantization. For example, if the nine-level quantizer in the 48-Msample/s $\Delta\Sigma$ modulator example presented in Section II-A were replaced by a one-bit quantizer, the dynamic range of the $\Delta\Sigma$ modulator in the 0-500-kHz band would be reduced from 88.5 dB to approximately 65 dB. Moreover, unlike the nine-level quantizer case, the additive noise from the single-bit quantizer would not be white and would be correlated with the input sequence. Its variance would be signal dependent and it would contain spurious tones. These problems can be mitigated by using a higher-order $\Delta\Sigma$ modulator architecture to more aggressively suppress the in-band portion of the additive noise from the two-level quantizer. However, to maintain stability in a higher order $\Delta\Sigma$ modulator with single-bit quantization, the input range of the $\Delta\Sigma$ modulator input signal must be reduced and more poles and zeros must be introduced within the feedback loop as compared to a multibit design with a comparable dynamic range. Even then, the problem of spurious tones persists, and it is difficult to predict where they will appear except through extensive simulation.

In recent years, mismatch-shaping DACs have emerged as enabling components for reaping the benefits of multibit quantization in $\Delta\Sigma$ data converters [20]–[32]. Mismatch-shaping DACs use a technique closely related to $\Delta\Sigma$ modulation to cause error from component mismatches to be suppressed within a desired narrow signal band and uncorrelated with the input sequence much like $\Delta\Sigma$ modulator quantization noise. Surprisingly, mismatch-shaping DACs are able to do this without knowing or measuring the values of the component mismatches. They operate by permuting the one-bit DAC elements in a multibit DAC of the type shown Fig. 6 in a data-dependent fashion. For example, a *digital encoder* can be inserted in the feedback paths between the ADC and the two nine-level DACs in Fig. 6 to convert the DACs to mismatch-shaping DACs. The digital encoder maps each of its 8 one-bit input lines to one of its eight one-bit output lines during each clock period, but changes the mapping after each clock period in a fashion that depends upon the 8-bit input sequence. An explanation of the mismatch-shaping phenomenon is beyond the scope of this paper, but is provided in [1], [27], and [29].

### *F. Delta–Sigma Fractional-$N$ PLLs*

An example of a typical *integer-$N$* PLL for frequency synthesis is shown in Fig. 8 [33]. It consists of a phase detector, a charge pump, a lowpass loop filter, a voltage-controlled oscillator (VCO), and a digital $N$-fold divider. The phase detector compares the positive edges of a reference frequency signal to those from the divider and causes the charge pump to drive the lowpass filter with current pulses whose widths are proportional to the phase difference between the two signals. The pulses are lowpass filtered by the loop filter and the resulting waveform drives the VCO. Within the loop bandwidth, the phase noise of the VCO is suppressed so it generates a spectrally pure periodic output with a frequency equal to $N$ times the reference frequency. The output frequency can be changed by changing $N$, but $N$ must be an integer, so the output frequency can be changed only by integer multiples of the reference frequency. If

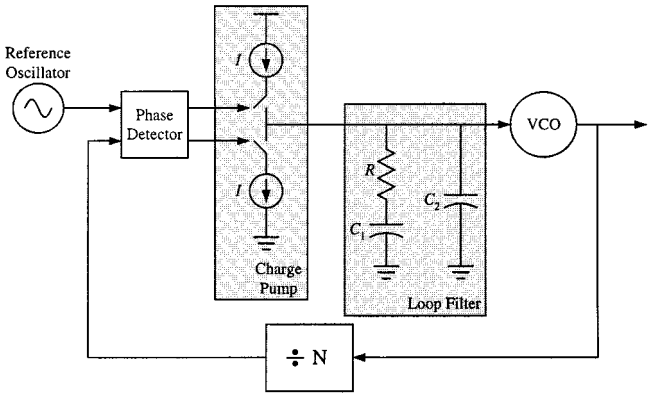


Fig. 8. Typical integer-$N$ PLL architecture.

fine tuning resolution is required, the only option is to make the reference frequency very low. Unfortunately, this tends to reduce the maximum practical loop bandwidth thereby increasing the settling time of the PLL, and it also tends to increase the portions of the phase noise in the PLL output signal contributed by the reference frequency source, the phase detector, and the divider.

Delta–sigma fractional-$N$ PLLs provide a means of achieving fine tuning resolutions without using low reference frequencies [34]–[36]. An example of a $\Delta\Sigma$ fractional-$N$ synthesizer is shown in Fig. 9(a). It is similar to the integer-$N$ PLL described above except that the fixed $N$-fold divider has been replaced by a digital *multimodulus* divider controlled by a second-order digital $\Delta\Sigma$ modulator with five-level quantization. The $\Delta\Sigma$ modulator is clocked by the output of the multimodulus divider. Its output, $y[n]$, can take on values in the range $\{-2, -1, 0, 1, 2\}$ and causes the multimodulus divider to down-count the VCO output signal by $N + y[n]$. The PLL loop filter tends to remove the out-of-band $\Delta\Sigma$ modulator quantization noise in $y[n]$. Provided the bandwidth of the $\Delta\Sigma$ modulator input sequence, $x[n]$, is within the PLL loop bandwidth, the instantaneous frequency of the VCO is set precisely to $N + x[n]$ times the reference frequency. Therefore, $\Delta\Sigma$ fractional-$N$ synthesizers can be used to generate fixed frequency signals with fine resolution or can be used to generate frequency-modulated signals.

The quantization noise from the $\Delta\Sigma$ modulator does add to the overall phase noise in the PLL output signal. However, provided the loop bandwidth is sufficiently narrow, much of the phase noise is suppressed. For example, Fig. 9(b) shows PSD plots of the output phase noise contributed by quantization noise from the $\Delta\Sigma$ modulators in two computer-simulated versions of the example fractional-$N$ PLL, one with a 50-kHz loop bandwidth and the other with a 500-kHz loop bandwidth. The parameters of the 50-kHz bandwidth version are: $N = 51$, $I = 50$ $\mu$A, $R = 1.6$ k$\Omega$, $C_1 = 13.9$ nF, $C_2 = 290$ pF, and a VCO gain of 200 MHz/V. Those of the 500-kHz bandwidth version are the same except with: $R = 16$ k$\Omega$, $C_1 = 140$ nF, and $C_2 = 2.9$ nF. As expected, the version with the 500-kHz bandwidth suppresses much less of the highpass $\Delta\Sigma$ modulator quantization noise than the 50-kHz bandwidth version. This tradeoff between loop bandwidth and phase noise repre-

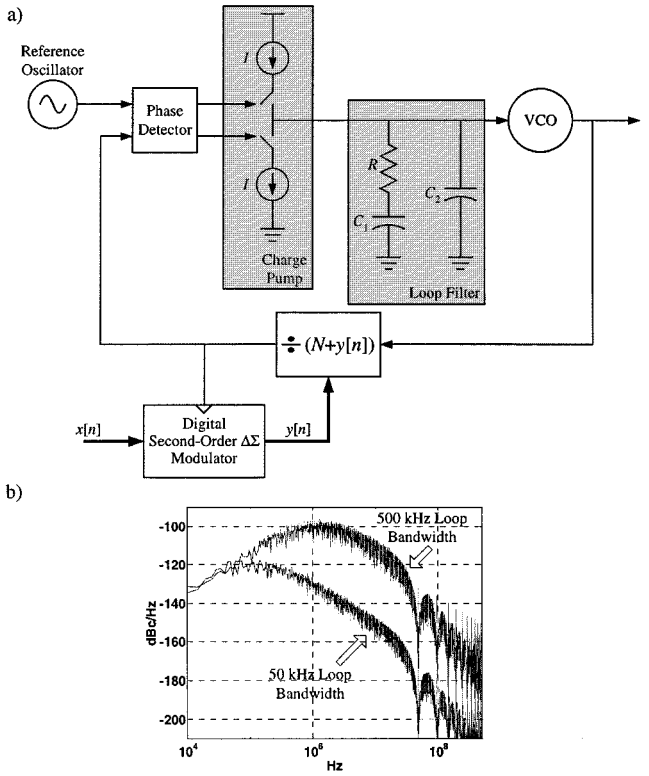


Fig. 9. (a) $\Delta\Sigma$ fractional-$N$ PLL example. (b) PSD plots of the phase noise resulting from the $\Delta\Sigma$ modulator quantization noise with $R$, $C_1$, and $C_2$ chosen such that the loop bandwidth is 50 kHz and 500 kHz, respectively.

sents a fundamental limitation in $\Delta\Sigma$ fractional-$N$ PLLs in general. In the next section, this issue is considered further with respect to specific applications to wireless transmitters.

## III. Delta–Sigma Data Converters in Wireless Transceivers

The three types of $\Delta\Sigma$ data converters discussed in Section II, i.e., $\Delta\Sigma$ ADCs, DACs, and fractional-$N$ synthesizers, as well as mismatch-shaping DACs are used in wireless transceivers for a variety of tasks. Delta–sigma ADCs are used widely in wireless handset receivers to digitize downconverted signals. Mismatch-shaping DACs are used within some of these $\Delta\Sigma$ ADCs, and also as components within segmented DACs in some wireless handset transmitters to generate analog signals prior to upconversion. Delta–sigma fractional-$N$ synthesizers sometimes are used to generate local oscillator signals with which to upconvert signals for transmission and downconvert signals for reception, and in some cases they are also used to generate frequency or phase-modulated transmit signals directly. Both $\Delta\Sigma$ DACs and $\Delta\Sigma$ ADCs are ubiquitous in the audio CODECs within cellular telephone handsets for converting analog voice signals to and from digital form. Delta–sigma DACs are used sometimes in auxiliary tasks such as automatic frequency control to compensate for frequency errors in local oscillators. The purpose of this section is to describe some of most significant of these applications and their implications with respect to the corresponding radio architectures through examples of commercial wireless transceivers.

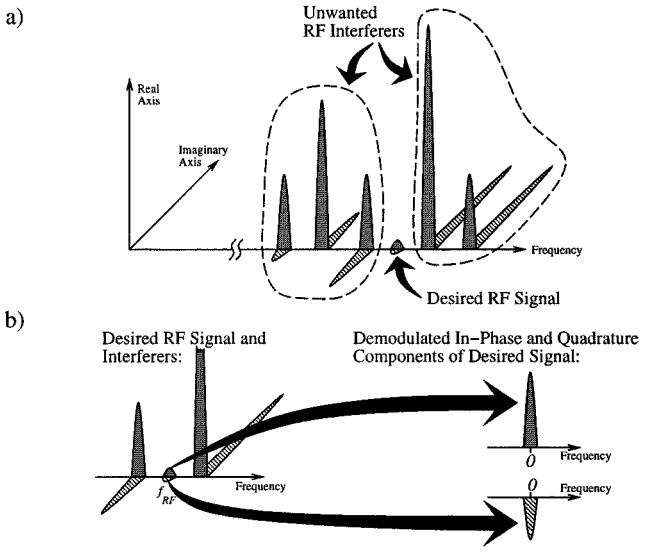


Fig. 10. (a) Frequency-domain representation of a typical signal at the antenna jack of a wireless receiver. (b) Quadrature demodulation operation of the receiver.

### A. A/D Conversion in Wireless Handset Receivers

*1) The Receiver Problem:* A frequency-domain representation of a typical radio frequency (RF) signal seen at the antenna jack of a wireless receiver is shown in Fig. 10(a). It consists of a *desired signal* centered at a frequency, $f_{\rm RF}$, along with numerous interfering signals, referred to as *interferers*, centered at surrounding frequencies. For example, a GSM cellular telephone base station can transmit 124 modulated signals distributed in 200-kHz increments between 935 MHz and 960 MHz. Each signal encodes a 270.833-kHz sequence of data bits using a Gaussian MSK signal format with a 3-dB bandwidth of 160 kHz. A GSM handset receiver must be able to treat any one of these as the desired signal and all other signals as interferers. The frequency band within which the desired signal can reside is referred to as the *receive band*, so the receive band extends from 935 MHz to 960 MHz in the GSM example. The handset receiver must remove the interferers and *detect* the transmitted bit sequence. In most receivers, the bit detection process is performed once the desired signal has been downconverted to a nonzero intermediate frequency (IF) or to dc. When the desired signal is downconverted to dc prior to bit detection, the downconversion is usually performed *in quadrature* as illustrated in Fig. 10(b).

In most modern wireless communication systems, the receiver is required to have a large dynamic range, high frequency selectivity, and high linearity. For example, one requirement of a GSM handset receiver is that in the absence of interferers it must have a bit error rate (BER) of less than 0.1% for any desired signal with a power level between $-102$ dBm and $-15$ dBm measured at the antenna jack. To achieve this BER limit, the detector following the downconversion process requires an input signal-to-noise-and-distortion ratio (SNDR) of at least 9 dB within the 200-kHz band containing the desired signal. This implies a minimum receiver dynamic range requirement of 96 dB. Another requirement of a GSM handset receiver is that it must achieve the 0.1% BER limit for

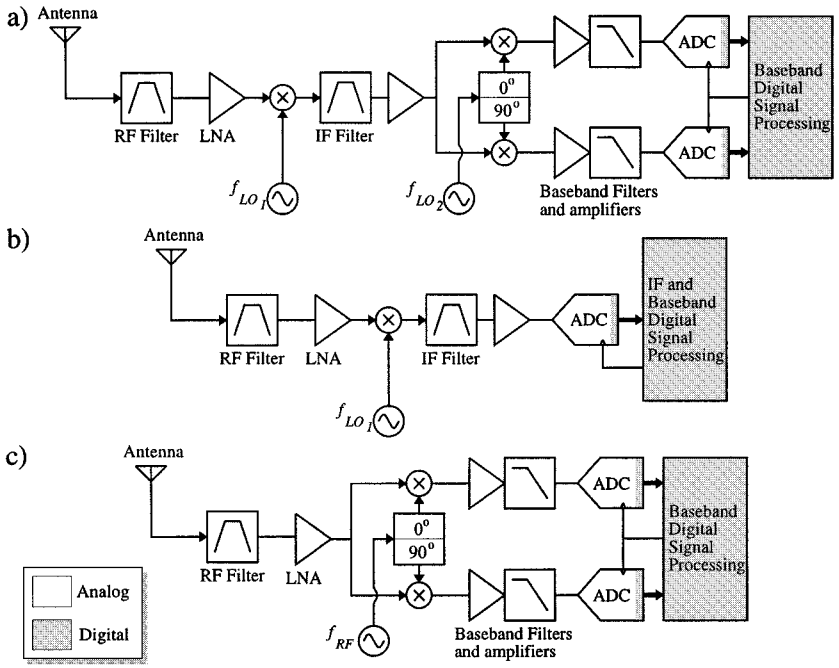


Fig. 11. (a) Superheterodyne receiver architecture with quadrature baseband ADCs. (b) Superheterodyne receiver architecture with a bandpass ADC. (c) Direct conversion receiver architecture with quadrature baseband ADCs.

a −99 dBm desired signal in the presence of a −23 dBm interferer located 3 MHz from the desired signal. This implies that the receiver must have a 3-dB bandwidth of 160 kHz around the desired signal yet reject the interferer 3 MHz away from the desired signal by at least 85 dB. Yet another requirement of the handset receiver is that it must achieve the 0.1% BER limit for a −99 dBm desired signal in the presence of two −49-dBm interferers, one 800 kHz and the other 1600 kHz from the desired signal. Thus, the receiver must have sufficient linearity that intermodulation products and aliased harmonics of the interferers do not reduce the SNDR at the detector input to less than 9 dB.

*2) Superheterodyne and Direct Conversion Receiver Architectures and Tradeoffs:* Most digital wireless receivers that incorporate ADCs prior to detection can be divided into three general categories: 1) superheterodyne with quadrature baseband A/D conversion; 2) superheterodyne with nonquadrature IF A/D conversion; and 3) zero-IF or low-IF direct conversion with quadrature A/D conversion.[3] Generic examples of these architectures are shown in Fig. 11. Historically, the superheterodyne architecture with quadrature baseband A/D conversion has been the most widely used of these architectures in commercial products. Superheterodyne receivers downconvert, filter, and amplify the RF signal from the antenna via multiple stages. As depicted in Fig. 11(a) for the case of a superheterodyne receiver with two downconversion steps, an *RF stage* attenuates interferers outside the receive band and then amplifies and downconverts the result to a fixed nonzero IF. An *IF stage* further attenuates interferers both inside and outside the receive band, and then further amplifies and downconverts the result, in quadrature, to a *baseband* centered at dc. A *baseband stage* further amplifies and filters and then A/D converts the resulting in-phase and quadrature signals. After the ADCs, digital filtering may be performed if necessary to further attenuate interferers before digital detection of the bit sequence is performed. Alternatively, as depicted in Fig. 11(b), the IF signal may be digitized by a single ADC after which additional filtering, quadrature downconversion to dc, and bit detection are performed in the digital domain. In both cases, passive bandpass filters that offer high selectivity with high linearity and low noise, such as surface acoustic wave (SAW) filters, typically are used in the RF and/or IF stages to attenuate interferers prior to amplification. By removing much of the interferer power prior to amplification, these filters greatly reduce the linearity and dynamic range requirements of the subsequent stages and of the ADCs. However, such filters are not amenable to on-chip implementation with present VLSI technology, and tend to be expensive relative to the rest of the receiver. They also tend to be large relative to the die size of the integrated radio components, so they limit the extent to which a receiver can be miniaturized.

To avoid these problems, zero-IF and low-IF direct conversion receivers, an example of which is shown in Fig. 11(c), have become prominent in recent years. By downconverting the entire receive band directly to a baseband centered at or near dc (usually less than 5 MHz), they allow most of the necessary amplification and interferer filtering to be performed by lowpass baseband amplifiers and filters which are amenable to on-chip implementation, either as analog components or as a combination of analog components, ADCs, and digital filters [37]–[39]. However, in contrast to superheterodyne receivers, the baseband components must be highly linear because they must pass the desired signal while rejecting interferers that can be huge (e.g., 78 dB more powerful than the desired signal in the case of a GSM receiver) because

[3]This excludes digital receivers based on analog FM detection and all-analog receivers.

they are not attenuated by previous receiver stages. Zero-IF and low-IF direct conversion receivers are particularly sensitive to even order nonlinearity in their baseband components because any interferer subjected to an even order nonlinearity introduces a distortion product at dc which potentially corrupts the dc or near-dc downconverted desired signal. In zero-IF direct conversion receivers, two additional problems are caused by the local oscillator having the same frequency as the RF desired signal: the local oscillator signal inadvertently can be radiated and interfere with other nearby receivers, and it can couple to the RF mixer input port and become downconverted to dc thereby contributing to a large unwanted offset on the downconverted desired signal. Offset voltages from circuit mismatches also contribute to this dc offset, and any $1/f$ noise introduced by the baseband components directly corrupts the downconverted desired signal. Low-IF direct conversion receivers avoid the dc offset problems and are less sensitive to $1/f$ noise, but are sensitive to gain and phase mismatches in their quadrature paths which can cause interferers at image frequencies to corrupt the downconverted desired signal. Nevertheless, despite these problems, high-performance commercial wireless receivers that perform zero-IF and low-IF direct conversion have been developed recently. In many cases, some of which are discussed below, the problems have been significantly eased by the use of $\Delta\Sigma$ ADCs.

*3) Analog Versus Digital Processing in Receivers:* In receivers that do not perform any digital filtering and use analog automatic gain control (AGC) to compensate for variability in the amplitude of the desired signal, precise A/D conversion usually is not necessary and the conversion rate can be as low as the symbol rate of the transmitted signal. For example, as mentioned above, the bit detector in a GSM receiver requires only 9 dB of SNDR to achieve the requisite 0.1% maximum BER. Therefore, a pair of flash ADCs that each perform 4-bit uniform quantization at a sample-rate of 270.833 kHz would more than suffice in a GSM receiver that performs quadrature downconversion with all filtering and AGC in the analog domain.

However, given the reduction in power consumption and circuit area that can be achieved by trading analog processing for digital processing in VLSI circuits, the trend in wireless receivers is to perform as much of the filtering as possible in the digital domain. But this greatly increases the dynamic range and sample-rate required of the ADCs. The ADCs must have a large dynamic range to accommodate large interferers, and they must have a high sample-rate to avoid aliasing of interferers onto the downconverted desired signal. For example, suppose a GSM handset receiver removes interferers outside the 25 MHz receive band via an RF filter and then performs quadrature downconversion to dc without significantly attenuating interferers in the receive band prior to the baseband ADCs. In this case, even with ideal analog AGC, the power of the input signal to each ADC can vary by 76 dB. If the receiver were to introduce no noise and distortion prior to the ADCs, each ADC would need to perform digitization with a dynamic range of 85 dB over the bandwidth of the downconverted desired signal to achieve the minimum required SNDR of 9 dB at the detector following the ADCs and digital filters. However, to allow for noise and distortion introduced by the receiver prior to the ADCs, a more reasonable dynamic range for each ADC is on the order of 95 dB. To avoid the possibility of an interferer aliasing onto the downconverted desired signal, each ADC must have a sample-rate of at least 25 MHz. Such ADC performance is difficult to achieve, but if a relatively small amount of analog filtering, e.g., such as offered by a third-order lowpass filter with a 200-kHz passband, is used prior to each ADC, the ADC dynamic range and sample-rate can be reduced to more manageable values, e.g., on the order of 80 dB and 13 MHz, respectively.

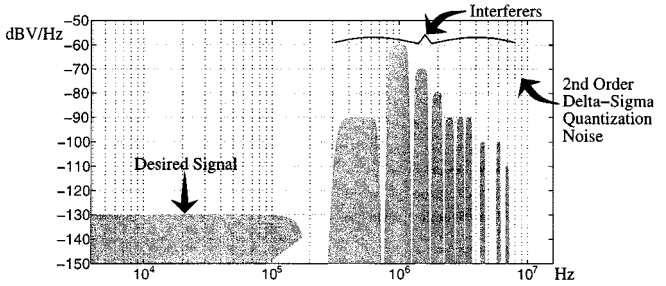


Fig. 12. Conceptual PSD plot of the digital output of the $\Delta\Sigma$ modulator in a $\Delta\Sigma$ ADC used in a wireless receiver.

*4) Delta–Sigma ADCs in Wireless Handset Receivers:* In present VLSI technology, ADCs with sample-rates greater than 10 MHz that achieve greater than 70 dB of dynamic range over their entire discrete-time frequency bands, i.e., from zero to half their sample-rate, tend to consume too much power to be attractive in battery-operated handset receivers. Fortunately, the ADCs in wireless handset receivers need only achieve high dynamic range over the bandwidth of the downconverted desired signal. The interferers do not have to be digitized accurately because the only purpose of digitizing them is to facilitate their removal by digital filters. Consequently, $\Delta\Sigma$ ADCs are ideally suited for use in wireless handset receivers. In a given receiver the $\Delta\Sigma$ ADC passband is chosen to be the band of the downconverted desired signal. As depicted in Fig. 12, the digital output of the $\Delta\Sigma$ modulator then contains the downconverted desired signal along with interferers and $\Delta\Sigma$ modulator quantization noise. Although digitized by the $\Delta\Sigma$ modulator, the interferers are corrupted by quantization noise. However, this is not a problem provided the analog circuitry within the $\Delta\Sigma$ modulator is sufficiently linear that the downconverted desired signal is not significantly corrupted by intermodulation products or aliased harmonics of the interferers. In this case, the decimation filter following the $\Delta\Sigma$ modulator performs the dual purposes of removing out-of-band quantization noise and attenuating interferers. Thus, $\Delta\Sigma$ modulators are particularly efficient because they only perform accurate A/D conversion in the band where high accuracy is necessary. In practice $\Delta\Sigma$ ADCs that achieve a given large dynamic range only over a narrow passband but have sufficient linearity to accommodate interferers over a larger frequency band tend to consume much less power than ADCs with comparable linearity that achieve the full dynamic range over the larger frequency band. For this reason, $\Delta\Sigma$ ADCs are widely used in receivers from all three of the receiver categories mentioned above.

*5) Delta–Sigma ADCs in Superheterodyne Receivers:* Although superheterodyne receivers inherently perform much of their AGC and filtering in the analog domain, $\Delta\Sigma$ modulators

nevertheless are used widely to facilitate supplemental AGC and filtering in the digital domain. For example, a commercial superheterodyne receiver with quadrature A/D conversion for GSM handsets is described in [40] and [41]. In this case, second-order $\Delta\Sigma$ modulators with one-bit quantization and a sample-rate of 13 MHz are used that achieve approximately 65 dB of dynamic range over a bandwidth of 100 kHz. Another example of a superheterodyne receiver with quadrature baseband $\Delta\Sigma$ ADCs, in this case, a commercial broadcast AM/FM receiver is presented in [42]. In this example, a pair of fifth-order continuous-time $\Delta\Sigma$ modulators with single-bit quantization and a sample-rate of 21.07 MHz achieve a dynamic range of 97 dB over a 9-kHz frequency band for AM reception, and 82 dB over a 200-kHz band for FM reception. The pair of $\Delta\Sigma$ modulators along with circuitry that performs quadrature downconversion from a 10.7-MHz IF dissipate only 8 mW of power.

Similarly, superheterodyne receivers with nonquadrature IF A/D conversion often incorporate $\Delta\Sigma$ ADCs. In such cases, the A/D conversion is implemented by a single *bandpass* $\Delta\Sigma$ ADC with a passband centered at an IF frequency. An example of such a receiver is presented in [43] for the case of a commercial IC that can be configured for a variety of two-way radio applications. In this example, a switched-capacitor fourth-order bandpass $\Delta\Sigma$ modulator with nine-level quantization, mismatch-shaping DAC's, and a user-selectable sample-rate, $f_s$, between 12 and 24 MHz is used to digitize signals in a passband centered at a second IF of $f_s/8$. The $\Delta\Sigma$ ADC achieves 88 dB of dynamic range in a 10-kHz passband and 75 dB of dynamic range in a 200-kHz passband with a power dissipation of less than 22 mW.

*6) Delta–SigmaADCsinDirectConversionReceivers :* Delta-sigma ADCs are particularly beneficial in zero-IF and low-IF direct conversion receivers. As described above, all interferers within the RF receive band are downconverted along with the desired signal to baseband in such receivers, so the full burden of removing these potentially large interferers and amplifying the potentially small downconverted desired signal falls on the baseband components. By providing high dynamic range A/D conversion with high linearity, $\Delta\Sigma$ ADCs allow for reduced analog baseband amplification and a transfer of much of the baseband filtering responsibility from analog circuits to digital circuits. The high A/D conversion dynamic range and the attendant reduction in the necessary amplification prior to the ADCs make dc offsets less of a problem in zero-IF direct conversion receivers; to a large extent, dc offsets can be digitized by the ADCs and removed in the digital domain. Generally, in both zero-IF and low-IF direct conversion receivers, the reduction in the necessary analog gain along with the relaxed analog filtering requirements significantly simplify the problem of achieving the necessary analog circuit linearity.

For these reasons, several commercial direct conversion receivers with high-performance quadrature $\Delta\Sigma$ ADCs have been deployed in recent years. For example, a Bluetooth receiver that performs zero-IF direct conversion with most of its receive band filtering in the digital domain is described in [44] and [45]. After downconversion and only low-order analog antialias filtering, a pair of second-order switched-capacitor $\Delta\Sigma$ modulators with 17-level quantization and mismatch-shaping DACs digitize the quadrature baseband signals at a sample-rate of 32 MHz. Each $\Delta\Sigma$ modulator achieves 80 dB of dynamic range over the 0-500-kHz signal band, and together the two $\Delta\Sigma$ modulators dissipate 24 mW of power. Another example of a commercial zero-IF direct conversion receiver, in this case a GSM handset receiver, is described in [46] and [47]. In this example, a pair of fourth-order switched-capacitor $\Delta\Sigma$ modulators with one-bit quantization digitize the quadrature baseband signals at a sample-rate of 13 MHz each with a dynamic range of 80 dB over the 0–100-kHz signal band [48]. An example of a commercial low-IF direct conversion receiver, again a GSM handset receiver, is presented in [49]. In this example, a pair of fourth-order switched-capacitor MASH $\Delta\Sigma$ modulators, each consisting of a cascaded pair of second-order $\Delta\Sigma$ modulators with single-bit quantization, digitize a baseband signal centered at 100 kHz. Each fourth-order $\Delta\Sigma$ modulator has a sample-rate of 13 MHz and achieves 84 dB of dynamic range over a bandwidth of 189 kHz. Together, the pair of $\Delta\Sigma$ modulators dissipates 10 mW of power.

### *B. D/A Conversion in Wireless Handset Transmitters*

In wireless transmitters, an RF modulated signal must be generated prior to transmission. Most commonly, this is done either by generating an analog baseband or IF version of the signal to be modulated and then upconverting the signal to RF, or by modulating a VCO with the instantaneous frequency of the signal to be modulated. In all transmitters with digital modulation formats and some with analog modulation formats, part of the signal processing is done in the digital domain, so, at some point, some form of D/A conversion is required. In transmitters that perform upconversion from a baseband centered at or near dc, a pair of DACs usually is required to convert in-phase and quadrature baseband signals to analog form prior to upconversion. Alternatively, the quadrature baseband signals may be modulated to an IF in the digital domain and a single DAC may be used to convert the result to analog form. In transmitters that modulate a VCO, a DAC can be used to generate a signal with which to directly modulate an open-loop VCO, or the VCO may be modulated indirectly through the digital $\Delta\Sigma$ modulator within a fractional-$N$ frequency synthesizer.

The DACs in wireless handset transmitters are rarely implemented as $\Delta\Sigma$ DACs, because high dynamic range D/A conversion usually is not required prior to upconversion. In contrast to the received signal, the digital baseband or IF version of the transmitted signal has no interferers, and little inadvertent amplitude variability. Therefore, DACs in wireless transmitters usually only require precisions in the range of 4–10 bits. For such low-precision conversion, $\Delta\Sigma$ DAC implementations tend to be less area and power efficient than other types of DACs.

Although the DACs prior to upconversion need not have a high dynamic range, they must be sufficiently linear to avoid creating spectral images of the modulated signal that exceed a certain specified spectral mask in the final output of the transmitter. Therefore mismatch-shaping DACs are sometimes used in wireless transmitters to convert nonlinear distortion that would otherwise be introduced by component mismatches to out-of-band noise. For example, a 10-bit segmented DAC is described in [50] that consists of a 4-bit mismatch-shaping

DAC to convert the four most significant of the ten input bits and a 6-bit DAC without mismatch-shaping to convert the six least significant of the ten input bits. A pair of the DACs are used to convert the in-phase and quadrature baseband signals in a GSM handset transmitter. Each DAC has a sample-rate of 6.5 MHz which is much higher than the 100-kHz bandwidth of its input sequence and is followed by a lowpass analog filter, so most of the shaped mismatch noise from the 4-bit MSB DAC is suppressed prior to upconversion. By virtue of its small step-size compared to that of the 4-bit DAC, mismatch-shaping is not required in the 6-bit DAC.

### C. VCO Modulation in Wireless Handset Transmitters

A transmitter with virtually any modulation format can be implemented using D/A conversion to generate analog baseband or IF signals and upconversion to generate the final RF signal. However, many of the commonly used modulation formats in wireless communication systems such as MSK and FSK involve only frequency or phase modulation of a single carrier [51]. In such cases, the transmitted signal can be generated by modulating an RF VCO as outlined above, thereby eliminating the need for conventional upconversion stages and much of the attendant analog filtering. At least two approaches have been successfully implemented in commercial wireless transmitters to date. One is based on open-loop VCO modulation, and the other is based on $\Delta\Sigma$ fractional-$N$ synthesis.

An example of a commercial transmitter that uses the open-loop VCO modulation technique is presented in [52] and [53], in this case for a DECT cordless telephone. Between transmit bursts, the desired center frequency is set relative to a reference frequency by enclosing the VCO within a conventional analog PLL. During each transmit burst, the VCO is switched out of the PLL and the desired frequency modulation is applied directly to its input. The primary limitation of the approach is that it tends to be highly sensitive to noise and interference from other circuits. For example, in [53], the required level of isolation precluded the implementation of a single-chip transmitter. Furthermore, the modulation index of the transmitted signal depends upon the absolute tolerances of the VCO components which are often difficult to control in low-cost VLSI technologies and can also drift rapidly over time.

In principle, $\Delta\Sigma$ fractional-$N$ synthesizers avoid these problems by indirectly modulating the VCO within a feedback loop. The VCO can be modulated by driving the input of the digital $\Delta\Sigma$ modulator in a $\Delta\Sigma$ fractional-$N$ synthesizer with the desired frequency modulation of the transmitted signal. As described in Section II, the bandwidth of the PLL must be narrow enough that the quantization noise from the $\Delta\Sigma$ modulator is sufficiently attenuated. However, the bandwidth of the PLL must be sufficiently high to allow for the modulation. For instance, the phase noise PSD of the example $\Delta\Sigma$ fractional-$N$ PLL shown in Fig. 9(a) with a 50-kHz loop bandwidth meets the necessary phase noise specifications when used as a local oscillator in a conventional upconversion stage within a Bluetooth wireless LAN transmitter [54]. However, if the Bluetooth transmitter is to be implemented by modulating the VCO within the fractional-$N$ PLL through the digital $\Delta\Sigma$ modulator, then the loop bandwidth of the PLL must be around 500 kHz. Unfortunately, when the loop bandwidth of the fractional-$N$ PLL shown in Fig. 9(a) is widened to 500 kHz by changing the loop filter components as described in Section II, the resulting phase noise becomes too large to meet the Bluetooth transmit requirements.

Nevertheless, commercial transmitters with VCO modulation through $\Delta\Sigma$ fractional-$N$ synthesizers are beginning to be deployed, especially in low-performance, low-cost wireless systems such as Bluetooth wireless LANs [55]. Facilitating this trend are various solutions that have been devised in recent years to allow for wide-band VCO modulation in $\Delta\Sigma$ fractional-$N$ PLLs without incurring the severe phase noise penalty mentioned above. One of the solutions is to keep the loop bandwidth relatively low, but pre-emphasize (i.e., highpass filter) the digital phase modulation signal prior to the digital $\Delta\Sigma$ modulator [56]. Unfortunately, this approach requires the highpass response of the digital pre-emphasis filter to be a reasonably close match to the inverse of the closed-loop filtering imposed by the largely analog PLL. Another of the solutions is to use a high-order loop filter in the PLL with a sharp lowpass response [57]. Increasing the order of the loop filter increases the attenuation of out-of-band quantization noise which allows for higher order $\Delta\Sigma$ modulation to reduce in-band quantization noise thereby allowing the loop bandwidth to be increased without increasing the total phase noise. However, as described in [57], this necessitates the use of a Type 1 PLL which significantly complicates the design of the phase detector. Yet another solution is to use a narrow loop bandwidth but modulate the VCO both through the digital $\Delta\Sigma$ modulator and through an auxiliary modulation port at the VCO input [55]. The idea is to apply the low-frequency modulation components at the $\Delta\Sigma$ modulator input and the high-frequency modulation components directly to the VCO. Again, matching is an issue, but it has proven to be a manageable issue at least for low-end applications such as Bluetooth transceivers.

## IV. Conclusion

The basic concepts underlying $\Delta\Sigma$ data converters and the application of these data converters to the tasks of modulation and demodulation in wireless transceivers have been presented. A second-order $\Delta\Sigma$ modulator with multibit quantization has been used as an example with which to explain $\Delta\Sigma$ modulation in general. It has been shown how $\Delta\Sigma$ modulation forms the basis of $\Delta\Sigma$ ADCs, $\Delta\Sigma$ DACs, and $\Delta\Sigma$ fractional-$N$ PLLs. Throughout, the goal has been to provide a thorough yet practical understanding of the concepts rather than an enumeration of the various topologies. In terms of their application to wireless transceivers, the focus of the presentation has been on the use of delta–sigma data converters for the critical tasks of modulation and demodulation and their implications with respect to the overall radio architecture. It has been argued that, in this context, $\Delta\Sigma$ data converters have proven to be enabling components in highly integrated wireless handset transceivers.

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