A PERFORMANCE ANALYSIS OF THE PARTIAL RANDOMIZATION DYNAMIC ELEMENT MATCHING DAC ARCHITECTURE

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ABSTRACT

This paper presents the results of a performance analysis of a novel dynamic element matching technique for low harmonic distortion digital-to-analog converters. The technique promises to be suitable for applications such as direct digital synthesis systems, wherein low hardware complexity is essential in addition to low harmonic distortion. As the main result of the analysis, the DAC can be designed such that the hardware complexity is reduced to a minimum while still providing a given least required spurious-free dynamic range.

1. INTRODUCTION

A new dynamic element matching (DEM) technique for low-harmonic distortion DACs that promises to be applicable in DDS for wireless communication systems was recently introduced [1], [2]. The DEM technique performs as well as the prior art in suppressing harmonic distortion [3], [4], but has the additional benefit of significantly reduced hardware complexity. Two versions of the DEM technique were introduced: *Full Randomization DEM* (FRDEM) and *Partial Randomization DEM* (PRDEM). With the assumption of static DAC-element errors being the only source of non-ideal DAC behavior, the performance of FRDEM was completely quantified in [2]. As a main result, it was proven that FRDEM completely eliminates harmonic distortion and thus—in principle—provides an infinite spurious-free dynamic range (SFDR).

In practice, however, non-ideal circuit behavior other than static DAC-element errors imposes a limit on the SFDR achievable by the DAC. Non-idealities such as clock-skew, clock coupling, and finite slew-rates inevitably contribute to harmonic distortion. PRDEM was motivated by a combination of this fact and the simulation-based finding that it offers great suppression of harmonic distortion with a considerable reduction in the hardware requirement compared to FRDEM.

This paper presents the results of an analysis of the performance of PRDEM [5], stating theoretical results and showing simulation data that support the theory. While the results are applicable to the DAC architecture of any bit-resolution of interest, the 8-bit version is considered in detail. For this example DAC, the analysis is used to quantify the hardware requirement given a desired minimum SFDR and given knowledge of the statistics of the static DAC-element errors.

2. ARCHITECTURE

The high-level topology of an example 8-bit version of the proposed DAC is shown in Fig. 1. The digital input, $x[n]$, is a sequence of unsigned 8-bit binary numbers less than 2^8, i.e, $x[n] \in \{0, 1, \ldots, x_{max}\}$, $x_{max} = 255$. The DAC consists of 3 layers of digital devices, each device referred to as a *switching block*, followed by an array of *DAC-banks* and an analog output summing node. The functional details of the DAC-bank are described shortly. The layers are numbered 6 through 8. Each switching block is labeled $S_{k,m}$, where k denotes the layer number and m denotes the position of the switching block in the layer. Each DAC-bank is labeled DB_i and a total of 8 DAC-banks are employed.

In general, for a b-bit DAC, the number of layers, I, is referred to as the *randomization index* and satisfies $1 \leq I \leq b-1$. The layers are numbered R through b, where $R = b - I + 1$. Thus, for the 8-bit example DAC of Fig. 1, $I = 3$ and $R = 6$. A total of 2^I DAC-banks are employed in a DAC with randomization index I.

Fig. 2a shows the details of the switching block $S_{k,m}$. The switching block has one $k+1$-bit input, two k-bit outputs, and an input for a *random control bit*, $c_k[n]$. This random control bit is common to all the switching blocks in the k^{th} layer, and is ideally a white random bit-sequence, statistically independent of the random control bits applied to the other layers. The switching block $S_{k,m}$ operates such that when $c_k[n]$ is high, the MSB of the binary input is mapped to all k bits of the top output, and the remaining k bits of the input are mapped directly to the k bits of the bottom output. When $c_k[n]$ is low, the situation is as above, except the mappings are interchanged. In layer b, the DAC input $x[n]$ is assigned to the $S_{b,1}$ input bits b_2 through b_{k+1}, and a zero is assigned to the input bit b_1, as indicated in Fig. 1. It follows that $S_{k,m}$ can be implemented using one random control bit and k binary switches.

Fig. 2b shows the functional details of the i^{th} DAC-bank. The DAC-bank has one 6-bit input, $x_{5,i}[n]$, and one analog output, $y_i[n]$, and consists of a 5-bit conventional DAC, a 1-bit conventional DAC, and an analog summing node. The outputs of the 5-bit and 1-bit conventional DACs are denoted $y_{5,i}[n]$ and $y_{1,i}[n]$, respectively. In general, for a b-bit DAC with randomization index I, the DAC-bank has a $b - I + 1$-bit wide input, and employs a $b - I$-bit conventional DAC and a 1-bit conventional DAC. The input to the $b - I$-bit conventional DAC consists of the $b - I$ MSBs of the DAC-bank input, interpreted as a sequence of unsigned integers in the range $0, 1, \ldots, 2^{b-I} - 1$. The input to the 1-bit conventional DAC is the LSB of the DAC-bank input. The output of the DAC-bank is formed as the sum of the outputs of the two conventional DACs.

It can be shown that for a b-bit version of the DAC with randomization index I, the number of binary switches required is $(b - I + 2)2^I - b - 2$. The number of random control bits required is simply I. Thus, the example 8-bit DAC with randomization index 3 requires merely 46 binary switches and 3 random control bits.

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3. PERFORMANCE DETAILS

It follows from the functional details of the DAC-bank of Fig. 2b that it can be viewed as a conventional 32-step DAC. In general, the DAC-bank can be viewed as a conventional 2^{b-I}-step DAC. The 5-bit and 1-bit conventional DACs operate according to $y_{5,i}[n] = \sum_{j=1}^{5}\left(2^{j-1}x_{5,i}^{(j)}[n] + e_i^{(j)}[n]\right)$ and $y_{1,i}[n] = x_{5,i}^{(0)}[n] + e_i^{(0)}[n]$, respectively, where the $e_i^{(j)}[n]$ are errors in the analog output levels such that

$$e_i^{(j)}[n] = \begin{cases} e_{h_i}^{(j)} & \text{if } x_{5,i}^{(j)}[n] = 1; \\ e_{l_i}^{(j)} & \text{if } x_{5,i}^{(j)}[n] = 0. \end{cases} \quad (1)$$

The errors in the analog output levels of the 5-bit and 1-bit conventional DACs are assumed to be time-invariant [3], but otherwise arbitrary, and are referred to as *static DAC-element errors.*

As shown in [2], interconnecting the switching blocks and DAC-banks in the network of Fig. 1 results in a DAC for which $y[n] = x[n]$ in the absence of static DAC-element errors. However, with non-zero static DAC-element errors, the DAC output has the form

$$y[n] = \alpha x[n] + \beta + e[n],$$

where α is a constant gain, β is a DC offset, and $e[n]$ is a conversion error term referred to as *DAC noise.* Thus, all harmonic distortion of the DAC is included in $e[n]$, and the purpose of PRDEM is to attenuate the harmonic distortion by decorrelating $e[n]$ from $x[n]$ to a high degree.

The simulated performance of an example 8-bit version of the proposed DAC is presented in Fig. 3. Each graph in the figure shows the simulated power spectral density (PSD) of $y[n]$ relative to x_{max}^2 of the DAC driven by a dithered and DC offset sinusoid. Fig. 3a corresponds to an ideal DAC (i.e., a DAC with no static DAC-element errors, so $y[n] = x[n]$), Fig. 3b corresponds to a DAC with non-zero static DAC-element errors but no random switching, and Figs. 3c-d correspond to a DAC with non-zero static DAC-element errors and randomization index 2 and 3, respectively. The static DAC-element errors were the same for Figs. 3b-d, and were chosen randomly from a normal distribution with a standard deviation of 0.5%.

It should be mentioned that this particular choice of static DAC-element errors is for demonstration purposes only; the underlying statistical distributions and correlation properties are arbitrary.

As is evident from the numerous spurs distributed across the spectrum in Fig. 3b, quite severe harmonic distortion results from the static DAC-element errors in the absence of random switching. The maximum-amplitude spur occurs at a frequency of approximately 1.5π radians, and has power 69.8 dB below the power of the desired sinusoidal signal. Additional simulations using other sinusoid frequencies similarly support this finding. Thus, the SFDR provided by the DAC of this example is 69.8 dB. The simulation data of Figs. 3c-d indicate that the SFDR rapidly increases as the randomization index increases; the SFDRs provided by the DAC are 89.5 dB and 97.6 dB, respectively.

A theoretical analysis of PRDEM is given in [5]. For the purposes of this presentation, the main results of the analysis will be stated here without proof, although the theoretical results will be supported by simulations. Consider a b-bit version of the proposed DAC architecture with randomization index I. Let $x[n]$ be a deterministic input sequence and let $x^{(j)}[n]$ denote the j^{th} bit of $x[n]$, $1 \le j \le b$. In accordance with the usual definitions, let the time-average mean of a sequence $x[n]$ be defined as

$$\overline{M}_x = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x[n],$$

and let the time-average autocorrelation of $x[n]$ be defined as

$$\overline{R}_{xx}[k] = \lim_{P\to\infty} \frac{1}{P}\sum_{n=1}^{P} x[n]x[n+k].$$

The two main theoretical results of [5] can now be stated as follows:

Result 1. *The DAC output can be written in the form*

$$y[n] = \alpha x[n] + \beta + e[n] \quad (2)$$

where

$$e[n] = w[n] + s[n], \quad (3)$$

and $w[n]$ is a zero-mean, white random process of the form

$$w[n] = \sum_{i=1}^{b} w^{(i)}[n]x^{(i)}[n], \quad (4)$$

and $s[n]$ is a deterministic sequence of the form

$$s[n] = \sum_{i=1}^{R-1} s_i\, x^{(i)}[n]. \quad (5)$$

Formulae for the constants α and β in (2) and for $w^{(i)}[n]$ in (4) and s_i in (5) are developed in [5]. For the purposes of this presentation, it suffices to know that the $w^{(i)}[n]$ are zero-mean, white random processes, and that the constant coefficients α, β, and s_i depend only upon the static DAC-element errors.

Result 2. *If $\overline{M}_x$ and $\overline{R}_{x_s x_s}[k]$ exist, then*

$$\overline{R}_{yy}[k] = \overline{R}_{x_s x_s}[k] + \overline{\eta} + \overline{\sigma}^2\delta[k], \quad (6)$$

with probability 1, where

$$\overline{\eta} = 2\beta\overline{M}_{x_s} + \beta^2, \quad (7)$$

and

$$\overline{\sigma}^2 = \sum_{i=1}^{b} \gamma_i\, \overline{M}_{x^{(i)}} + \sum_{j=1}^{b-1}\sum_{i=j+1}^{b} \gamma_{i,j}\, \overline{M}_{x^{(i,j)}}. \quad (8)$$

In (6), $x_s[n]$ *is the sequence resulting from lumping* $\alpha x[n]$ *and* $s[n]$ *together, i.e.,*

$$x_s[n] = \alpha x[n] + s[n]. \tag{9}$$

Formulae for the constant coefficients γ_i and $\gamma_{i,j}$ in (8) are developed in [5]. For the purposes of this presentation, it suffices to know that these coefficients depend only upon the static DAC-element errors.

The validity of the detailed knowledge of the spurious content of $y[n]$ implied by Result 1 is demonstrated by computer simulation data in Fig. 4. Each plot shows the simulated PSD relative to x_{max}^2 of a selected signal of the 8-bit DAC used for the plots of Fig. 3 with the randomization index fixed at 3. Fig. 4a shows the sequence $y[n]-x[n]$. As expected from (2), the resulting sequence appears to consist of a scaled version of $x[n]$, white noise, and spurious tones. Fig. 4b shows $e[n]$ formed as the sequence $y[n]-\alpha x[n]-\beta$, and it appears to consist of white noise and spurious tones. Fig. 4c shows $w[n]$ formed as the sequence $y[n]-\alpha x[n]-\beta-s[n]$, where $s[n]$ is given by (5). As expected, $w[n]$ appears to be zero-mean white noise. Fig. 4d shows the corresponding $s[n]$ computed using (5). Notice that superimposing the data of Fig. 4c and Fig. 4d yields the data of Fig. 4b, as expected from (3). The power of $w[n]$ is given by (8), and the validity of this expression can also be demonstrated using the simulation data of Fig. 4. Specifically, evaluating (8) for the simulated values of static DAC-element errors and the input sequence applied to the DAC yields a power of $w[n]$ of $\overline{\sigma}^2 = -75.44$ dB relative to x_{max}^2. Numerically integrating the data of Fig. 4c results in -75.43 dB relative to x_{max}^2, in agreement with theory.

Result 1 will be used in the following to develop a simple expression for the minimum SFDR provided by the DAC. A few definitions helpful in this development are given next. To this end, let $\mathcal{I}^+ = \{\, i : s_i > 0 \,\}$ and $\mathcal{I}^- = \{\, i : s_i < 0 \,\}$, and let $s^+ = \sum_{i\in\mathcal{I}^+} s_i$ and $s^- = \sum_{i\in\mathcal{I}^-} s_i$. Furthermore, let $A_{s_{max}} = (s^+ - s^-)/2$. Parseval's relation states that the power of $s[n]$ equals the sum of the powers of the distinct spurs occurring in the PSD of $s[n]$. Since $s[n]$ is real, its PSD is symmetric and worst-case SFDR performance occurs when the power of $s[n]$ is at maximum and its PSD consists of only *two* distinct spurs corresponding to non-zero frequencies ω_s and $-\omega_s$. Since $x^{(i)}[n] \in \{\, 0, 1 \,\}$, it follows from (5) that $s^- \le s[n] \le s^+$. Thus, worst-case total spur power is $A_{s_{max}}^2$, and the power of each spur is bounded by $A_{s_{max}}^2/2$. The amplitude of any sinusoidal component of $y[n]$ is bounded by $|\alpha x_{max}/2|$. Since $y[n]$ is real, the maximum power of any frequency component is $(\alpha x_{max})^2/8$. These derivations yield:

$$\text{Minimum SFDR} = 20\log_{10}\Big(\frac{\alpha x_{max}}{2A_{s_{max}}}\Big)\ \text{dB}. \tag{10}$$

With knowledge of the statistical distribution of the static DAC-element errors, (10) allows for an IC fabrication yield estimation of the minimum SFDR. The yield estimation procedure used in the following is based upon the idea of computing a large number of samples of the parameter of interest for a given level of static DAC-element errors, thereby generating data that closely resemble the corresponding statistical distribution of the parameter. An example of this is shown in Fig. 5. Specifically, the figure shows the minimum SFDR for the 8-bit version of the DAC as a function of the randomization index and static DAC-element errors, which were chosen randomly from a normal distribution with a standard deviation ranging from 0.05% to 2%. Fig. 5a-d show the smallest of the largest 95%, 65%, 35%, and 5% values, respectively. For example, with a standard deviation of 0.5% and a randomization index of 3, the data of Fig. 5a predicts that merely 5% of all 8-bit DACs provide at least 90.3 dB SFDR, while the data of Fig. 5d predicts that 95% of all 8-bit DACs provide at least 77.7 dB SFDR. Thus, with a high degree of probability,

$$77.7\ \text{dB} \le \text{Minimum SFDR} \le 90.3\ \text{dB}. \tag{11}$$

The above estimate for the minimum SFDR may at first glance seem overly conservative given that the example 8-bit DAC of Fig. 3 achieved an SFDR of 97.6 dB with randomization index 3. Recall, however, that the yield estimation data represents worst-case performance data, where it is assumed that all power in $s[n]$ is concentrated in *two* spurs occurring at frequencies $+\omega_s$ and $-\omega_s$. When driving the DAC by a sinusoid, typically *many* spurs occur in the PSD of $e[n]$, as observed in Fig. 6a, which is Fig. 4d repeated for convenience. The occurrence of numerous spurs results in decreased power of the maximum-amplitude spur—and thus an increased SFDR—relative to worst-case performance data. Fig. 6b shows the PSD of $e[n]$ of the same 8-bit DAC used for the plot of Fig. 6a, but driven by a sequence $x[n]$ chosen such that the resulting PSD of $s[n]$ consists of exactly two spurs (and a DC component). In this case, the maximum-amplitude spur has power -88.3 dB relative to $(\alpha x_{max})^2/8$, in support of (11).

4. CONCLUSION

The results of an analysis of PRDEM originally proposed in [1] have been presented. It was shown that harmonic distortion is increasingly suppressed as the randomization index is increased.

The IC fabrication yield estimation data of the minimum SFDR of the 8-bit version allowed for a determination of the minimum hardware requirement of the DAC given a desired minimum SFDR and given knowledge of the statistics of the static DAC-element errors.

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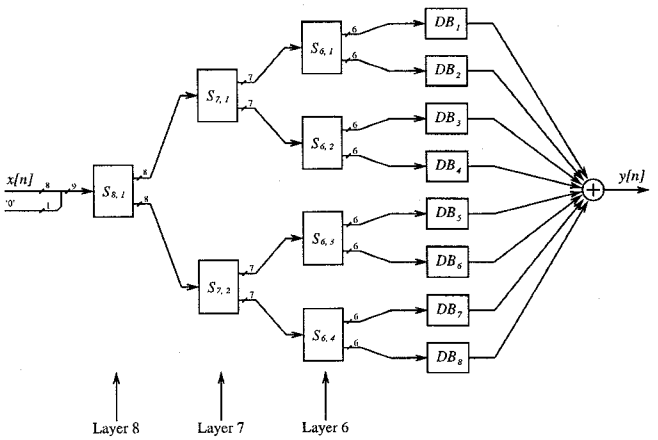
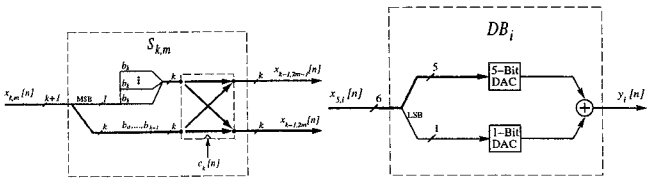
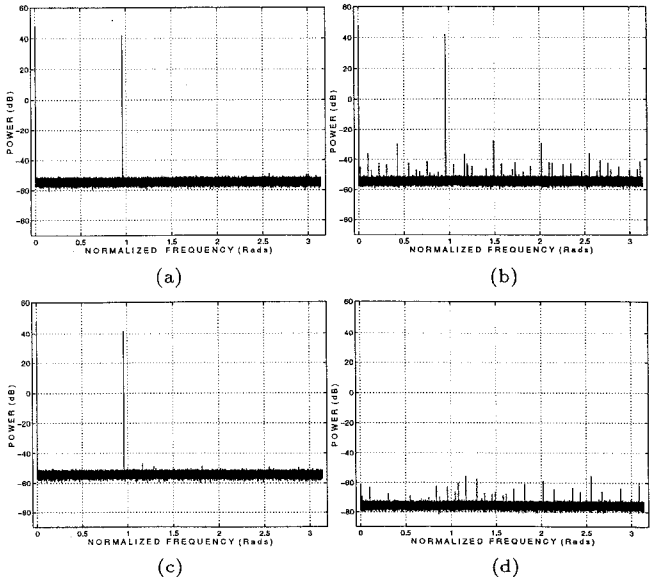


Figure 1: An 8-bit DAC with randomization index 3.



(a) (b)

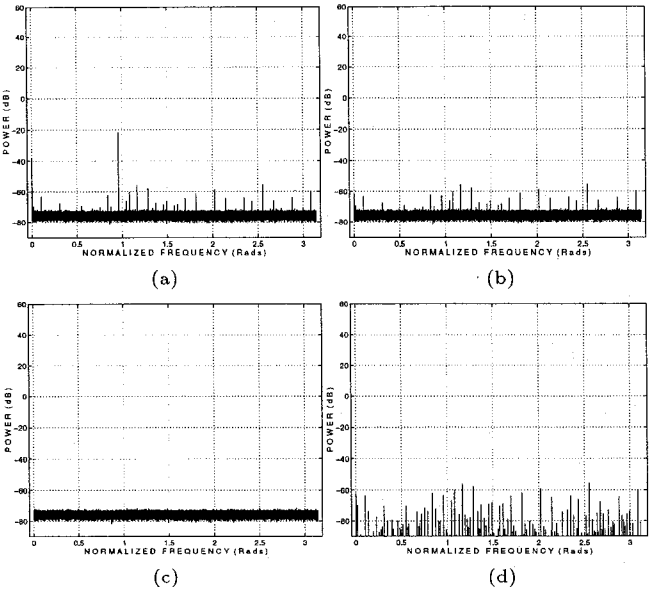
Figure 2: Details of (a) the switching block and (b) the DAC-bank.



(a) (b)

(c) (d)

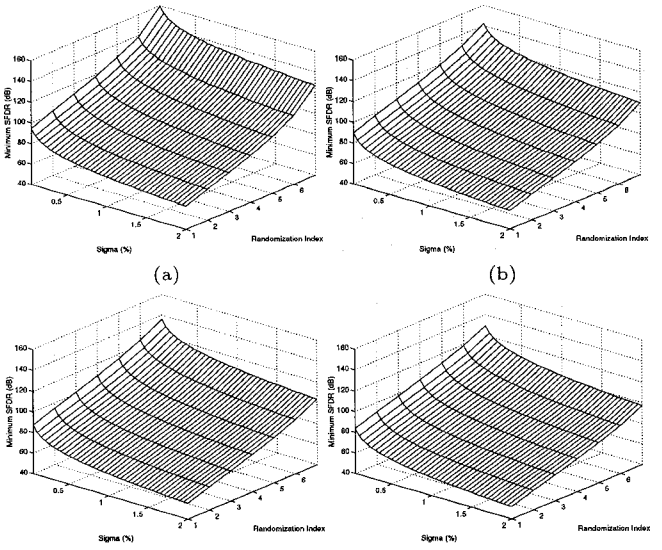
Figure 3: Simulated PSDs of the example 8-bit DAC.



(a) (b)

(c) (d)

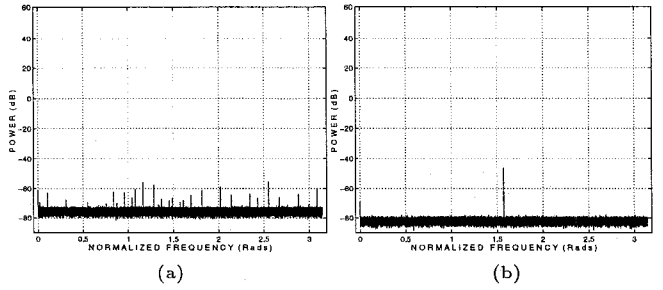
Figure 4: Simulated PSDs of the example 8-bit DAC.



(a) (b)

(c) (d)

Figure 5: Yield estimation data of the minimum SFDR provided by the 8-bit version.



(a) (b)

Figure 6: Simulated PSDs of the example 8-bit DAC.