CLOCK DISTRIBUTION USING COUPLED OSCILLATORS

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ABSTRACT

This paper presents a robust, low complexity clock distribution technique applicable to both printed circuit boards and integrated circuits. The technique exploits the natural tendency of certain oscillators to lock in frequency and nearly lock in phase when coupled together. Experimental and theoretical results are presented that indicate the technique has the potential to dramatically reduce clock skew in digital circuits. A clock distribution architecture using the technique is proposed.

1. INTRODUCTION

Periodic clock signals must be delivered simultaneously to physically separate locations in synchronous digital circuits. The clock signal provides a time reference that keeps the various components of the circuit operating in lock-step. However, the clock signals must be distributed from a common clock source (such as a crystal oscillator), and clock distribution networks typically consist of metal interconnections and clock drivers, both of which introduce propagation delay. In principle, the propagation delay would not be a problem if all the clock signals suffered exactly the same delay. Indeed, most clock distribution techniques attempt to introduce exactly the same delay between the clock source and all the distribution points in the circuit [1], [2]. Unfortunately, this is hard to accomplish precisely because of variability in the propagation delays introduced by fabricated interconnections and clock drivers. The resulting difference in the clock phase between two separate points in the circuit is called *clock skew*, and if large enough, can result in improper circuit function. This problem is particularly evident in printed circuit board design, but as clock speeds are driven ever higher, the problem arises in integrated circuits as well [3].

This paper introduces a clock distribution method that is based on a network of strongly coupled RC oscillators. The technique exploits the tendency of coupled oscillators to lock together in frequency. This is a well known phenomenon that is often called *oscillator pull* or *injection locking* [4], [5], [6]. What is not generally known is that RC oscillators, if approximately matched in frequency and amplitude, will not only lock in frequency, but will also take on nearly the same phase when their outputs are coupled through nearly lossless transmission lines that are less than a quarter wavelength long. Typical metal traces on integrated circuits and printed circuit boards meet these constraints [7].

To the extent that the oscillators phase-lock to each other, they set up a standing wave causing all points along the transmission lines to be in phase. A network of perfectly phase-locked oscillators would provide a clock reference that has zero skew. Since real oscillators do not obtain perfect phase-locking, there will always be some phase skew. However, it is demonstrated here that skew from this source is small relative to the transmission line delays. Previously, in [8], a single oscillator was used to form a standing wave for backplane synchronization of a multicomputing system running at 160 MHz. Although a better than ten-fold reduction in clock skew was achieved, the approach required near lossless reflections of the clock signal at the loading points to maintain the standing wave. The technique presented here, which uses a network of oscillators to form the standing wave, avoids this requirement.

2. EXPERIMENTAL RESULTS

To experimentally demonstrate the idea, the clock distribution circuit shown in Fig. 1 was constructed on a printed circuit board using discrete components. As indicated in Fig. 1a, a network of three RC oscillators with outputs labeled C_0, C_1, and C_2 are coupled together with a $7.5''$ microstrip joining C_0 and C_1, and an $8.0''$ microstrip joining C_1, and C_2. The microstrips are represented schematically in Fig. 1a as transmission lines. The oscillators are nominally identical but no effort has been made to match them. As shown in Fig. 1b, each consists of an npn transistor and a pnp transistor in a push-pull configuration followed by an RC lowpass filter and digital inverter. The output of the digital inverter is also the oscillator output and is fed back to the bases of the two transistors. The finite slew rate of the inverter combined with the hysteresis of the push-pull pair causes instability. The frequency of oscillation is set (within limits) by the choice of R and C. A jumper between the output of the digital inverter and the feedback path, labeled S_1, allows the oscillator to be disabled for demonstration purposes. When the jumper is closed, the oscillator is enabled and oscillates normally; when it is open the oscillator is disabled and does not oscillate.

A simple experiment using this circuit provides convincing evidence that a clock distribution system based on strongly coupled oscillators is practical. The oscilloscope image of Fig. 2a shows measured signals corresponding to C_0, C_1, and C_2 with C_1, and C_2 disabled. Thus, the oscillator corresponding to C_0 is driving the microstrip transmission lines, the oscilloscope probes, and the push-pull transistor pairs of the other two oscillators. The three signals shown in the oscilloscope image, from largest-amplitude to smallest-amplitude correspond to C_0, C_1, and C_2, respectively. As indicated in the figure, there is approximately $2.5ns$ of skew between C_0, and C_1, and $5ns$ of skew between C_0, and C_2.

The oscilloscope image of Fig. 2b shows the voltages at the same points in the circuit except that all three oscillators are enabled. The oscillators have very nearly

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the same phase with a common frequency of 91.8 MHz. It follows that a nearly perfect standing wave must exist on the microstrip transmission lines joining the oscillators. Clearly, by coupling the outputs of the enabled oscillators, the system has become self-synchronized.

The oscillator design used in this experiment was chosen for practical reasons. However, the authors have observed similar phase-locking characteristics using other RC oscillators including Wien-bridge oscillators, multivibrators, and Van der Pol oscillators.

3. PRACTICAL CONSIDERATIONS

There are two practical issues concerning coupled oscillator clocking that need to be addressed. The first is the issue of establishing a precisely controlled operating frequency. Fig. 3 shows a proposed clock distribution architecture that uses coupled oscillators. It consists of an analog phase detector, a first-order analog filter, and N voltage controlled oscillators (VCO's). The VCO's are output coupled through metal lines represented schematically as transmission lines. The output of the top VCO in the figure is phase compared to a reference clock by the phase detector. The output of the phase detector is filtered and the resulting signal is used as the (low frequency) control signal for all the VCO's. When the VCO's lock in frequency, they behave as a single "distributed" VCO and the overall system has the topology of a standard second-order phase-locked-loop (PLL). Any difference between the phase of the standing wave and the phase of the reference clock causes the phase detector and filter combination to generate a low frequency error signal that gradually adjusts the common VCO frequency so as to reduce the difference. Since the reference signal will have a very narrow bandwidth, and rapid lock-acquisition is not essential, the loop bandwidth of the PLL can be made very small. This allows the VCO's to lock without being significantly affected by the PLL dynamics.

The second practical issue is how to provide an approximately square-edged clock signal rather than the sinusoidal signal appearing in Fig. 2. One approach is to distribute the clock signal using a sinusoidal standing wave and convert to a digital signal where needed using a hard-limiter. This approach was used successfully in [8]. Another approach is to use a non-sinusoidal, square-edged, standing wave that would not require conversion. The advantages and disadvantages of both approaches are discussed in [9].

4. THEORY

For the purpose of understanding the near phase-locking behavior of the oscillators, the theoretical treatment of coupled oscillators is reduced to two idealized oscillators (called Oscillator A and Oscillator B) coupled through a lossless transmission line of length, ℓ, characteristic impedance, Z_0, and velocity of propagation, ν. Since frequency locking has been observed under a wide range of conditions in simulation, experiment and throughout the literature, it is assumed in this analysis that the oscillators lock in frequency. The goal is to calculate the steady-state phase difference between the two oscillators and compare this difference with simulation. The phase difference represents a small power transfer (in the form of a traveling wave) between the oscillators and results from the inevitable mismatch of their free-running frequencies and amplitudes. It is this small power transfer that allows non-identical oscillators to run at the same frequency when coupled.

4.1 An Idealized Oscillator Example

An idealized version of the experimental oscillator is shown in Fig. 4a. It consists of a hysteresis generating element with a *dead zone* of width V_d, an input RC network with time constant $\tau_1 = R_1C_1$, a gain element of gain $-G$, and an output RC network with time constant $\tau_2 = R_2C_2$. The voltage across capacitor C_1 is labeled v_1 and the voltage across capacitor C_2 is labeled v_2. Voltage v_2 is the oscillator output and is fed back to the input of the hysteresis generating element. The hysteresis element models the push-pull pair in the experimental oscillator but is idealized to have infinite input impedance and zero output impedance. Similarly, τ_1 simulates the actual RC network, while the gain element and τ_2 simulate the actual inverter. Notice that if the hysteresis element is replaced by a short, the circuit is a second order, linear system and is under-damped for sufficiently large gain; it will ring given an initial impulse, however it will not sustain an oscillation. With the hysteresis in place, the oscillator becomes unstable and oscillates at a frequency determined by G, τ_1, and τ_2, and an amplitude determined by V_d.

Although the system is nonlinear, it can be modeled exactly using an extension of linear systems theory. In the time domain, the time axis can be broken into regions within which the hysteresis element is inside or outside of its dead zone. These two regions of operation can each be represented using linear O.D.E.'s, and an overall solution can be found by matching solutions at the boundaries of the regions. When the oscillator is operating outside of the hysteresis dead zone it is equivalent to the closed-loop system shown in Fig. 4b, called *System 1*, with capacitor voltages $v_1^{(1)}(t)$ and $v_2^{(1)}(t)$. The DC voltage source, $V_o^{(1)}$, shown in the figure takes on the value $\frac{V_d}{2}$, the offset voltage of the hysteresis element. When the oscillator is operating in the dead zone of the hysteresis element, it is equivalent to the open-loop system shown in Fig. 4c, called *System 2*, with capacitor voltages $v_1^{(2)}(t)$ and $v_2^{(2)}(t)$. The DC voltage source, $V_o^{(2)}$, shown in the figure maintains a constant hysteresis output voltage.

The oscillator frequency and amplitude are determined exactly by performing the following procedure:

1) In System 1 with initial conditions $t = 0$, $v_1^{(1)}(0) > 0$, $v_2^{(1)}(0) = 0$ and $V_o^{(1)} = \frac{V_d}{2}$, calculate $v_1^{(1)}(t)$ and $v_2^{(1)}(t)$ until $t = t_1$, where t_1 is the minimum time such that $t_1 > 0$ and $\frac{dv_2^{(1)}}{dt}(t_1) = 0$;
2) In System 2 with $v_1^{(2)}(t_1) = v_1^{(1)}(t_1)$, $v_2^{(2)}(t_1) = v_2^{(1)}(t_1)$, and $V_o^{(2)} = V_o^{(1)} + v_2^{(1)}(t_1)$ calculate $v_1^{(2)}(t)$ and $v_2^{(2)}(t)$ until $t = t_2$, where t_2 is the minimum time such that $t_2 > t_1$ and $|v_2^{(2)}(t_2) - v_2^{(2)}(t_1)| = V_d$;
3) In System 1, with $v_1^{(1)}(t_2) = v_1^{(2)}(t_2)$, $v_2^{(1)}(t_2) =$

$v_2^{(2)}(t_2)$ and $V_o^{(1)} = V_o^{(2)} - v_2^{(2)}(t_2)$ calculate $v_1^{(1)}(t)$ and $v_2^{(1)}(t)$ until $t = t_3$, where t_3 is the minimum time such that $t_3 > t_2$ and $\frac{dv_2^{(1)}}{dt}(t_3) = 0$;

4) Let $t_1 = t_3$ and repeat from Step 2 until steady-state conditions are reached.

4.2 Transmission Line Results

Because steady-state conditions are assumed, each oscillator sees an admittance load imposed by the transmission line and the other oscillator. The admittance seen by Oscillator A, Y_A, was derived in terms of the amplitudes of the two oscillators, V_A and V_B, and the phase difference between them, $\phi = \phi_A - \phi_B$, by considering the superposition of all possible sinusoidal standing waves and traveling waves at a particular frequency, ω. The details of the derivation are presented in [9]. The real and imaginary parts of the admittance are given by

$$\mathrm{Re}\{Y_A\} = \frac{1}{Z_0}\frac{V_B}{V_A}\frac{\sin\phi}{\sin\theta_\ell}, \tag{1}$$

and

$$\mathrm{Im}\{Y_A\} = \frac{1}{Z_0}\left[\frac{V_B}{V_A}\cos\phi\left(\tan\frac{\theta_\ell}{2} + \cot\theta_\ell\right) - \cot\theta_\ell\right], \tag{2}$$

respectively, where $\theta_\ell = \frac{\omega\ell}{\nu}$ is the *electrical length* of the transmission line. The real and imaginary parts of Y_A can be represented as a resistance, R_A, and a capacitance, C_A, in parallel, where

$$R_A = \frac{1}{\mathrm{Re}\{Y_A\}}, \qquad \text{and} \qquad C_A = \frac{\mathrm{Im}\{Y_A\}}{\omega}. \tag{3}$$

The parallel resistance, R_B, and capacitance, C_B, representing the transmission line load as seen by Oscillator B, are calculated with the same formulas except with the A and B subscripts interchanged.

4.3 Outline Of Analytic Procedure

Although the frequency and amplitude of the idealized oscillator can be determined precisely by the analysis described in Section 4.1, explicit formulas for these quantities in terms of the oscillator parameters are not (yet) available. This prevents the most direct method of solving for ϕ, namely substituting expressions for V_A, V_B, and ω into (1) and (2). However, for the purpose of providing a theoretical calculation of ϕ to compare with simulation, an indirect method is employed. Note that, by symmetry, if both Oscillator A and Oscillator B were identical, then ϕ would be zero; ϕ is non-zero only when one or more of Oscillator A's parameters are different from those of Oscillator B. With this in mind, the following analytic procedure is used:

1) Choose an operating frequency, ω, and desired transmission line parameters.
2) Find nominal oscillator parameters that cause the idealized oscillator pair and transmission line to operate at this frequency assuming that ϕ is zero. In this case it follows from (1), (2) and (3) that $R_A = \infty$, and $C_A = \frac{1}{\omega Z_0}\tan(\theta_\ell)$. This is done using the oscillator analysis described in Section 4.1 above, which also reveals the amplitude. Let this amplitude be V_A, the amplitude of Oscillator A.
3) Change the parameters G, R_2, or C_2 of Oscillator A, and then determine what changes in R_A and C_A are needed to exactly compensate for the parameter changes such that V_A and ω do not change. As shown in [9] and outlined below, this is always possible.
4) Use Equations (1) and (2) to calculate ϕ and V_B.
5) Calculate the loading of Oscillator B implied by Equation (3) (i.e. calculate R_B and C_B).
6) Calculate the values of G, R_2, and C_2 of Oscillator B required to make it run at ω, given that its load is R_B and C_B. If small changes were made in Step 3, then these values will be near the nominal values chosen in Step 2.
7) Calculate V_d for Oscillator B such that it will oscillate with amplitude V_B calculated in Step 4.

By comparing the differential equations that describe a loaded oscillator with those that describe an unloaded oscillator, it was found that an oscillator with gain G and output time constant τ_2, loaded with parallel resistor, R_L, and capacitor, C_L, is equivalent to the unloaded oscillator (i.e. $R_L = \infty$ and $C_L = 0$) with gain $\overline{G}$ and output time constant $\overline{\tau}_2$, where

$$G = \overline{G}\left(1 + \frac{R_2}{R_L}\right), \tag{4}$$

and

$$\tau_2 = \overline{\tau}_2\left(1 + \frac{R_2}{R_L}\right) - R_2 C_L. \tag{5}$$

Step 6 uses (5), solved for either R_2 or C_2, followed by (4), while Step 3 uses an inverted form of the equations where R_L and C_L have been solved for in terms of the desired gain ($\overline{G}$), the desired output time constant ($\overline{\tau}_2$), and the actual oscillator parameters (G, R_2 and C_2).

The procedure given above produces a two oscillator system that is frequency locked at a known frequency, with known, non-identical, oscillator parameters. In addition, the phase difference and amplitudes of the oscillators are known. This provides enough information to simulate this system using a simulation package such as PSpice for the purpose of comparison. Note that Steps 5, 6 and 7 are only necessary for the purpose of getting enough data to simulate the system. If only ϕ is desired, such as would be the case in a sensitivity study of ϕ versus variations in oscillator parameters, then there is no need to proceed beyond Step 4.

4.4 Comparison With Simulation

The analytic procedure given in Section 4.3 was carried out for nominal oscillator values of $V_d = 2$V, $G = 40$, $R_1 = 30\Omega$, $C_1 = 290$pf, $R_2 = 30\Omega$, and $C_2 = 284$pf, and transmission line values of $\ell = 10$cm, $Z_0 = 100\Omega$, and $\nu = 1 \times 10^{10} cm/s$ (Step 1). These parameters result in an operating frequency of 100 MHz and an amplitude of $V_A = 3.083$V (Step 2). The gain of Oscillator A was changed from 40 to 39.2 (Step 3) and ϕ and V_B were calculated to be $-.0498$ radians

and 2.427V, respectively (Step 4). Parameter values for Oscillator B were then calculated to be $V_d = 1.575$V, $G = 41.30$, and $R_2 = 30.22\Omega$ (Steps 5, 6 and 7 where R_1, C_1, and C_2 were left unchanged). PSpice was used to simulate the coupled oscillator system using these parameter values resulting in a frequency of 100.0 MHz, $V_A = 3.075$V, $V_B = 2.420$V and $\phi = -.0461$ radians. Note that both analysis and simulation predict a phase difference that is less than 0.8% of the clock period.

Analytical and simulated results for V_A, V_B and frequency agree to within 0.3%, yet there is a small discrepancy between the analytical and simulated values for ϕ (about 7.4%). It is caused by oscillator harmonics that are not accounted for in the impedance expressions used for the transmission lines. The analysis can be improved, however, by repeating the calculations outlined above for each harmonic of interest and superimposing the results as described in [9].

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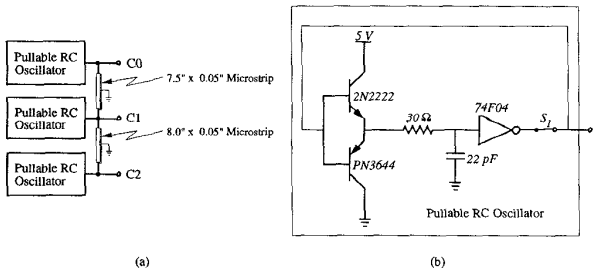

Figure 1: Schematic diagram of an experimental clock distribution circuit: a) three pullable RC oscillators coupled through 7.5" and 8.0" microstrips of width 0.05", b) the details of the pullable RC oscillators.

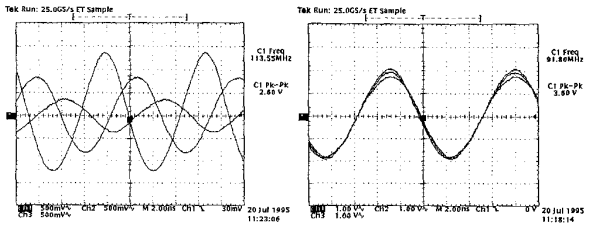

Figure 2: Oscilloscope images showing the measured waveforms corresponding to C_0, C_1, and C_2 in the experimental clock distribution circuit shown in Fig. 1; a) with only oscillator C_0 enabled; b) with all oscillators enabled.

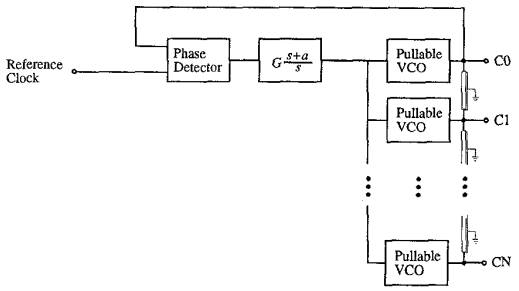

Figure 3: A proposed clock distribution architecture.

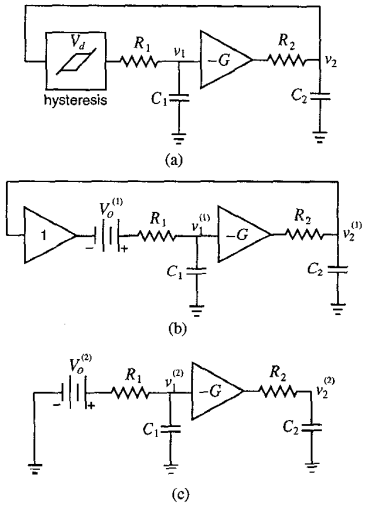

Figure 4: a) Idealized Oscillator, b) Idealized Oscillator out of dead zone (System 1), and c) Idealized Oscillator in dead zone (System 2).