Delta-Sigma Modulator Based A/D Conversion without Oversampling

Ian Galton, *Member, IEEE,* and Henrik T. Jensen, *Student Member, IEEE*

Abstract— Although $\Delta\Sigma$ modulators are widely used for low to moderate rate analog-to-digital conversion, the time oversampling requirement has discouraged their application to higher rate converters. This paper presents an architecture wherein multiple $\Delta\Sigma$ modulators are combined so that neither time oversampling nor time interlacing are necessary. Instead, the system achieves the effect of oversampling from the multiplicity of $\Delta\Sigma$ modulators. For a system containing M P^{th}-order $\Delta\Sigma$ modulators, approximately P bits of accuracy are gained for every doubling of M. A major benefit of the architecture is that it retains much of the robustness of the individual $\Delta\Sigma$ modulators to nonideal circuit behavior. As a result, the architecture offers the potential of integrating high-precision, high-speed A/D converters together with digital signal processing functions using VLSI processes optimized for digital circuitry. The paper presents the general architecture and provides a performance analysis closely supported by computer simulations.

I. INTRODUCTION

PRIMARILY because of advances in VLSI technology, oversampling $\Delta\Sigma$ modulator A/D converters have become popular in applications requiring high precision. Although they employ complicated digital circuitry, their relatively simple analog circuitry tends to be robust with respect to nonideal circuit behavior [1]. They generally do not require the trimmed components necessary in conventional high-precision A/D converters. Consequently, high-precision $\Delta\Sigma$ modulator A/D converters can be implemented using high-density VLSI processes optimized for digital circuitry. This allows integration of the A/D converter with other digital signal processing components. Such integration gives rise to smaller, more reliable, and less expensive systems.

One of the drawbacks of the approach is that time oversampling is required. Typically, to achieve a given precision, the input sample-rate of a $\Delta\Sigma$ modulator A/D converter must be significantly higher than the A/D conversion rate. For A/D conversion rates below a few MHz, the oversampling requirement has generally not been a significant problem. However, in higher-bandwidth applications such as video processing and digital radio the oversampling requirement has been prohibitive [1].

This paper presents a $\Delta\Sigma$ modulator-based A/D converter architecture, referred to as the $\Pi\Delta\Sigma$ modulator A/D converter, that avoids the time oversampling requirement, but

retains many of the attractive properties of conventional $\Delta\Sigma$ modulator A/D converters [2], [3]. The system achieves the effect of oversampling from the use of multiple noninterlaced $\Delta\Sigma$ modulators. For example, as will be shown, a system consisting of 16 sixth-order $\Delta\Sigma$ modulators with three-level quantizers in which all components are clocked at the A/D conversion rate can ideally achieve greater than 16 b of A/D conversion precision. In general, for a system containing M Pth-order $\Delta\Sigma$ modulators, approximately P bits of accuracy are gained for every doubling of M.

The remainder of the paper is divided into four main sections. Section II presents the A/D converter architecture. Section III provides a heuristic explanation of how the A/D converter works. Section IV in conjunction with two appendices presents the theory behind the A/D converter, and quantifies the ideal performance of the system. It also presents a design example with simulations and a hardware complexity estimate of the system. Section V presents an analysis of the A/D conversion error that can arise from nonideal analog circuit behavior and presents a modification of the architecture that digitally compensates for the error.

II. ARCHITECTURE

The $\Pi\Delta\Sigma$ modulator A/D converter architecture is shown in Fig. 1. It consists of M parallel channels that all operate on the input sequence, $x[n]$. On each channel, the input sequence is multiplied by a channel-specific ±1 sequence, delta-sigma modulated, lowpass filtered, and multiplied by a delayed version of the channel-specific ±1 sequence. The outputs of the channels are added to produce the overall output, $y[n]$.

The ±1 sequences are called *Hadamard sequences* and are denoted in Fig. 1 as $u_r[n]$, $0 \leq r \leq M - 1$. They are derived from an $M \times M$ Hadamard matrix, **H**.[1] Specifically, $u_r[n]$ is just the rth row of a Hadamard matrix repeated over and over again. Thus,

$$u_r[n] = m[r, n \bmod M], \tag{1}$$

where $m[j, k]$ is the element in the jth row and kth column of **H**.

Because Hadamard sequences are ±1 sequences, each multiplier shown in Fig. 1 need only change the sign of its input depending upon whether the current value of the Hadamard sequence is one or minus one, respectively. For the bank
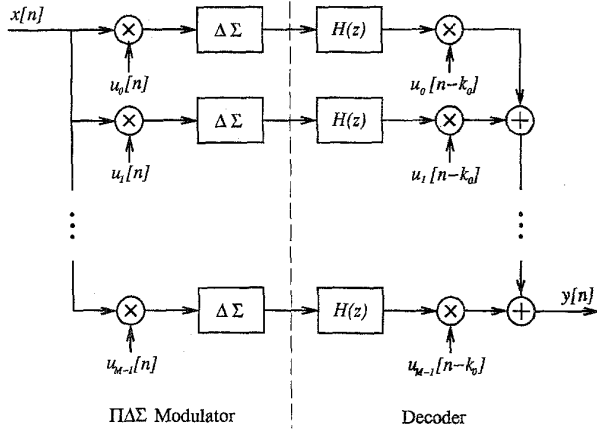
[1] A Hadamard matrix, **H**, consists exclusively of plus and minus ones and has the property that $\mathbf{H}^T \mathbf{H} = M\mathbf{I}$ where **I** is the identity matrix [4]

Fig. 1. The $\Pi\Delta\Sigma$ modulator A/D converter architecture.

Fig. 2. The $\Delta\Sigma$ modulator quantization error model.

Fig. 3. The $\Pi\Delta\Sigma$ADC quantization error model.

of multipliers prior to the $\Delta\Sigma$ modulators, this requires the capability of analog sign inversion. For those following the $H(z)$ filters it requires the capability of digital sign inversion. In general, the multipliers on one of the channels can be eliminated because one of the Hadamard sequences is typically an all-ones sequence.
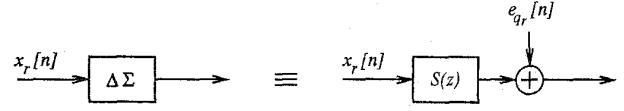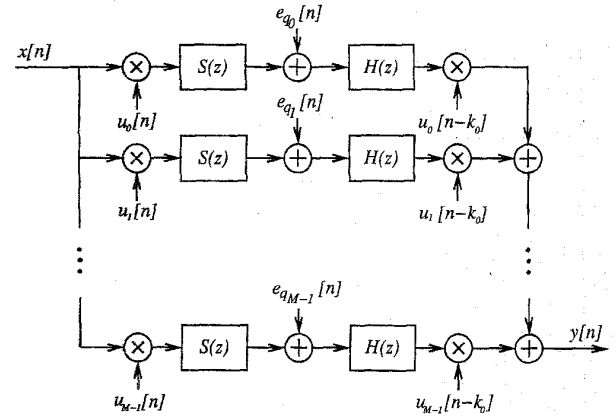
The use of Hadamard sequences requires that M be chosen such that there exists an $M \times M$ Hadamard matrix. A sufficient condition for this to occur is that M be a positive power of two. Several simple circuits for generating Hadamard sequences when M is a power of two have been presented [5]–[8]. Hadamard matrices also exist for which M is not a power of two. A necessary (and conjectured to be sufficient) condition for an $M \times M$ Hadamard matrix to exist is that M be a multiple of four, and Hadamard matrices for every multiple of four less than 428 are known [4].

As in conventional $\Delta\Sigma$ modulator A/D converters, various $\Delta\Sigma$ modulators can be used in the $\Pi\Delta\Sigma$ modulator A/D converter, but the specifics of the application and the constraints of the circuit technology determine which type of $\Delta\Sigma$ modulator is best for a given application. The channel filters, $H(z)$, depend on the type of $\Delta\Sigma$ modulators used. As will be shown, optimal channel filters can be found, but for P^{th}-order $\Delta\Sigma$ modulators, hardware-efficient comb^{P+1} filters work almost as well.

Throughout the paper, the following terminology is used. The portion of the system containing the analog ± 1 multipliers and the $\Delta\Sigma$ modulators is referred to as the $\Pi\Delta\Sigma$ modulator, and the portion containing the digital filters, digital ± 1 multipliers, and channel summers is referred to as the *decoder*. The full $\Pi\Delta\Sigma$ modulator A/D converter is referred to as the $\Pi\Delta\Sigma$ADC. The process of multiplying by a Hadamard sequence is referred to as *Hadamard modulation*, and the multipliers are referred to as *Hadamard modulators*.

III. HEURISTICS

In general, the output of a $\Delta\Sigma$ modulator is a coarsely quantized sequence (rarely more than a few bits) that, in the absence of circuit errors, can be viewed as the sum of a *signal*

component and a *quantization error component*. Therefore, as depicted in Fig. 2, a $\Delta\Sigma$ modulator is ideally equivalent to a linear time-invariant (LTI) filter, shown as $S(z)$, plus an additive quantization error source, shown as $e_{q_r}[n]$. The signal component is $x_r[n] * s[n]$, where $s[n]$ is the impulse response of $S(z)$, and the quantization error component is $e_{q_r}[n]$.

With this $\Delta\Sigma$ modulator model, the $\Pi\Delta\Sigma$ADC can be viewed as a linear system to which the M $\Delta\Sigma$ modulator quantization error components are added as depicted in Fig. 3. Accordingly, the $\Pi\Delta\Sigma$ADC output is a digital sequence that is the sum of an *overall signal component* and an *overall quantization error component*. That is,

$$y[n] = w[n] + e[n],$$

where $w[n]$ denotes the overall signal component and $e[n]$ denotes the overall quantization error component. By superposition, the overall signal component can be calculated by considering the quantization error components from the $\Delta\Sigma$ modulators to be zero.

As an example, consider a four channel $\Pi\Delta\Sigma$ADC with FIR filters of length-7. For simplicity, suppose that the $\Delta\Sigma$ modulators have $S(z) = 1$, so the overall signal component can be calculated by considering the $\Pi\Delta\Sigma$ modulator without the $\Delta\Sigma$ modulators. Fig. 4 shows the $\Pi\Delta\Sigma$ADC at time $n = n'$ with the $\Delta\Sigma$ modulators omitted. From top to bottom in the figure, the first four boxed subsystems are the $H(z)$ filters, and the fifth boxed subsystem generates the Hadamard sequences for channels 1-3 (the Hadamard sequence for channel-0 is an all-ones sequence).

As is evident from the values in the channel-0 $H(z)$ shift register, the value of $x[n]$ at time $n = n'$ is 7, and the previous six input values were 6, 5, 4, 3, 2, and 1, respectively. Notice that the values in the other $H(z)$ shift registers have these
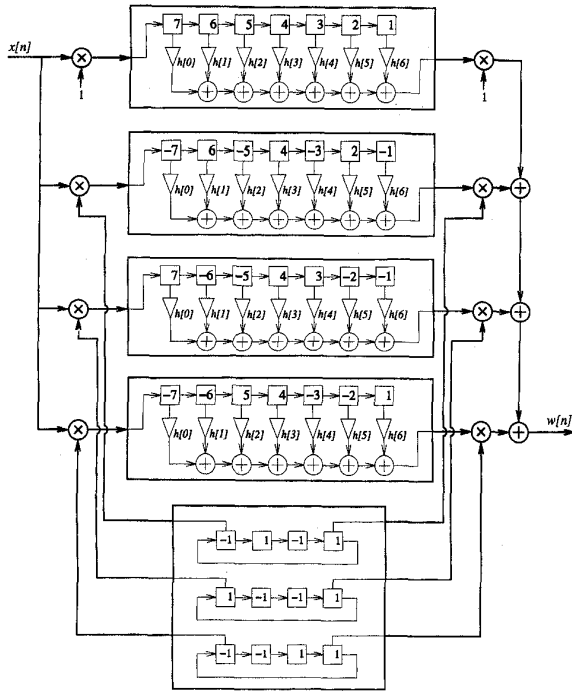
Fig. 4. An example of the processing performed by a four channel $\Pi\Delta\Sigma$ADC in the absence of quantization error.

same magnitudes because the Hadamard sequences are ± 1 sequences. The Hadamard sequences in the decoder happen to all be positive at time $n = n'$, so $w[n']$, is just the sum of all the $H(z)$ outputs. That is, $w[n']$ is the sum of the first taps of the four shift registers times $h[0]$ plus the sum of the second taps of the four shift registers times $h[1]$ and so on. However, as is evident from the figure, only the fourth taps of the four shift registers add to a nonzero number, so $w[n'] = 4 \cdot h[3]x[n'-3]$.

Now consider the system of Fig. 4 at the next time instant, $n = n'+1$. Each $H(z)$ shift register will be shifted one to the right, and its first tap will be loaded with $x[n'+1]$ because each Hadamard sequence in the $\Pi\Delta\Sigma$ modulator will be positive. The Hadamard sequences in the decoder will not all be positive, so $w[n'+1]$ is not just the sum of all the filter outputs. Instead, it is the sum of the zeroth and third filter outputs minus the sum of the first and second filter outputs. From the figure, it is easy to verify that $w[n'+1] = 4 \cdot h[3]x[n'+1-3]$. Continuing in this fashion it is evident that $w[n] = 4 \cdot h[3]x[n-3]$ for all n, so the overall signal component is simply a delayed and scaled version of the input sequence. A particularly important feature of this system is that the overall signal component only depends on the center coefficient of $H(z)$, namely $h[3]$. Even though the signal component from each $\Delta\Sigma$ modulator is filtered by $H(z)$, the Hadamard modulation evidently causes the effect of the filtering to be "undone."

The overall quantization error component, on the other hand, depends on all the coefficients of $H(z)$. This is because each $\Delta\Sigma$ modulator quantization error component is introduced just prior to $H(z)$, so the overall quantization error component is the sum the M $\Delta\Sigma$ modulator quantization error com-

ponents after they have been filtered by $H(z)$ and digitally Hadamard modulated. Since the $\Delta\Sigma$ modulator quantization error components were not Hadamard modulated prior to filtering, the effect of the filtering is not undone as in the case of the $\Delta\Sigma$ modulator signal components. If the $\Delta\Sigma$ modulator quantization error components have most of their power at high frequencies, the use of lowpass $H(z)$ filters can result in a significant attenuation of the quantization error contributed by each channel. As discussed in the next section, the quantization error contributed by each channel is typically uncorrelated with that of the other channels, so the power of the overall quantization error component is just M times the power of the quantization error contributed by one of the channels.

One obvious limitation of the $\Pi\Delta\Sigma$ADC of this example is that the filters only have length-7. Indeed, if longer filters were used, it would be possible to better attenuate the quantization error from each channel, although the overall signal component, in general, would not be simply a delayed version of the input sequence. For instance, if length-11 filters were used, an extension of the argument above indicates that the overall signal component would have the form $w[n] = 4(h[3]x[n - 3] + h[7]x[n - 7])$. In this case, the $\Pi\Delta\Sigma$ADC would act as an LTI filter with transfer function $4z^{-3}(h[3] + h[7]z^{-4})$ with respect to the input sequence. This filtering can be avoided by constraining $H(z)$ such that $h[7] = 0$ and $h[3] \neq 0$ (or vice versa) and choosing the nine remaining coefficients so as to minimize the power of the overall quantization error component. Of course, the approach is not limited to length-11 filters. Filters of any length can be used, and for each length a method of optimally choosing the unconstrained coefficients for various $\Delta\Sigma$ modulators is presented in Appendix A. The minimum overall quantization error component powers obtainable as a function of filter length for various $\Delta\Sigma$ modulators are calculated in the next section. As might be expected, increasing the filter length continues to reduce the power of the overall quantization error component, but a point of diminishing returns is reached at filter lengths beyond approximately $2PM$ where P is the $\Delta\Sigma$ modulator order and M is the number of channels. As will be quantified shortly, these optimal filters give rise to highly attenuated quantization error, but require noninteger coefficients; at lengths of $2PM$ they may be prohibitively expensive to implement with current circuit technology.

An alternate approach is to use so-called comb^{P+1} filters for which extremely hardware-efficient recursive structures are known. As will be shown, they result in quantization error attenuation that is almost as good as that obtainable with optimal filters. However, their impulse responses are not constrained in the fashion described above, so they result in an overall signal component that is an LTI filtered version of the input sequence.

In some applications, filtering of the overall signal component may not present a problem provided the filter has no zeros near the unit circle. For example, such filtering imposed by the A/D converter in a spectrum analyzer would not pose a significant problem because the output spectrum estimate could be adjusted digitally to account for the filtering.

Alternatively, an *equalization filter* following the $\Pi\Delta\Sigma$ADC could be used to compensate for the filtering. For instance, in the example above, provided none of the zeros of $h[3] + h[7]z^{-4}$ are on the unit circle, the overall signal component could be converted to a delayed version of the input sequence with arbitrary accuracy (as a function of filter complexity).

IV. THEORETICAL PERFORMANCE

A. The Overall Signal Component

As shown by example in the previous section and proven in Appendix A, the overall signal component is an LTI filtered version of the input sequence. That is, the overall signal component can be written as $w[n] = h'[n] * x[n]$, or, equivalently, $W(z) = H'(z)X(z)$. A general expression for $h'[n]$ as a function of the channel filter impulse response, $h[n]$, the $\Delta\Sigma$ modulator signal component impulse response, $s[n]$, and the delay, k_0, between the Hadamard sequences in the $\Pi\Delta\Sigma$ modulator and those in the decoder is derived in Appendix A. However, most of the discussion below is restricted to the case where the $\Delta\Sigma$ modulators only impose a delay on their signal components, the channel filters are odd-length FIR, and k_0 is a specific function of $\Delta\Sigma$ modulator delay and channel filter length. Specifically, $s[n] = \delta[n - L]$ where L is an integer, $h[n] = 0$ when $n < 0$ or $n \geq N$ where N is an odd integer, and $k_0 = \frac{N-1}{2} + L$.

With these restrictions, it follows from Theorem A1 of Appendix A, that

$$H'(z) = Mz^{-k_0} \sum_{m=-K}^{K} h\left[\frac{N-1}{2} + mM\right] z^{-mM}, \quad (2)$$

where $K = \left\lfloor \frac{N-1}{2M} \right\rfloor$. Therefore, $w[n]$ only depends on every M^{th} value of $h[n]$. In this sense, the effect of the filtering performed by $H(z)$ on each channel is at least partially negated. If $H(z)$ is further restricted such that

$$h[n] = \begin{cases} \frac{1}{M}, & \text{when } n = \frac{N-1}{2} ; \\ 0, & \text{when } n = \frac{N-1}{2} + mM , m = 0, \pm 1, \cdots \pm K \end{cases} \quad (3)$$

then it follows that $w[n] = x[n - k_0]$ so the effect of the filtering performed by $H(z)$ is completely negated. The coefficients not specified by (3) have no effect on the overall signal component, so they may be chosen to minimize the power of the overall quantization error using the results presented in Appendix B.

Alternatively, comb^{P+1} or other types of filters that are not constrained according to (3) but are perhaps simpler to implement than the optimal filters of Appendix B can be used. In such cases $H'(z)$ is not a simple delay, but so long as it does not have any zeros on the unit circle an equalization filter with a frequency response that approximates (a delayed version of)

$$F(e^{j\omega}) = \frac{1}{M \sum_{m=-K}^{K} h\left[\frac{N-1}{2} + mM\right] e^{-j\omega mM}} \quad (4)$$

can be used to compensate for the filtering performed by the $\Pi\Delta\Sigma$ADC.

B. The Equalized Overall Quantization Error Component

A meaningful measure of the $\Pi\Delta\Sigma$ADC quantization error performance is the power of the overall quantization error component after equalization, which can be written as

$$P_e = \frac{1}{2\pi} \int_{-\pi}^{\pi} S_{ee}(e^{j\omega}) \left|F(e^{j\omega})\right|^2 d\omega, \quad (5)$$

where $S_{ee}(e^{j\omega})$ is the power spectral density of the overall quantization error component.[2] When $h[n]$ satisfies (3), $|F(e^{j\omega})| = 1$ so P_e is just the power of the overall quantization error component. When $h[n]$ does not satisfy (3) the overall signal component is not just a delayed version of the input sequence. In such cases, the $\Pi\Delta\Sigma$ADC without equalization can be viewed as a perfectly equalized A/D converter with quantization error power P_e followed by $H'(z)$. Therefore, P_e is a measure of A/D converter performance that is independent of whether or how accurately the equalization filter is implemented (which depends on the application).

To evaluate (5), it is necessary to calculate $S_{ee}(e^{j\omega})$. From Fig. 3 it follows that

$$e[n] = \sum_{r=0}^{M-1} u_r[n - k_0]e_r[n], \quad (6)$$

where $e_r[n] = e_{q_r}[n]*h[n]$ is the quantization error contributed by the rth $\Delta\Sigma$ modulator as measured at the output of $H(z)$. The autocorrelation of $e[n]$ is defined as $R_{ee}[k] = \mathrm{E}(e[n]e[n+k])$. Substituting (6) into this definition and interchanging the expectation and summations results in

$$R_{ee}[k] = \sum_{r=0}^{M-1} \sum_{q=0}^{M-1} u_r[n - k_0]u_q[n - k_0 + k]\mathrm{E}(e_r[n]e_q[n+k]). \quad (7)$$

It is shown in [2] that for many of the known $\Delta\Sigma$ modulators and most practical input sequences that do not overload the $\Delta\Sigma$ modulators, $e_r[n]$ and $e_q[n+k]$ are uncorrelated when $r \neq q$, and $R_{e_r e_r}[k]$, the autocorrelation of $e_r[n]$, is independent of r. It follows that (7) reduces to

$$R_{ee}[k] = MC_M[k]R_{e_r e_r}[k], \quad (8)$$

where

$$C_M[k] = \frac{1}{M} \sum_{r=0}^{M-1} u_r[n - k_0]u_r[n - k_0 + k]. \quad$$

From the definition of the Hadamard sequences, $C_M[k]$ can be written as:

$$C_M[k] = \begin{cases} 1 & \text{if } k \text{ is a multiple of } M \\ 0 & \text{otherwise,} \end{cases} \quad (9)$$

which is a well-known sequence in the field of multirate signal processing and is called the *comb sequence*.

Taking the Fourier transform of (8) using the comb sequence modulation formula derived in [9] results in

$$S_{ee}(e^{j\omega}) = \sum_{k=0}^{M-1} S_{e_r e_r}\left(e^{j(\omega - 2\pi k/M)}\right).$$

where $S_{e_r e_r}(e^{j\omega})$ is the power spectral density of $e_r[n]$.

The most common method of analyzing $\Delta\Sigma$ modulators involves modeling the coarse A/D converters within the $\Delta\Sigma$ modulators as additive uniformly distributed white noise sources [1]. This method of analysis is widely used, and is actually an exact method in terms of calculating average quantization error power [10]. Applying the model gives $S_{e_r e_r}(e^{j\omega}) = \frac{\Delta^2}{12}|N(e^{j\omega})H(e^{j\omega})|^2$ where $N(z)$ is the effective filter imposed on the white quantization noise by the $\Delta\Sigma$ modulators, and Δ is the quantization step-size. Thus, the power spectral density of the overall quantization error component can be written as

$$S_{ee}(e^{j\omega}) = \frac{\Delta^2}{12} \sum_{k=0}^{M-1} \left| N\left(e^{j(\omega - 2\pi k/M)}\right) H\left(e^{j(\omega - 2\pi k/M)}\right) \right|^2.$$

(10)

This expression in conjunction with (5) is used to calculate P_e in the subsections below.

C. Optimal Filters

Figs. 5 and 6 show the ideal performance obtainable using the optimal channel filters derived in Appendix B. Each shows plots of P_e in dB relative to Δ^2 (i.e., $10\log(P_e/\Delta^2)$) as a function of $\Delta\Sigma$ modulator order, number of channels, and filter length. For each $\Delta\Sigma$ modulator, $N(z) = (1 - z^{-1})^P$ were P is the $\Delta\Sigma$ modulator order. In both figures, data are shown for $\Delta\Sigma$ modulators of orders $2, 3, 4, 5$, and 6.

Fig. 5 consists of five parts each of which shows plots of P_e versus filter length for a particular $\Delta\Sigma$ modulator order. For each $\Delta\Sigma$ modulator, seven curves are shown; from top to bottom the curves correspond to $M = 8, 12, 16, 20, 24, 28$, and 32, respectively. For a given M, filter length, and $\Delta\Sigma$ modulator order, P_e can be determined using Fig. 4. For example, for a sixteen channel $\Pi\Delta\Sigma$ADC with sixth-order $\Delta\Sigma$ modulators and filters of length-100, Fig. 5 indicates that P_e is less than -100 dB; as the filter length is increased, P_e asymptotically approaches a value of approximately -107 dB.

Fig. 6 shows the minimum attainable P_e as a function of M on a log scale for each $\Delta\Sigma$ modulator order. From top to bottom the curves shown correspond to second, third, fourth, fifth, and sixth-order $\Delta\Sigma$ modulators, respectively. For each P_e calculation, the filter length was sufficiently long (at least $2PM$) that an increase in length would not significantly decrease P_e. Note that in each case the curve is approximately straight and that for every doubling of the number of channels P_e decreases by approximately $6P$ dB. This implies that doubling the number of channels increases the conversion accuracy of the $\Pi\Delta\Sigma$ADC by approximately P bits.
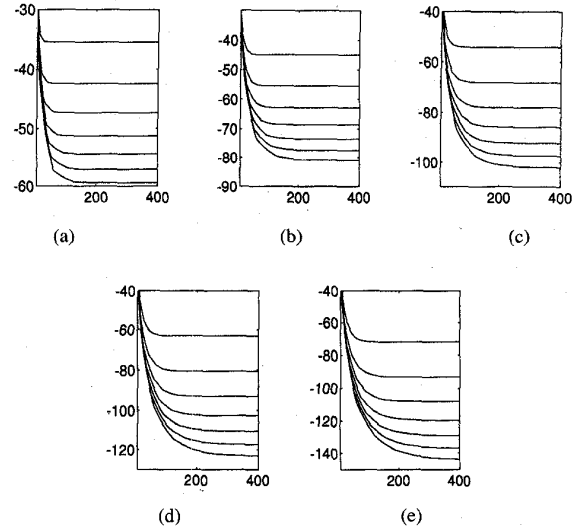

Fig. 5. P_e in dB relative to Δ^2 versus filter length, N, for optimal $H(z)$ with $M = 8, 12, 16, \cdots, 32$ for (a) second-order, (b) third-order, (c) fourth-order, (d) fifth-order, and (e) sixth-order $\Delta\Sigma$ modulators.
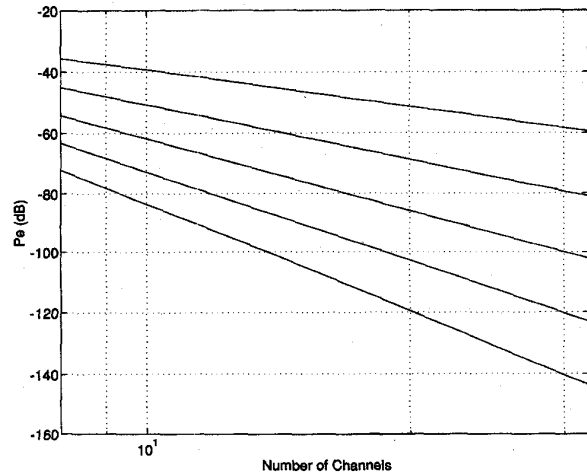

Fig. 6. P_e in dB relative to Δ^2 for optimal $H(z)$ versus number of channels on a log scale. From top to bottom, the curves correspond to $\Pi\Delta\Sigma$ADC's employing second, third, fourth, fifth, and sixth-order $\Delta\Sigma$ modulators, respectively.

D. Comb^{P+1} Filters

Figs. 7 and 8 show data that are analogous to those shown in Figs. 5 and 6, respectively, except that they correspond to channel filters with transfer function

$$H(z) = \left(\frac{1 - z^{-N_1}}{1 - z^{-1}}\right)^{P_1} \left(\frac{1 - z^{-N_2}}{1 - z^{-1}}\right)^{P_2},$$

(11)

where $P_1 + P_2 = P + 1$, and $N_2 = N_1 + 1$. Such filters have come to be known as comb^{P+1} filters. It is easy to verify that $H(z)$ is FIR with length $N = P_1(N_1 - 1) + P_2(N_2 - 1) + 1$. Thus, it is always possible to choose P_1 and P_2 for given values of P and N.

As is evident from Fig. 7, for each $\Delta\Sigma$ modulator order and number of channels, there is a particular filter length
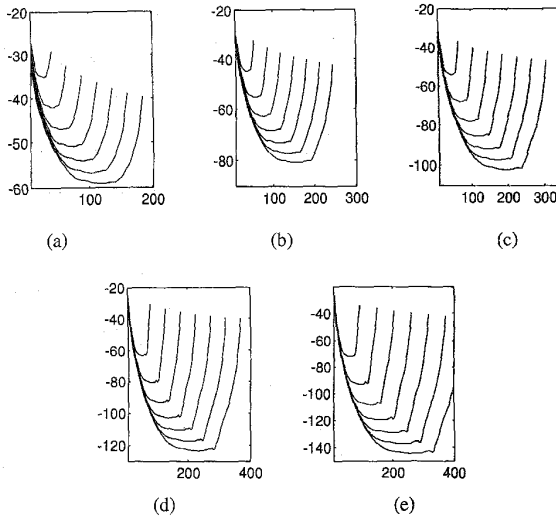
(a)   (b)   (c)

(d)   (e)

Fig. 7. P_e in dB relative to Δ^2 versus filter length, N , for comb^{P+1} $H(z)$ with $M = 8, 12, 16, \cdots, 32$ for (a) second-order, (b) third-order, (c) fourth-order, (d) fifth-order, and (e) sixth-order $\Delta\Sigma$ modulators.
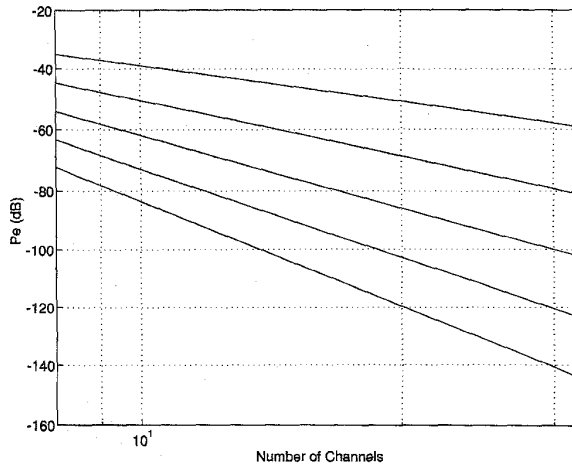

Fig. 9. Power spectral density in dB relative to Δ^2 of the equalized output of the $\Pi\Delta\Sigma$ ADC.

Number of Channels

Fig. 8. P_e in dB relative to Δ^2 for comb^{P+1} $H(z)$ versus number of channels on a log scale. From top to bottom, the curves correspond to $\Pi\Delta\Sigma$ ADC's employing second, third, fourth, fifth, and sixth-order $\Delta\Sigma$ modulators, respectively.

for which P_e is minimized. Interestingly, in each case the minimum P_e value is very close to that which occurs for the optimal filters. However, in contrast to the case of the optimal filters, as the filter length is increased, P_e eventually begins to increase. Fig. 8 shows the minimum attainable P_e as a function of M on a log scale for each $\Delta\Sigma$ modulator order. The figure indicates that, as in the case of the optimal filters, doubling the number of channels increases the conversion accuracy of the $\Pi\Delta\Sigma$ ADC by approximately P bits.

E. A Design Example

As an example, consider a 16-channel $\Pi\Delta\Sigma$ ADC with sixth-order $\Delta\Sigma$ modulators and comb^7 channel filters. Suppose that each $\Delta\Sigma$ modulator consists of three cascaded second-
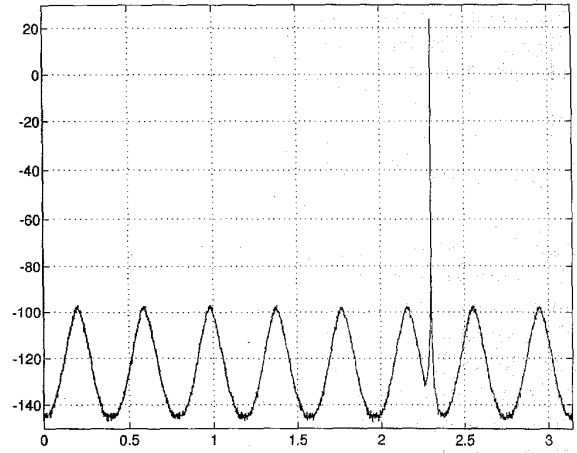
order $\Delta\Sigma$ modulator stages each with three-level quantizers [11]. Ideally, the $\Delta\Sigma$ modulators are such that $S(z) = z^{-3}$ and $N(z) = (1 - z^{-1})^6$. Suppose the channel filters are of the comb^{P+1} type with transfer function (11) where $N_1 = 19$, $N_2 = 20$, $P_1 = 3$, and $P_2 = 4$, so that $N = 131$. As indicated by the data shown in Fig. 7, these parameters result in $P_e \approx -107$ dB relative to Δ^2 . Given that the $\Delta\Sigma$ modulators have a usable input range of approximately $(-0.4\Delta, 0.4\Delta)$, this is equivalent to approximately 16 b of A/D conversion precision.

Fig. 9 shows the estimated power spectral density of the equalized output of the $\Pi\Delta\Sigma$ ADC as obtained by computer simulation. The input to the simulated $\Pi\Delta\Sigma$ ADC was a sinusoid of amplitude 0.30Δ and frequency $\frac{375}{512}\pi$ radians. The spectral estimation was performed by averaging 16 periodograms corresponding to $\frac{3}{4}$ -length-overlapping Hanning windowed length-16384 segments of the simulated $\Pi\Delta\Sigma$ ADC output, and then scaling the result by $|F(e^{j\omega})|^2$ to achieve equalization.

Fig. 10(a) shows the simulation data of Fig. 9 with the overall signal component removed, namely $S_{ee}(e^{j\omega})|F(e^{j\omega})|^2$, and Fig. 10(b) shows the corresponding data as predicted by theory (calculated using (4) and (10)). It is evident that for the case shown, the simulation data closely supports the theory. Numerous other simulation experiments performed by the authors are similarly supportive of the theory.

In a conventional $\Delta\Sigma$ modulator A/D converter, the circuit area required for the decimation filter is typically more than an order of magnitude larger that required for the $\Delta\Sigma$ modulator. Similarly, in a $\Pi\Delta\Sigma$ ADC, it is likely that most of the circuit area will be occupied by the decoder and, if implemented, the equalization filter. Therefore, it is of interest to gauge the hardware complexity of these components. A rough indication of complexity can be obtained by estimating the number of multiplies and additions performed per sample interval, and the number of delay elements required.

For the current example, the decoder must implement 16 comb^7 filters, and fifteen adders to sum the channels. From
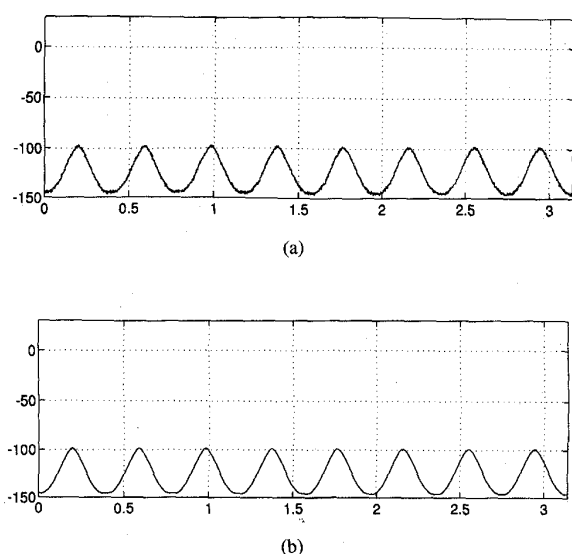
Fig. 10. (a) Power spectral density in dB relative to Δ^2 of the overall quantization error component corresponding to the simulation data of Fig. 9. (b) The corresponding theoretical power spectral density.

Fig. 11. (a) Magnitude response of equalization filter in dB. (b) Overall response of the $\Pi\Delta\Sigma$ADC with respect to the input signal in dB. (c) Selected range of data from Fig. 11(b) in a linear plot showing the equiripple property of the overall response of the $\Pi\Delta\Sigma$ADC.

the results presented in [12], it follows that each of the comb[7] filters requires 14 adders, no multipliers, and 144 delay elements. Therefore, a direct implementation of the decoder performs $14 \cdot 16 + 15 = 239$ additions and no multiplications per sample interval, and requires $144 \cdot 16 = 2304$ delay elements. Additional logic is required to implement the digital Hadamard modulation, but the Hadamard sequences are all-ones sequences so no real multiplications are required; the additional hardware required to generate the Hadamard sequences is on the order of 100 logic gates.

An efficient equalization filter can be implemented using the Parks-McClellan algorithm [13]. By setting the desired magnitude response to be $|F(e^{j\omega})|$, choosing the weighting function to be $|H'(e^{j\omega})|$, and optimizing over $(-\pi, \pi)$, the resulting equalization filter is such that the response of the $\Pi\Delta\Sigma$ADC with respect to the overall signal component is equiripple with linear phase.

Fig. 11(a) shows the magnitude response in dB of an equalization filter designed for the current example, and Fig. 11(b) shows the corresponding response of the $\Pi\Delta\Sigma$ADC with respect to the overall signal component. As indicated by Fig. 11(c), the maximum magnitude ripple imposed by the equalized $\Pi\Delta\Sigma$ADC on the input signal is only about $4.1 \cdot 10^{-4}$, corresponding to $3.6 \cdot 10^{-3}$ dB. Although this particular equalization filter has length-656, only 41 samples of its impulse response are nonzero (a consequence of the $2\pi/16$ periodicity of $|F(e^{j\omega})|$). Moreover, the filter coefficients are symmetric. Therefore an implementation of the filter would require 40 additions and 20 multiplications per sample interval and 655 delay elements.

In summary, an example $\Pi\Delta\Sigma$ADC has been considered and shown to achieve approximately 16 b of A/D conversion precision. Decoder and Equalization filter implementations have been considered that, together, require the equivalent
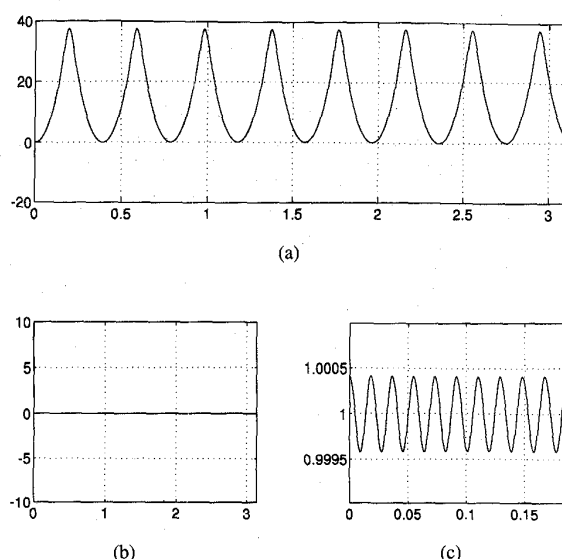
of 279 adders, 20 multipliers, and 2959 delay elements all clocked at the A/D conversion rate. While this is not a trivial amount of digital processing, it is within the limits imposed by current digital VLSI technology. Moreover, in estimating the decoder complexity, no use was made of the symmetry inherent in the decoder structure, so it may be possible to design a more hardware-efficient decoder. In particular, multirate block filtering techniques [9] should allow a significant reduction in the number of delay elements required.

V. SENSITIVITY TO NONIDEAL CIRCUIT BEHAVIOR

In practice, nonideal circuit behavior reduces the conversion accuracy of the $\Pi\Delta\Sigma$ADC below that predicted by the analysis above. Common types of nonideal circuit behavior arise from electronic noise, errors in the nominal values of components such as capacitors and resistors, finite op-amp gain and bandwidth, nonzero op-amp settling time, comparator hysteresis, and clock timing jitter. In $\Delta\Sigma$ modulators, these nonidealities manifest themselves as analog gain mismatches, a high electronic noise floor, integrator leak, integrator nonlinearity, nonuniform quantization levels in the coarse A/D converters, and nonuniform reference levels in the D/A converters. In the $\Pi\Delta\Sigma$ modulator, the nonidealities additionally manifest themselves as channel gain and offset mismatches and Hadamard modulation level errors.

The presence of nonideal circuit behavior causes the output of the $\Pi\Delta\Sigma$ADC to contain an *overall circuit error component* in addition to the overall signal and and overall quantization error components discussed above; the output is the sum of the three components. It is convenient to distinguish between two types of errors that make up the overall circuit error component: those that are common to conventional $\Delta\Sigma$ modulator A/D converters, and those that are unique to the

$\Pi\Delta\Sigma$ADC. This allows existing results concerning nonideal circuit behavior in conventional $\Delta\Sigma$ modulator A/D converters to be applied directly to the $\Pi\Delta\Sigma$ADC. Specifically, the overall circuit error component can be considered the sum of two subcomponents: the *conversion error subcomponent*, and the *reconstruction error subcomponent*. The conversion error subcomponent is the result of all types of nonideal $\Delta\Sigma$ modulator performance arising from nonideal circuit behavior except for $\Delta\Sigma$ modulator signal component gain and offset errors. The reconstruction error subcomponent is the aggregate of all A/D conversion errors arising from nonideal circuit behavior that are not part of the conversion error subcomponent.

The conversion error subcomponent is analogous to the error caused by nonideal circuit behavior in conventional $\Delta\Sigma$ modulator A/D converters. Although down-sampling is not performed, each $\Pi\Delta\Sigma$ADC channel contains the equivalent of a conventional $\Delta\Sigma$ modulator A/D converter because each $\Delta\Sigma$ modulator is followed by a lowpass filter. Hence, on each channel the component of the sequence just prior to Hadamard modulation in the decoder arising from nonideal $\Delta\Sigma$ modulator behavior has the same characteristics as the corresponding component of the output of a conventional $\Delta\Sigma$ modulator A/D converter (aside from down-sampling). In general, the M such error components are correlated. However, like the quantization error components from the $\Delta\Sigma$ modulators, the error components caused by nonideal $\Delta\Sigma$ modulator behavior are generated after the analog Hadamard modulators in the $\Pi\Delta\Sigma$ modulator. Consequently, they are decorrelated by the digital Hadamard modulators in the decoder, so they add in power, not amplitude; the power of the conversion error subcomponent is simply the sum of the powers of the lowpass filtered errors from the M nonideal $\Delta\Sigma$ modulators. For each $H(z)$ considered in this paper,

$$\frac{M}{2\pi}\int_{-\pi}^{\pi}\left|H(e^{j\omega})\right|^2 d\omega < \frac{M}{2\pi}\int_{-\pi}^{\pi}\left|H(e^{j\omega})F(e^{j\omega})\right|^2 d\omega < 1,$$

so the conversion error subcomponent typically is less than M times as powerful as the corresponding error at the output of a conventional $\Delta\Sigma$ modulator A/D converter.

Unlike the conversion error subcomponent, the reconstruction error subcomponent does not have a direct analogy in conventional $\Delta\Sigma$ modulator A/D converters. It results from nonideal analog Hadamard modulator behavior and from mismatches among the signal component gains and offsets of the $\Delta\Sigma$ modulators. Ideally, the signal component of the rth $\Delta\Sigma$ modulator in the $\Pi\Delta\Sigma$ modulator is $w_r[n] = x[n - L]u_r[n - L]$. However, nonideal Hadamard modulation levels and nonideal gains and offsets in the analog circuitry on either side of the Hadamard modulator give rise to a nonideal signal component of the form

$$\begin{aligned}\widehat{w}_r[n] =&\, w_r[n] + a_r x[n - L]u_r[n - L]\\ &+ b_r x[n - L] + c_r u_r[n - L] + d_r\end{aligned}$$

where a_r, b_r, c_r, and d_r are not all zero and may vary in time. For example, a_r is nonzero when the gain of the signal component of the rth $\Delta\Sigma$ modulator deviates from
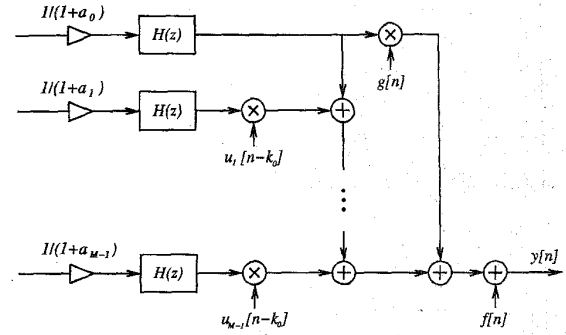

Fig. 12. A modified decoder structure that digitally compensates for channel gain, offset, and Hadamard sequence level mismatches.

unity. This type of deviation can be caused directly by gain errors in the analog circuitry, and indirectly by errors in the Hadamard modulation levels. Similarly, b_r is nonzero when the Hadamard modulation levels are not symmetric about zero; c_r is nonzero when the analog circuitry prior to the Hadamard modulator introduces a nonzero offset, and d_r is nonzero when the analog circuitry following the Hadamard modulator introduces a nonzero offset.

Through a straightforward modification of Theorem A1, the reconstruction error subcomponent can be written explicitly as

$$r[n] =$$
$$\sum_{k=0}^{\infty} h[k]x[n - k - L]\sum_{r=0}^{M-1} u_r[n - k_0]\left[a_r u_r[n - k - L] + b_r\right]$$
$$+ \sum_{k=0}^{\infty} h[k]\sum_{r=0}^{M-1} u_r[n - k_0]\left[c_r u_r[n - k - L] + d_r\right]. \quad (12)$$

It can be verified from (12) that random deviations of a_r, b_r, c_r, and d_r from zero translate to A/D conversion errors with the same order of magnitude. Therefore, matching the gains and offsets introduced by each channel could be a limiting practical problem with the $\Pi\Delta\Sigma$ADC approach.

In cases where a_r, b_r, c_r, and d_r are nonzero but do not vary rapidly with respect to the input signal, digital techniques can be used to significantly mitigate the problem. To the extent that a_r, b_r, c_r, and d_r are known, the errors to which they give rise can be compensated by modifying the decoder as shown in Fig. 12. Since it is always possible to choose one of the Hadamard sequences to be all ones, in the decoder of Fig. 12, $u_0[n]$ is assumed to be the all-ones sequence. To compensate for the effects of a_r, the rth channel of the decoder is multiplied by $1/(1 + a_r)$. To remove the errors associated with c_r and d_r, the M–length periodic sequence

$$f[n] = -\sum_{k=0}^{\infty} h[k]\sum_{r=0}^{M-1} u_r[n - k_0]\left[c_r u_r[n - k - L] + d_r\right]$$

is simply added to the $\Pi\Delta\Sigma$ADC output. Similarly, to remove the error associated with b_r, the output of the first channel is

multiplied by the M–length periodic sequence

$$g[n] = - \sum_{r=0}^{M-1} b_r u_r[n - k_0]$$

and added to the $\Pi\Delta\Sigma\text{ADC}$ output.

Aside from the problem of added complexity, the main draw-back of this *digital trimming* approach is that the actual values of a_r, b_r, c_r, and d_r must be determined for each channel. This requires either an extra manufacturing step or the implementation of an auto-calibration mode in the $\Pi\Delta\Sigma\text{ADC}$. Alternatively, it may be possible to determine the values dynamically because the form of the error they introduce is known explicitly, but establishing the details of such an algorithm is currently an open problem.

Fig. 13(a)–(d) shows simulation data that illustrate the effect of the reconstruction error subcomponent and its digital compensation for the case of the 16-channel $\Pi\Delta\Sigma\text{ADC}$ example considered in the previous section. Fig. 13(a)–(c) each show the power spectral density of the equalized $\Pi\Delta\Sigma\text{ADC}$ output corresponding to the simulation conditions of Fig. 9 except with channel gain errors, channel offset errors, and analog Hadamard level errors. Specifically, these errors were chosen randomly within $\pm0.01\%$ for Fig. 13(a), $\pm0.1\%$ for Fig. 13(b), and $\pm1.0\%$ for Fig. 13(c). The harmonics and intermodulation components predicted by (12) are clearly visible and increase as a function of the error magnitude as expected. The powers of the A/D conversion errors in the three cases, obtained by integrating the data in the three figures, are -85, -65, and -45 dB respectively. The spurious-free dynamic ranges are 87, 67, and 47 dB, respectively.

Fig. 13(d) corresponds to the simulation conditions of Fig. 13(c) except that digital trimming was used in the decoder per Fig. 12. To simulate measurement error, the values used for a_r, b_r, c_r, and d_r were chosen with random errors within $\pm0.1\%$. The power of the A/D conversion error in this case is -104 dB and the spurious-free dynamic range is 118 dB. As is evident from the figure, the digital trimming scheme is effective even with imperfect values for a_r, b_r, c_r, and d_r.

Numerous additional simulations along the lines of those leading to Fig. 13(a)-(d) has been performed by the authors with similar results. For example, performing the simulations with different random number seeds (i.e., with different specific error values), and with different input sequences (e.g., different sinusoid frequencies, multiple sinusoids, etc.) did not change the nature of the results.

An additional comment is in order regarding the use of $\Delta\Sigma$ modulators in a nonoversampling system. Oversampling in conventional $\Delta\Sigma$ modulator A/D converters allows for relaxed anti-aliasing filter specifications. Of course, if the $\Pi\Delta\Sigma\text{ADC}$ is operated without any oversampling, its anti-aliasing filter specifications can not be relaxed. Indeed, the anti-aliasing filter issues are the same for the $\Pi\Delta\Sigma\text{ADC}$ as they are for any other nonoversampling A/D converter. Hence, the $\Pi\Delta\Sigma\text{ADC}$ does not share one of the major advantages of conventional $\Delta\Sigma$ modulator A/D converters. However, this does not imply that the $\Delta\Sigma$ modulators in the $\Pi\Delta\Sigma\text{ADC}$ must have the full-rate bandwidth. Because each $\Delta\Sigma$ modulator is followed by a
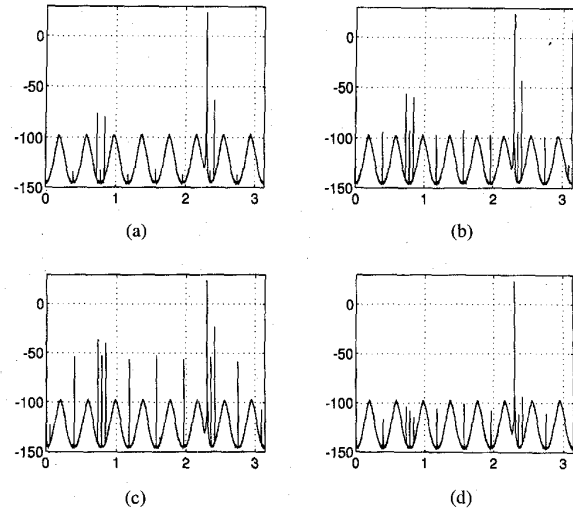

Fig. 13. Power spectral densities of equalized $\Pi\Delta\Sigma\text{ADC}$ outputs with channel gain, channel offset, and analog Hadamard level errors: (a)-(c) correspond to $\Pi\Delta\Sigma\text{ADC}$'s with randomly chosen errors of $\pm0.01\%$, $\pm0.1\%$, and $\pm1.0\%$, respectively, and (d) corresponds to the $\Pi\Delta\Sigma\text{ADC}$ of (c) except that digital trimming was used with nonideal values of a_r, b_r, c_r, and d_r. The A/D conversion error powers are -85, -65, -45, and -104 dB, respectively, and the spurious-free dynamic ranges are 87, 67, 47, and 118 dB, respectively.

lowpass filter, $H(z)$, with a bandwidth that is approximately an Mth of the desired A/D converter bandwidth, it follows that the bandwidth of the $\Delta\Sigma$ modulators can be considerably less than the full-rate bandwidth just as in the case of conventional $\Delta\Sigma$ modulator A/D converters.

VI. CONCLUSION

A new architecture for A/D conversion has been introduced and analyzed. The system is so far unique in that it performs $\Delta\Sigma$ modulator-based A/D conversion without time oversampling or time interlacing. Through the use of Hadamard modulation on multiple channels the system achieves the effect of oversampling without the need for clock rates that are higher than the A/D conversion rate. The analysis presented is general in that it does not place significant restrictions on the types of $\Delta\Sigma$ modulators that can be used. The effects of nonideal circuit behavior were considered and it was shown that, after digital trimming, the architecture is not significantly more sensitive to nonideal circuit behavior than are its constituent $\Delta\Sigma$ modulators. A sixteen channel system with sixth-order $\Delta\Sigma$ modulators was considered in detail as an example and shown to have a theoretical precision of approximately 16 b.

The ideas presented in this paper may allow the application of $\Delta\Sigma$ modulator technology to higher-bandwidth applications than are currently feasible. Whether the approach can compete favorably with other full-rate approaches such as pipelined A/D converters is yet to be seen. Additional experimental work is necessary to establish the limitations of the approach with respect to VLSI implementation.

APPENDIX A

The following theorem asserts that, provided the $\Delta\Sigma$ modulators fit the paradigm of Fig. 2, the $\Pi\Delta\Sigma\text{ADC}$ is equivalent

to an LTI filter $H'(z)$ plus an additive quantization error source, $e[n]$, where $e[n]$ is a linear combination of the quantization error components from each of the $\Delta\Sigma$ modulators. Therefore, the theorem identifies the overall signal and overall quantization error components in the output of the $\Pi\Delta\Sigma$ADC.

Theorem A1: If the $\Delta\Sigma$ modulators in the $\Pi\Delta\Sigma$ modulator can be modeled as shown in Fig. 2, then the output of the $\Pi\Delta\Sigma$ modulator has the form $y[n] = w[n] + e[n]$ where $e[n]$ is a linear combination of the additive quantization error components introduced by the $\Delta\Sigma$ modulators, and $w[n] = x[n] * h'[n]$ where

$$h'[n] = MC_M[n - k_0][s[n] * h[n]],$$

$h[n]$ is the impulse response of $H(z)$, and $C_M[n]$ is the comb sequence defined in (9).

Proof: The decoder is a linear system, so $e[n]$ must be a linear combination of the additive quantization error components introduced by the $\Delta\Sigma$ modulators. Because $w[n]$ is, by definition, not a function of the quantization error components from the $\Delta\Sigma$ modulators, superposition can be used to determine the expression for $w[n]$. Specifically, $w[n]$ would be the output of the $\Pi\Delta\Sigma$ADC if the quantization error source, $e_q[n]$, in each $\Delta\Sigma$ modulator were set to zero.

Consider the rth channel of the $\Pi\Delta\Sigma$ADC with the quantization error source set to zero. Let $q[n] = s[n] * h[n]$. The output of each channel can be written as

$$t_r[n] = \sum_{k=0}^{\infty} q[k]x[n - k]u_r[n - k]u_r[n - k_0].$$

The overall signal component is just the sum of the M $t_r[n]$ sequences:

$$w[n] = \sum_{r=0}^{M-1} t_r[n]$$

$$= \sum_{k=0}^{\infty} q[k]x[n - k] \sum_{r=0}^{M-1} u_r[n - k]u_r[n - k_0]. \quad (13)$$

By definition, $u_r[n]$ is the rth row of an $M \times M$ Hadamard matrix repeated periodically. It follows that

$$\sum_{r=0}^{M-1} u_r[n-k]u_r[n-k_0] = \begin{cases} M, & \text{if } k - k_0 \text{ is a multiple of } M \\ 0, & \text{otherwise.} \end{cases}$$

Hence,

$$\sum_{r=0}^{M-1} u_r[n - k]u_r[n - k_0] = MC_M[k - k_0],$$

so (13) becomes

$$w[n] = M\sum_{k=0}^{\infty} q[k]x[n - k]C_M[k - k_0],$$

from which the result follows.

APPENDIX B

In Section IV it is shown that the overall signal component is just a delayed version of the input sequence provided the $\Delta\Sigma$ modulators have $S(z) = z^{-L}$ and (3) is satisfied. Since (3) only constrains every M^{th} value of $h[n]$, the remaining values may be chosen so as to minimize P_e. A method for choosing these unconstrained coefficients optimally is developed in this appendix.

Combining (5) and (10) with $F(z) = 1$ results in

$$P_e = \frac{1}{2\pi}\int_{-\pi}^{\pi} \frac{\Delta^2}{12} \sum_{k=0}^{M-1} \left| N\left(e^{j(\omega - 2\pi k/M)}\right)H\left(e^{j(\omega - 2\pi k/M)}\right)\right|^2 d\omega.$$

Since discrete-time Fourier transforms are periodic-2π, this can be written as

$$P_e = \frac{M\Delta^2}{24\pi}\int_{-\pi}^{\pi} \left|N(e^{j\omega})H(e^{j\omega})\right|^2 d\omega. \quad (14)$$

By Parseval's Theorem, this is equivalent to

$$P_e = \frac{M\Delta^2}{12} \sum_{m=-\infty}^{\infty} \left[h[m] * n[m]\right]^2,$$

where $n[m]$ is the impulse response of $N(z)$. With some algebra, this becomes

$$P_e = M \sum_{j=-\infty}^{\infty} h(j) \sum_{k=-\infty}^{\infty} h[k]R_{j,k},$$

where

$$R_{j,k} = \frac{\Delta^2}{12} \sum_{m=-\infty}^{\infty} n[m - j]n[m - k].$$

If $H(z)$ is an odd length–N FIR filter, a more compact notation is $P_e = M\mathbf{h}^T\mathbf{R}\mathbf{h}$, where

$$\mathbf{h} = \begin{bmatrix} h[0] \\ \vdots \\ h[N - 1] \end{bmatrix},$$

and

$$\mathbf{R} = \begin{bmatrix} R_{0,0} & \cdots & R_{0,N-1} \\ \vdots & \ddots & \vdots \\ R_{N-1,0} & \cdots & R_{N-1,N-1} \end{bmatrix}.$$

From (3) the center element of $\mathbf{h}$ is constrained to be $\frac{1}{M}$, and each element with an index equal to the index of the center element plus a multiple of M is constrained to be zero. Each of these constrained indexes will be referred to as a *constraint index*.

The following theorem provides a formula for a vector consisting of the unconstrained values of $h[n]$—that is, the vector formed by deleting the elements of $\mathbf{h}$ with constraint indexes. This vector and (3) completely define the impulse response of the optimal $H(z)$.

Theorem B1: Let $\widehat{\mathbf{R}}$ be the submatrix formed by deleting the columns and rows of $\mathbf{R}$ with constraint indexes, let $\widehat{\mathbf{b}}$ be the vector formed from the center column of $\mathbf{R}$ by deleting the elements with constraint indexes, and let $\widehat{\mathbf{h}}_{\mathrm{opt}}$ be the vector formed from the optimal $\mathbf{h}$ by deleting the elements with constraint indexes. Then, provided $N(e^{j\omega})$ is nonzero on some interval, $\widehat{\mathbf{R}}$ is nonsingular and

$$\widehat{\mathbf{h}}_{\mathrm{opt}} = -\frac{1}{M}\widehat{\mathbf{R}}^{-1}\widehat{\mathbf{b}}.$$

Proof: The first problem is to prove that $\widehat{\mathbf{R}}$ is nonsingular. Since $H(e^{j\omega})$ is rational, it can only have a finite number of zeros in the interval $[-\pi, \pi]$. By hypothesis, $N(e^{j\omega})$ is nonzero on some interval in $[-\pi, \pi]$ ($N(e^{j\omega})$ is periodic with period 2π), so from (14) it follows that $P_e > 0$. Since $P_e = M\mathbf{h}^T\mathbf{R}\mathbf{h}$ for any $\mathbf{h}$, $\mathbf{R}$ must be positive definite which implies that all its eigenvalues are positive.

By definition, $\mathbf{R}$ is Hermitian. From Theorem 4.3.15 of [14] the eigenvalues of a submatrix of a Hermitian matrix with positive eigenvalues are also positive. Therefore, the eigenvalues of $\widehat{\mathbf{R}}$ are positive. Since any submatrix of a Hermitian matrix is also Hermitian, it follows that $\widehat{\mathbf{R}}$ is nonsingular.

The next problem is to prove that $\widehat{\mathbf{h}}_{\mathrm{opt}} = -\frac{1}{M}\widehat{\mathbf{R}}^{-1}\widehat{\mathbf{b}}$. Let $\mathbf{h}$ correspond to any length-N FIR filter constrained by (3), and let $\phi = \mathbf{h}^T\mathbf{R}\mathbf{h}$. Let

$$\mathbf{y} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ \frac{1}{M} \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

and let $\mathbf{x} = \mathbf{h} - \mathbf{y}$. Then,

$$\phi = (\mathbf{x} + \mathbf{y})^T\mathbf{R}(\mathbf{x} + \mathbf{y}).$$

Since $\mathbf{R}$ is Hermitian and Toeplitz, this reduces to

$$\phi = \mathbf{x}^T\mathbf{R}\mathbf{x} + \frac{2}{M}\mathbf{b}^T\mathbf{x} + \frac{1}{M^2}R_{0,0},$$

where $\mathbf{b}$ is equal to the center column (or row) of $\mathbf{R}$. The elements of $\mathbf{x}$ whose indexes are not constraint indexes are equal to those of $\mathbf{h}$ and the elements of $\mathbf{x}$ with constraint indexes are zero, so

$$\phi = \widehat{\mathbf{h}}^T\widehat{\mathbf{R}}\widehat{\mathbf{h}} + \frac{2}{M}\widehat{\mathbf{b}}^T\widehat{\mathbf{h}} + \frac{1}{M^2}R_{0,0}, \tag{15}$$

where $\widehat{\mathbf{h}}$ is the vector formed from $\mathbf{h}$ by deleting the elements with constraint indexes.

Because ϕ is a quadratic function of $\widehat{\mathbf{h}}$, the value of $\widehat{\mathbf{h}}$ that minimizes ϕ, namely $\widehat{\mathbf{h}}_{\mathrm{opt}}$, must satisfy $\nabla\phi = 0$ where $\nabla\phi$ is the multivariable derivative of ϕ. From (15),

$$\nabla\phi = 2\widehat{\mathbf{R}}\widehat{\mathbf{h}} + \frac{2}{M}\widehat{\mathbf{b}}.$$

Therefore, $\widehat{\mathbf{h}}_{\mathrm{opt}} = -\frac{1}{M}\widehat{\mathbf{R}}^{-1}\widehat{\mathbf{b}}$.

Provided the $\Delta\Sigma$ modulators have $S(z) = z^{-L}$ and generate quantization error whose power spectral density is that of white noise driving an LTI filter, $N(z)$, then Theorem B1 provides a closed form solution for the impulse response of the odd length-N FIR filter $H(z)$ that minimizes P_e under the constraint that the overall signal component is just a delayed version of the input.

Although a large class of $\Delta\Sigma$ modulators, including most of the multistage $\Delta\Sigma$ modulators, have these properties [1], [15], [10], there exist many useful $\Delta\Sigma$ modulators for which $S(z)$ is not just a delay. For example, in most of the single-loop higher-order $\Delta\Sigma$ modulators, $S(z)$ corresponds to a lowpass IIR filter [16]. Although the power spectral density of the quantization error from these $\Delta\Sigma$ modulators is often modeled as that of white noise driving an LTI filter, $N(z)$, there is not yet a rigorous theoretical basis for doing so. Nevertheless, if the quantization error is at least quasistationary or can be well approximated by a quasistationary sequence, and its power spectral density is known then the problem of choosing an optimal $H(z)$ is well posed and in principal can be solved. However, there is no obvious general formula for choosing the optimal constrained $H(z)$; it appears that for $\Delta\Sigma$ modulators outside the class of $\Delta\Sigma$ modulators considered above, the optimization must be performed on a case by case basis.

REFERENCES

[1] J. C. Candy and G. C. Temes, "Oversampling methods for A/D and D/A conversion," in *Oversampling Delta-Sigma Data Converters Theory, Design and Simulation.* New York: IEEE Press, 1992, pp. 1–25.
[2] I. Galton, "An analysis of quantization noise in $\Delta\Sigma$ modulation and its application to parallel $\Delta\Sigma$ modulation," Ph.D. dissertation, California Instit. Technol., 1992.
[3] E. King, R. Aram, T. Fiez, and I. Galton, "Parallel delta-sigma A/D conversion," *Proc. IEEE CICC*, May 1994.
[4] J. H. van Lint and R. M. Wilson, *A Course in Combinatorics.* Cambridge: Cambridge Univ. Press, 1992.
[5] F. H. Harmuth, *Sequency Theory.* New York: Academic, 1977.
[6] L. C. Fernandez and K. R. Rao, "Design of a synchronous walsh-function generator," *IEEE Trans. Electromag. Compat.*, vol. EMC-19, pp. 407–409, Nov. 1977.
[7] F. Kitai and C. K. Yuen, "Walsh function generators," *Applications of Walsh Functions and Sequency Theory.* New York: IEEE Press, 1974, pp. 297–315.
[8] P. W. Besslich, "Walsh function generators for minimum orthogonality error," *Trans. Electromag. Compat.*, vol. EMC-15, pp. 177-179, Nov. 1973.
[9] P. P. Vaidyanathan, *Multirate Systems and Filter Banks..* Englewood Cliffs, NJ: Prentice-Hall, 1992.
[10] I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inform. Theory*, vol. 40, pp. 848–859, May 1994.
[11] I. Dedic, "A sixth-order triple-loop sigma-delta CMOS ADC with 90dB SNR and 100kHz bandwidth," *IEEE ISSCC Dig. Tech. Papers*, vol. 37, pp. 188–189, 1994.
[12] S. Chu and C. S. Burrus, "Multirate filter designs using comb filters," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 913–924, Nov. 1984.
[13] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, Englewood Cliffs, NJ: Prentice-Hall, 1989.
[14] R. A. Horn and C. R. Johnson, *Matrix Analysis.* Cambridge: Cambridge Univ. Press, 1985.

[15] I. Galton, "Granular quantization noise in the first-order delta-sigma modulator," *IEEE Trans. Inform. Theory*, vol. 39, pp. 1944–1956, Nov. 1993.

[16] K. C. H. Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 309-318, Mar. 1990.

Ian Galton (M'92) for a photograph and biography, see p. 630 of the October 1995 issue of this TRANSACTIONS.
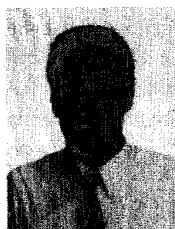
Henrik T. Jensen (S'94) was born in Odense, Denmark in 1968. He received the B.S. degree in computer engineering from Odense University, Odense, Denmark, in 1992. He received the M.S. degree, through a Fulbright scholarship, in electrical engineering from the University of California, Irvine, in 1994, where since April 1994 he has been pursuing the Ph.D. degree in electrical engineering.