Analog-Input Digital Phase-Locked Loops for Precise Frequency and Phase Demodulation

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Abstract—**Most conventional analog-input digital phase-locked loops (ADPLL's) suffer from the effects of in-loop quantization and from nonlinear behavior caused by the approximations inherent in practical digitally controlled oscillators (DCO's). The resulting errors limit the accuracy of ADPLL-based frequency demodulation and usually make ADPLL-based phase demodulation impractical because of severe phase-drift problems. This paper presents a new class of ADPLL's that are insensitive to the deleterious effects of quantization, and do not exhibit nonlinear behavior when implemented with practical DCO's. The ADPLL's are well suited to applications requiring precise frequency demodulation, and can also be used for phase demodulation because their quantization error is well behaved even after discrete-time integration. The paper establishes an analogy between the ADPLL's and delta–sigma modulators, and applies existing delta–sigma modulator results to predict the frequency and phase demodulation accuracy of the ADPLL's. A mechanization of the general architecture consisting of easily implemented components such as analog integrators, digital flip–flops, and digital counters is then presented and analyzed.**

I. Introduction

ANALOG-INPUT digital phase-locked loop (ADPLL) circuits are often used to generate digital estimates of the instantaneous frequency of angle-modulated analog input signals [1], [2]. In such cases the ADPLL simultaneously performs the operations of an all-analog phase-locked loop and an analog-to-digital (A/D) converter.

Most of the known ADPLL mechanizations approximate the ideal ADPLL shown in Fig. 1 [1]. The system consists of a *sampled phase detector*, a discrete-time *loop filter*, and a *digitally controlled oscillator (DCO)*. The input signal, $x_r(t)$, is assumed to be an angle-modulated sinusoid possibly corrupted by noise. The sampled phase detector generates a sequence proportional to the instantaneous phase difference between its two input signals at times $t_n, n = 0, 1, 2, \ldots$. The loop filter attenuates high-frequency noise components, and the DCO generates a feedback signal whose phase at time t_{n+1} varies as a linear function of the DCO input at time t_n.

Ideally, the output of the loop filter $y[n]$ corresponds to the instantaneous frequency of the input signal $x_r(t)$ and can be accumulated modulo-2π to obtain the instantaneous phase of $x_r(t)$. Thus, in principle, ADPLL's can be used as either frequency demodulators or phase demodulators. However, errors introduced by most practical ADPLL implementations place an upper limit on the accuracy of ADPLL-based frequency demodulators. Moreover, ADPLL-based phase demodulators are rarely used because the instantaneous frequency errors accumulate and cause the estimated instantaneous phase to drift rapidly from the actual instantaneous phase.

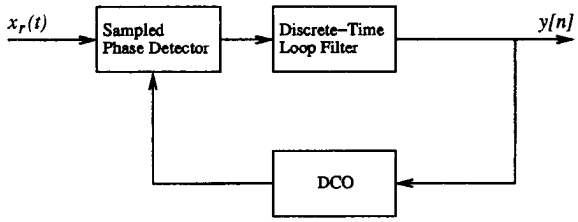

Fig. 1. The ideal ADPLL.

The errors introduced by practical ADPLL mechanizations usually stem from two approximations. The first approximation is that the phase detector is followed by or combined with a very coarse A/D converter (rarely more than a few bits) to simplify implementation of the DCO. The resulting quantization error often limits ADPLL performance [3]. The second approximation is associated with the DCO implementation. Although it is difficult to build an ideal DCO, it is relatively simple to build a digital device whose output period varies as a linear function of its input [1]. For example, such a *period linear* device can be easily built using a digital counter or shift register. Hence, the ideal DCO usually is approximated by a period linear DCO. This results in nonlinear loop equations and gives rise to errors such as asymmetric signal acquisition and tracking behavior [2], [4].

This paper presents a class of practical ADPLL's that avoid the above-mentioned problems and, therefore, can be used for highly accurate frequency and phase demodulation. Although the ADPLL's use very coarse A/D conversion, they employ quantization noise shaping so that most of the quantization error power lies outside the signal baseband and can be removed by subsequent lowpass filtering. As will be shown, the ADPLL's operate on the frequency modulation of their input signals in an analogous fashion to the way that delta–sigma ($\Delta\Sigma$) modulator data converters operate on the amplitude of their input signals [5]. Hence, they are referred to as $\Delta\Sigma$PLL's. One of the benefits of the approach is that instantaneous phase estimation using modulo-2π accumulation is practical because the quantization error is well behaved even after it is accumulated (i.e., it remains

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bounded and noise shaped). Moreover, the ADPLL's can be mechanized using simple period linear DCO's without introducing nonlinearities into the loop equations, so the attractive properties of ΔΣPLL's can be preserved in practical implementations.

In addition to providing improved performance in applications requiring simultaneous frequency demodulation and A/D conversion, the suitability of ΔΣPLL's for phase demodulation opens the possibility of new ADPLL applications. For example, ΔΣPLL's can be used for coherent demodulation of continuous phase modulation signal formats such as minimum shift keying [6]. Conventional ADPLL's usually are not suitable for such applications because of the phase-drift problem mentioned above.

The paper is divided into three main sections and an appendix. Section II motivates the subsequent presentation by first describing how ΔΣPLL's can be used for frequency and phase demodulation. Section III and the Appendix present a detailed analysis of the general ΔΣPLL architecture. Existing ΔΣ modulator theory is applied to predict the accuracy of ΔΣPLL-based instantaneous frequency and phase estimation. Section IV presents a mechanization of the general ΔΣPLL architecture consisting of easily implemented components such as analog integrators, digital flip–flops, and digital counters.

The approach taken in this paper was first proposed in [7] and [8]. A distinct approach that gives rise to ADPLL's that are approximately analogous to ΔΣ modulators was presented in [9]. However, the ADPLL's presented in [9] are quite different than those presented in this paper, and they generate a digital approximation of the instantaneous period of the input rather than the instantaneous frequency.

II. Frequency-to-Digital and Phase-to-Digital Conversion

Before considering specific ΔΣPLL's, motivation will be provided by treating them as "black boxes" and considering how they can be used for frequency and phase demodulation. The ΔΣPLL's to be presented operate on $x_r(t)$ and output a coarsely quantized sequence of the form

$$y[n] = c\widehat{\psi}[n] + e_L[n] \tag{1}$$

where c and L are constants that depend on the particular ΔΣPLL, $\widehat{\psi}[n]$ corresponds to the instantaneous frequency of $x_r(t)$ at time t_n, and $e_L[n]$ is quantization error. In particular, L is a positive integer referred to as the *order* of the ΔΣPLL, and $e_L[n]$ is well modeled as the output of a filter with transfer function

$$N_L(z) = (1 - z^{-1})^L \tag{2}$$

driven by white noise. Consequently, the power spectral density (PSD) of $e_L[n]$ is proportional to $\sin^{2L}(\omega/2)$, so most of the error power resides at high frequencies. Thus, the ΔΣPLL quantizes instantaneous frequency in the same manner that a ΔΣ modulator quantizes amplitude [5].

A ΔΣPLL-based frequency demodulator consists of a ΔΣPLL followed by a lowpass filter as shown in Fig. 2(a). The sample-rate of the ΔΣPLL is chosen to be many times

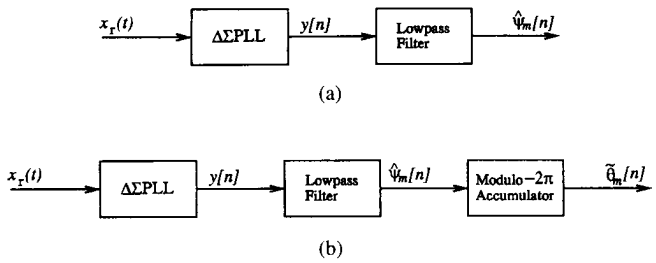


Fig. 2. The high-level structure of (a) a ΔΣFDC and (b) a ΔΣPDC.

higher than the Nyquist rate of the instantaneous frequency of $x_r(t)$, so $\widehat{\psi}[n]$ is restricted to a low frequency *baseband*. The lowpass filter is chosen to pass signal components within this baseband and reject higher frequency components, thereby removing the out-of-band quantization error. The result is a digital estimate of the instantaneous frequency of $x_r(t)$ that can be made increasingly accurate by increasing the sampling rate of the ΔΣPLL and appropriately decreasing the passband of the lowpass filter. In the next section, existing ΔΣ modulator results will be used to quantify this tradeoff.

Fig. 2(b) shows the corresponding ΔΣPLL-based phase demodulator. It consists of a ΔΣPLL-based frequency demodulator followed by a modulo-2π integrator that operates according to

$$\widetilde{\theta}_m[n] = \left[\widehat{\psi}_m[n] + \widetilde{\theta}_m[n-1]\right] \bmod 2\pi.$$

As will be shown, $\widetilde{\theta}_m[n]$ is equivalent (i.e., equal, modulo-2π) to the instantaneous phase of $x_r(t)$ at time t_n plus a constant plus an error term that is well modeled as the output of a filter with transfer function $N_{L-1}(z)H(z)$ driven by white noise, where $N_{L-1}(z)$ is the highpass transfer function given by (2) except with L replaced by $L-1$, and $H(z)$ is the transfer function of the lowpass filter in Fig. 2(b). Consequently, the comments made above with respect to the ΔΣPLL-based frequency demodulator also apply to the ΔΣPLL-based phase demodulator.

As described above, both ΔΣPLL-based frequency demodulators and ΔΣPLL-based phase demodulators perform A/D conversion simultaneously with frequency and phase demodulation. Therefore, for the remainder of the paper, they will be referred to as delta–sigma frequency-to-digital converters (ΔΣFDC's), and delta–sigma phase-to-digital converters (ΔΣPDC's), respectively.

III. The General ΔΣPLL Architecture and Theory

A. The ΔΣPLL Architecture

Fig. 3 shows the general form of the class of ΔΣPLL's considered in this paper. The number L can be any positive integer and the corresponding system is referred to as the Lth-order ΔΣPLL. Each ΔΣPLL consists of a sampled phase detector, a forward path transfer function equivalent to $L-1$ cascaded discrete-time integrators, an N-bit A/D converter, a

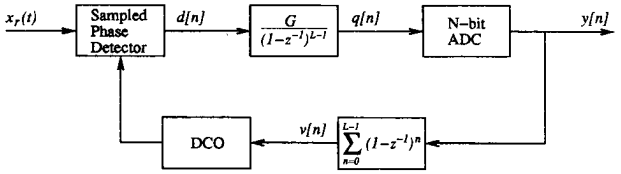


Fig. 3. The Lth-order $\Delta\Sigma$PLL.

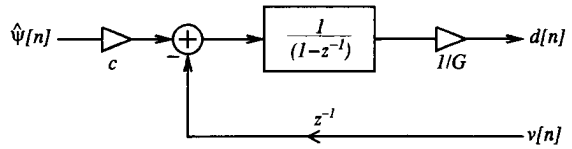


Fig. 4. The processing performed on $\hat{\psi}[n]$ by the combination of the DCO and the sampled phase detector.

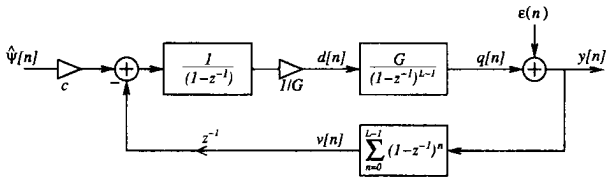


Fig. 5. The processing performed on $\hat{\psi}[n]$ by the Lth-order $\Delta\Sigma$PLL.

feedback transfer function of

$$\sum_{n=0}^{L-1}(1-z^{-1})^n$$

and a DCO. The DCO operates on the digital sequence $v[n]$ and generates an output signal whose instantaneous phase at time t_n is

$$\omega_c t_n + K_d \sum_{k=1}^{n} v[k-1] + \theta_1 \tag{3}$$

where ω_c is the *nominal center frequency* of $x_r(t)$, K_d is a positive constant referred to as the *DCO gain*, and θ_1 is an arbitrary initial phase of the DCO at time t_0. The sampled phase detector outputs a sequence proportional to the phase difference between its two inputs; the nth value of the sequence is K_p times the instantaneous phase difference between the two phase detector inputs measured at time t_n, where K_p is a constant referred to as the *phase detector gain*. The forward path gain factor is $G = (K_p K_d)^{-1}$, and the A/D converter performs uniform mid-tread quantization with step-size Δ.

B. The Assumed Input Signal

It is assumed that the input signal has the form

$$x_r(t) = A\sin\big(\omega_c t + \theta_x(t)\big) \tag{4}$$

where A is a constant amplitude, and $\theta_x(t)$ is the *instantaneous phase* relative to $\omega_c t$. The instantaneous phase can be written as

$$\theta_x(t) = \int_{t_0}^{t} \psi(\tau)d\tau + \theta_0 \tag{5}$$

where $\psi(t)$ is the *instantaneous frequency* relative to ω_c, and θ_0 is an arbitrary initial value of $\theta_x(t)$ at time t_0. Note that the nominal center frequency, ω_c, may not correspond exactly to the actual center frequency of $x_r(t)$. For example, an error in the frequency reference used to generate $x_r(t)$ may cause these values to differ. In general, the mean of $\psi(t)$ is equal to the difference between the actual and nominal center frequencies.

C. The $\Delta\Sigma$ Modulator Analogy

From (3)–(5), it follows that the output of the sampled phase detector at the nth sample time, t_n, is

$$d[n] = K_p\Big[\int_{t_0}^{t_n} \psi(\tau)d\tau - K_d \sum_{k=1}^{n} v[k-1] + \theta_0 - \theta_1\Big].$$

With the definition

$$\hat{\psi}[n] = \int_{t_{n-1}}^{t_n} \psi(\tau)d\tau \tag{6}$$

$d[n]$ can be written as

$$d[n] = K_p K_d \sum_{k=1}^{n}\Big(\frac{1}{K_d}\hat{\psi}[k] - v[k-1]\Big) + \alpha \tag{7}$$

where

$$\alpha = K_p(\theta_0 - \theta_1).$$

Hence, the combination of the DCO and sampled phase detector can be interpreted as the system shown in Fig. 4 with $c = 1/K_d$ and initial condition $d[0] = \alpha$. Accordingly, the $\Delta\Sigma$PLL of Fig. 3 processes $\hat{\psi}[n]$ as shown in Fig. 5 wherein the DCO and sampled phase detector have been replaced by the system of Fig. 4 and the A/D converter has been replaced by an additive quantization noise source. The quantization noise, $\varepsilon[n]$, is defined as $\varepsilon[n] = y[n] - q[n]$, so no approximation has been made by considering the A/D converter as an additive noise source.

In Fig. 5, let $S_L(z)$ be the transfer function between the $\hat{\psi}[n]$ input and the output, let $N_L(z)$ be the transfer function between the $\varepsilon[n]$ input and the output, and let $Q_L(z)$ be the transfer function between the $\varepsilon[n]$ input and the node corresponding to $q[n]$. Then, as proven in the Appendix,

$$S_L(z) = \frac{1}{K_d}, \qquad N_L(z) = (1-z^{-1})^L$$

and

$$Q_L(z) = -z^{-1}\sum_{n=0}^{L-1}(1-z^{-1})^n.$$

It follows that (1) holds with $c = 1/K_d$ and $e_L[n]$ equal to the output of a filter with transfer function $N_L(z)$ driven by $\varepsilon[n]$. It remains to characterize $\varepsilon[n]$.

The system of Fig. 5 can be viewed as a $\Delta\Sigma$ modulator in that it is a special case of the generic $\Delta\Sigma$ modulator presented and analyzed in [10]. It can also be rearranged to verify that

the A/D converter sees the same input sequence as the A/D converter in the L-loop $\Delta\Sigma$ modulator first presented in [11], and later considered in [12] and [13]. It follows from the results of [10]–[13] that, provided $N \geq L$ and $\widehat{\psi}[n]$ is appropriately bounded (the bound is derived below), the quantization noise, $\varepsilon[n]$, introduced by the A/D converter in the $\Delta\Sigma$PLL is well modeled as asymptotically white noise with power $\Delta^2/12$ that is asymptotically independent from $\widehat{\psi}[n]$. Therefore, the PSD of $e_L[n]$ is well modeled as

$$S_{e_L}(e^{j\omega}) = \frac{\Delta^2}{12}\left|N_L(e^{j\omega})\right|^2 = \frac{\Delta^2}{12}2^L \sin^{2L}(\omega/2). \quad (8)$$

D. $\Delta\Sigma$FDC Performance

It follows from the results presented in [12] that if $\widehat{\psi}[n]$ is restricted to a baseband of bandwidth $(-\pi/R, \pi/R)$, then the power of the portion of $e_L[n]$ that lies within the baseband is given by

$$n_{o_L}^2 = \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot R^{-(2L+1)}. \quad (9)$$

If the lowpass filter rejects signal components outside of the baseband and passes those within the baseband, then the power of the quantization error measured at the output of the lowpass filter is $n_{o_L}^2$. Thus, $n_{o_L}^2$ represents the minimum achievable quantization error power for a $\Delta\Sigma$FDC with given values of L and R. It follows from (9) that for a given bandwidth of $\psi(t)$, doubling the sample-rate of the sampled phase detector and halving the passband of the lowpass filter increases the precision of the $\Delta\Sigma$FDC by approximately $6(L + 1/2)$ dB which corresponds to $L + \frac{1}{2}$ bits.

Computer simulations show very close agreement with these theoretical results. For example, Fig. 6 shows $\Delta\Sigma$PLL simulation data corresponding to $L = 2$, 3, and 4. For each $\Delta\Sigma$PLL, Fig. 6(a) shows the estimated PSD of the quantization error, and Fig. 6(b) shows the corresponding values of $n_{o_L}^2$ versus R as calculated from the data in Fig. 6(a). The $\Delta\Sigma$PLL's were each simulated with an L-bit A/D converter (where L is the $\Delta\Sigma$PLL order), and $\widehat{\psi}[n] = -0.3183 \cdot K_d\Delta$. Each spectral estimation was performed by averaging ten periodograms corresponding to nonoverlapping Hanning windowed length-8192 segments of the simulated $\Delta\Sigma$PLL output. Each value of $n_{o_L}^2$ was calculated by integrating the corresponding PSD over the interval $(-\pi/R, \pi/R)$. As is evident from the figure, the simulated $\Delta\Sigma$PLL's perform as predicted by theory. The data in Fig. 6(a) and (b) closely support (8) and (9), respectively. Moreover, Fig. 6(b) indicates that for each doubling of R, $n_{o_L}^2$ decreases by $6(L + 1/2)$ dB as predicted.

If a fewer-than-L-bit A/D converter is used in an L-loop $\Delta\Sigma$ modulator or the amplitude of the input sequence is too large, the A/D converter can become overloaded (i.e., its usable input range can be exceeded) [12]. By analogy, the same must be true for an Lth-order $\Delta\Sigma$PLL. Whenever the A/D converter is overloaded, the $\Delta\Sigma$PLL also is said to be *overloaded*. At best, the in-band quantization error power of an overloaded $\Delta\Sigma$PLL is higher than the value of $n_{o_L}^2$ predicted above. At worst, the $\Delta\Sigma$PLL can become unstable.

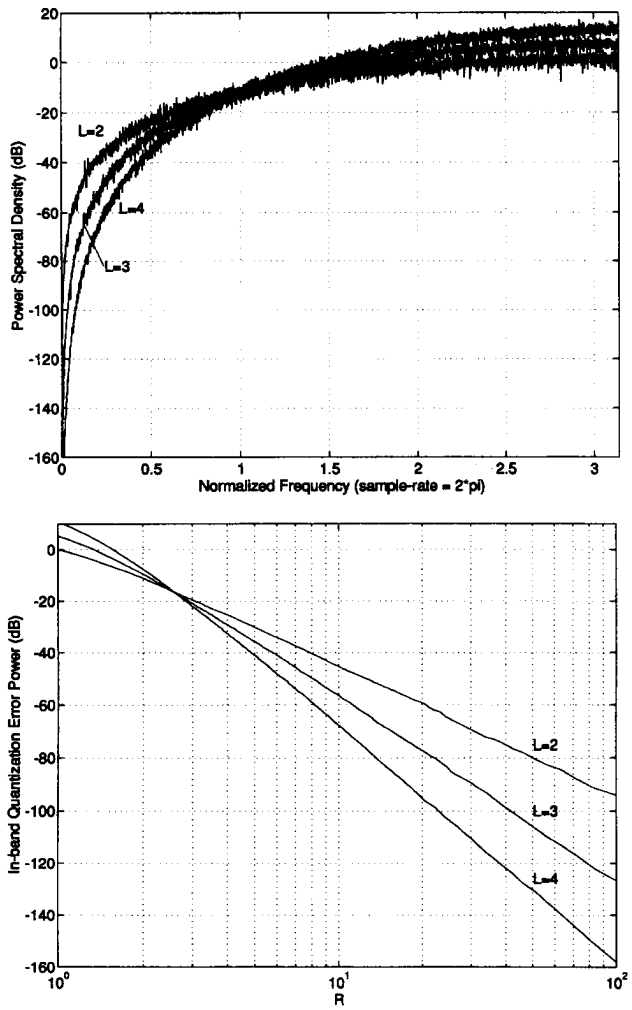


Fig. 6. (Top) Estimated power spectra of the quantization error introduced by simulated second, third, and fourth-order $\Delta\Sigma$PLL's and (Bottom) in-band quantization error power calculated from the data in (top).

It follows from a more general result shown in the Appendix that overload can be avoided in an Lth-order $\Delta\Sigma$PLL provided

$$-K_d\Delta\left[2^{N-1} - 2^{L-1} + 1\right] < \widehat{\psi}[n] < K_d\Delta\left[2^{N-1} - 2^{L-1}\right] \quad (10)$$

for all n (this result could have been derived using an extension of the corresponding argument presented in [13] for the L-loop $\Delta\Sigma$ modulator). This input amplitude range is referred to as the *no-overload range* of the $\Delta\Sigma$PLL. Note that, as in the case of the L-loop $\Delta\Sigma$ modulator, if $N < L$ then there is no positive no-overload range. Nevertheless, double-loop, second-order $\Delta\Sigma$ modulators with one-bit A/D converters have been experimentally shown to perform well for sufficiently small-amplitude input sequences because such sequences cause overload relatively infrequently [12]. As would be expected, this behavior is also evident in the second-order $\Delta\Sigma$PLL.

E. $\Delta\Sigma$PDC Performance

It will now be shown that the output of the $\Delta\Sigma$PDC of Fig. 2(b) is equal, modulo-2π, to

$$\theta_m[n] = \frac{1}{K_d}h[n] * \left[\theta_x(t_n) + \phi_0 + K_d e_{L-1}[n]\right] \quad (11)$$

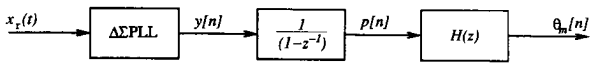


Fig. 7. A modified ΔΣFDC-based phase demodulator for derivation purposes.

where $h[n]$ is the impulse response of the lowpass filter, ϕ_0 is a constant, and e_{L-1} is equal to the output of a filter with transfer function $N_{L-1}(z)$ driven by $\varepsilon[n]$. Therefore, using the arguments made above for the ΔΣFDC, if $\theta_x(t_n)$ is restricted to a baseband of bandwidth $(-\pi/R, \pi/R)$, and the lowpass filter scales signal components within the baseband by K_d and rejects signal components outside the baseband, then the output of the ΔΣPDC is equal, modulo-2π, to

$$\theta_m[n] = \theta_x(t_n) + \phi_0 + \xi_L[n]$$

where $\xi_L[n]$ has power $K_d^2 \cdot n_{o_{L-1}}^2$ (provided the ΔΣPLL is not allowed to overload). The significance is that the ΔΣPDC generates a phase modulation estimate that does not drift away from the actual phase modulation (because $N_L(e^{j\omega})$ has a zero at $\omega = 0$), and that the estimation accuracy can be calculated using (9).

To verify (11) consider a modified phase demodulator in which the modulo-2π operator is omitted. Denoting the output of the modified phase demodulator as $\theta_m[n]$ it follows that

$$\widetilde{\theta}_m[n] = \theta_m[n] \bmod 2\pi. \tag{12}$$

Omitting the modulo-2π operator reduces the modulo-2π accumulator to a discrete-time integrator which may be interchanged with $H(z)$ without affecting the output of the system (because the integrator and $H(z)$ are linear time-invariant systems). The modified phase demodulator can thus be drawn as shown in Fig. 7. It follows from the figure that

$$p[n] = \sum_{k=1}^{n} y[k] + p[0] \tag{13}$$

where $p[0]$ is the initial condition of the integrator. From the derivation above

$$y[n] = \frac{1}{K_d} \int_{t_{n-1}}^{t_n} \psi(\tau) d\tau + e_L[n]. \tag{14}$$

Because $e_L[n]$ corresponds to $\varepsilon[n]$ filtered by $(1 - z^{-1})^L$, it follows that $e_L[n] = e_{L-1}[n] - e_{L-1}[n-1]$. Using this and substituting (14) into (13) gives

$$p[n] = \frac{1}{K_d}\left[\theta_x(t_n) + K_d e_{L-1}[n] - K_d e_{L-1}[0] - \theta_x(t_0) + p[0]\right].$$

From Fig. 7, $\theta_m[n] = h[n] * p[n]$ (11) follows with $\phi_0 = p[0] - K_d e_{L-1}[0] - \theta_x(t_0)$.

F. Acquisition Mode and Tracking Mode

As in the case of conventional ADPLL's, ΔΣPLL's can be viewed as having two modes of operation: *acquisition mode* and *tracking mode*. However, the definition of these two modes is somewhat different than for ADPLL's. The difference arises because ΔΣPLL's do not attenuate their own quantization error as do conventional ADPLL's.

When an input signal is first applied to the ideal ADPLL of Fig. 1, there is an initial transient response that depends on the initial conditions of the loop filter and the initial phase of the DCO. The ADPLL is said to be in acquisition mode until the transient response has died out (below a level determined by the precision requirements of the application) and then is said to be in tracking mode. However, this definition does not have a clear meaning if the ADPLL performs quantization, as do most conventional ADPLL mechanizations, because it is not possible to fully differentiate between the quantization error and the transient response in the ADPLL output. Nevertheless, most ADPLL mechanizations attenuate their quantization error to the point where it can be neglected to first-order so the definition can be applied as an approximation.

The problem with applying such a definition to the ΔΣPLL is that the quantization error component of the output can be larger than the signal component (prior to the external lowpass filtering). Nevertheless, a useful definition of the two modes does exist for ΔΣPLL's. Specifically, a ΔΣPLL is said to be in tracking mode at time n if the A/D converter is not overloaded at time n and did not overload at times $n-1, n-2, \cdots, n-2L+1$; otherwise, it is said to be in acquisition mode. The rational behind this definition is that the desired characteristics of the ΔΣPLL occur when overload is avoided, and it can be verified using the results presented in the Appendix that none of the nodes in the ΔΣPLL depend on more than the $2L-1$ most recent values of the quantization noise. Hence, the ΔΣPLL is not affected by A/D converter overload error introduced more than $2L-1$ sample-times in the past.

G. Sampled Phase Detector Operating Range

As will be shown in Section IV, knowledge of the maximum operating range of the sampled phase detector output, $d[n]$, during tracking mode is necessary in order to properly design the ΔΣPLL. Practical phase detectors have a maximum range, $[-\theta_{\max}, \theta_{\max}]$, over which they can measure phase differences. Therefore, it is important to choose the ΔΣPLL parameters such that $d_{\max} \leq \theta_{\max}$ where $d_{\max}$ is the maximum value attained by $|d[n]|$ during tracking mode. As shown in the Appendix, $d[n]$ does not contain a dc component during tracking mode so its operating range is symmetric about zero. Moreover, it is shown that if the ΔΣPLL is in tracking mode at time n, then

$$d_{\max} = K_p 2^{L-2}\left[\widehat{\psi}_{\max} - \widehat{\psi}_{\min}\right] + K_p K_d 2^{L-2}(2^L - 1)\Delta \tag{15}$$

where $\widehat{\psi}_{\max}$ and $\widehat{\psi}_{\min}$ are the upper and lower limits of $\widehat{\psi}[n]$, respectively. If overload is avoided by choosing $\widehat{\psi}_{\max}$ and $\widehat{\psi}_{\min}$ to be the extremes of the no-overload range given by (10), then (15) reduces to

$$d_{\max} = K_p K_d \Delta 2^{L+N-2}. \tag{16}$$

This bound is useful in the design of the ΔΣPLL presented in Section IV.

H. Tracking Behavior in the Presence of Noise

In ADPLL applications, the input signal is often corrupted by additive noise. In such cases, the corrupted input signal can be written in the form

$$x_r(t) = \big(A + r_n(t)\big)\sin\big(\omega_c t + \theta_x(t) + \theta_n(t)\big)$$

where $r_n(t)$ and $\theta_n(t)$ are envelope and phase deviations, respectively, arising from the additive input noise [14]. Usually, the envelope deviation is removed prior to frequency demodulation (e.g., using a bandpass limiter). Therefore, the output of an ideal frequency demodulator operating on such an input signal is $\psi(t) + \psi_n(t)$ where $\psi_n(t) = d\theta_n(t)/dt$ is an undesired instantaneous frequency error term arising from the additive noise.

In the case of a $\Delta\Sigma$FDC, the additive input noise causes $\widehat{\psi}[n]$ to have the form

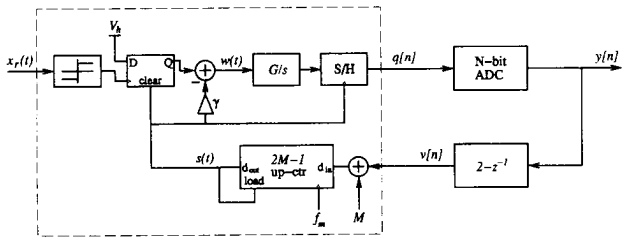
$$\widehat{\psi}[n] = \int_{t_{n-1}}^{t_n} \big[\psi(\tau) + \psi_n(\tau)\big]d\tau.$$

From the results presented above, provided (10) is satisfied and $d_{\max} \leq \theta_{\max}$ then the $\Delta\Sigma$FDC operates as an ideal frequency demodulator aside from quantization error. If $\psi_n(t)$ is bounded, then N, K_p, and K_d can be chosen such that these conditions are satisfied. In general, the sensitivity of a $\Delta\Sigma$PLL to additive input noise can be reduced by increasing N and choosing K_p and K_d so as to reduce $d_{\max}$.

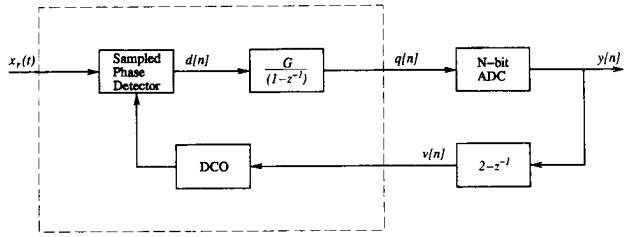
When the input noise is such that (10) is not satisfied, the $\Delta\Sigma$PLL may overload. In such cases, by the $\Delta\Sigma$ modulator analogy derived above, the error introduced by the overloaded $\Delta\Sigma$PLL is identical in form to that introduced by an overloaded $\Delta\Sigma$ modulator (provided $d_{\max} \leq \theta_{\max}$). While few theoretical results describing the error introduced by overloaded $\Delta\Sigma$ modulators are available currently, the approximate tradeoff between input amplitude and overload error are known from simulation results [5]. For example, for sinusoidal inputs the A/D conversion performance smoothly degrades as a function of input amplitude once (10) is exceeded. If the input noise is such that $d_{\max} > \theta_{\max}$, then it is likely that the error introduced by the $\Delta\Sigma$PLL will deviate from that of the corresponding $\Delta\Sigma$ modulator. Additional research is necessary to characterize this error and the corresponding performance tradeoffs.

IV. $\Delta\Sigma$PLL Mechanization

Thus far, the analysis of the $\Delta\Sigma$PLL has assumed that the DCO and sampled phase detector are ideal. However, as mentioned in the introduction, conventional DCO's are usually based on period linear devices that introduce nonlinearities into the loop equations thereby spoiling the achievable frequency and phase demodulation performance. This section presents a practical combined DCO and sampled phase detector mechanization that implements the ideal equations up to the analog accuracy of the components. To simplify the notation and figures, the specific example of a second-order $\Delta\Sigma$PLL is considered. The extension of the approach to higher-order $\Delta\Sigma$PLL's requires no new ideas.



(a)



(b)

Fig. 8. (a) A mechanization of the second-order $\Delta\Sigma$PLL and (b) the general form of the second-order $\Delta\Sigma$PLL.

Fig. 8(a) shows the proposed mechanization as applied to the second-order $\Delta\Sigma$PLL. For reference, the general form of the second-order $\Delta\Sigma$PLL (corresponding to Fig. 3 for the special case of $L = 2$) is shown in Fig. 8(b). As will be shown, the proposed mechanization of Fig. 8(a) is functionally equivalent to the $\Delta\Sigma$PLL of Fig. 8(b) because the subsystems contained within the dashed boxes in the two figures are functionally equivalent.

The system of Fig. 8(a) uses a hard limited version of the input signal to clock a D flip–flop whose data input is always high. The flip–flop is cleared on the rising edge of a signal, $s(t)$, that is generated as the carry bit of a digital up-counter. A scaled version of $s(t)$ is subtracted from the output of the flip–flop and the result is scaled by $G = (K_p K_d)^{-1}$ (these parameters will be derived below), integrated, and sampled-and-held on the rising edge of $s(t)$. The output of the sample-and-hold is converted to an N-bit digital sequence by a mid-tread A/D converter.

The subsystem within the dashed box of Fig. 8(b) consists of the DCO and sampled phase detector followed by a discrete-time integrator. Therefore, it is sufficient to show that, in the system of Fig. 8(a)

$$q[n] = G\sum_{k=1}^{n} d[k] + q[0] \tag{17}$$

where $d[n]$ has the form of (7) for some, as yet to be determined, constants K_p, K_d, and α. To this end, the following definitions are useful:

1) $t_0, t_1, t_2, \ldots$, are the times of the rising edges of the Q-output of the D flip–flop;
2) $\tau_0, \tau_1, \tau_2, \ldots$, are the times of the falling edges of the Q-output of the D flip–flop labeled such that $t_0 < \tau_0 < t_1 < \tau_1 \cdots$;
3) for each n, $q[n]$, $y[n]$, and $v[n]$ all correspond to the time interval $\tau_n \leq t < \tau_{n+1}$; and

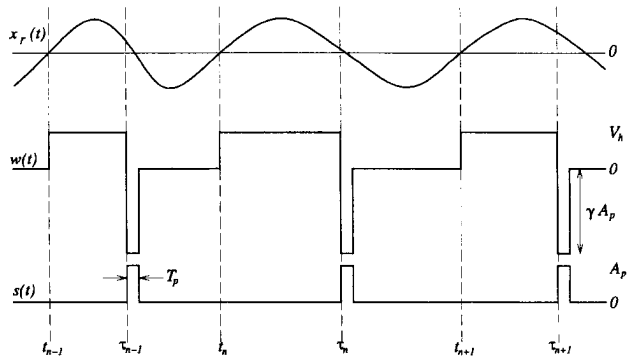


Fig. 9. Typical plots of $x_r(t)$, $w(t)$, and $s(t)$.

4) the logical high and low levels of the Q-output of the D flip–flop are V_h and 0, respectively.

From Fig. 8, it follows that

$$q[n] = G\int_{\tau_0}^{\tau_n} w(\tau)d\tau + q[0].$$

This can be rewritten as (17) with the definition that

$$d[n] = \int_{\tau_{n-1}}^{\tau_n} w(\tau)d\tau. \tag{18}$$

Therefore, it remains to show that (18) is equivalent to (7) for some constants K_p, K_d, and α.

As will be evident from the following derivation, during tracking mode each positive-going zero crossing of $x_r(t)$ occurs at one of the times t_n, and each rising edge of $s(t)$ occurs at one of the times τ_n. In the following derivation it will be assumed that after time t_0, the $\Delta\Sigma$PLL is in tracking mode. Fig. 9 shows typical plots of the signals $w(t)$ and $s(t)$ with $x_r(t)$ shown for reference. From the figure and (18), it follows that

$$d[n] = V_h(\tau_n - t_n) - \gamma A_p T_p \tag{19}$$

where A_p and T_p are the amplitude and duration, respectively, of the $s(t)$ pulses. To make further progress, expressions are required for τ_n and t_n in terms of $v[n]$ and $\widehat{\psi}[n]$.

To derive an expression for τ_n, the operation of the up-counter must be considered. The up-counter is clocked at a rate $f_m = Mf_c$ where M is a positive integer and $f_c = \omega_c/(2\pi)$. It operates as a variable-period pulse generator. When the counter reaches its terminal value of $2M - 1$, the carry bit (and, therefore, $s(t)$) goes high. On the next rising edge of the f_m-rate clock, the counter is loaded with the value $M + v[n-1]/\Delta$.[1] Thus, $M - v[n-1]/\Delta$ time intervals of duration $1/f_m = T_c/M$ separate τ_n and τ_{n-1}, where $T_c = 1/f_c$. With the definition that $\Delta_n = \tau_n - \tau_{n-1}$, it follows that

$$\Delta_n = T_c\left[1 - \left(\frac{1}{M\Delta}\right)v[n-1]\right]. \tag{20}$$

[1]The factor of $1/\Delta$ arises because it is customary to consider the LSB of a counter to be unity, but in this case the LSB of the counter corresponds to that of the A/D converter which has an implicit value of Δ (assuming mid-tread quantization). If mid-rise quantization were used, the factor would be $2/\Delta$ which would ultimately require f_m to be twice as large to achieve the same K_d.

By definition

$$\tau_n = \sum_{k=1}^{n}\Delta_k + \tau_0.$$

Expanding Δ_k using (20) leads to

$$\tau_n = \sum_{k=1}^{n} T_c\left[1 - \left(\frac{1}{M\Delta}\right)v[k-1]\right] + \tau_0. \tag{21}$$

To derive an expression for t_n, an expression for $\delta_n = t_n - t_{n-1}$ will be derived and substituted into

$$t_n = \sum_{k=1}^{n}\delta_k + t_0.$$

The phase of $x_r(t)$ can be written as $p_x(t) = 2\pi f_c t + \theta_x(t)$, so

$$\begin{aligned} p_x(t_n) - p_x(t_{n-1}) &= 2\pi f_c\delta_n + \theta_x(t_n) - \theta_x(t_{n-1}) \\ &= 2\pi f_c\delta_n + \widehat{\psi}[n]. \end{aligned} \tag{22}$$

Because the positive-going zero crossings of $x_r(t)$ occur at times t_n, it follows that $p_x(t_n) - p_x(t_{n-1}) = 2\pi$, so (22) can be rearranged as

$$\delta_n = T_c\left(1 - \frac{\widehat{\psi}[n]}{2\pi}\right). \tag{23}$$

Therefore

$$t_n = \sum_{k=1}^{n} T_c\left(1 - \frac{\widehat{\psi}[k]}{2\pi}\right) + t_0. \tag{24}$$

Substituting (21) and (24) into (19) and collecting terms results in

$$d[n] = V_h\left[\sum_{k=1}^{n} T_c\left(\frac{\widehat{\psi}[k]}{2\pi} - \frac{v[k-1]}{M\Delta}\right) + \tau_0 - t_0\right] - \gamma A_p T_p.$$

with the definitions

$$K_p = \frac{V_h T_c}{2\pi}, \qquad K_d = \frac{2\pi}{M\Delta}$$

and

$$\alpha = \frac{2\pi K_p}{T_c}(\tau_0 - t_0) - \gamma A_p T_p$$

this reduces to (7) as required.

It remains to select values for the scale factor γ and for the parameter M. Notice from the expressions for K_p, K_d, and α that γ only appears in the expression for α. At first glance, one might be tempted to eliminate the circuitry associated with γ in Fig. 8(a), effectively setting $\gamma = 0$. However, this would result in an unstable system. If γ were zero, then $w(t) \geq 0$ for all t (see Fig. 9). But $w(t)$ is integrated prior to A/D conversion (see Fig. 8(a)), so the magnitude of the A/D converter input would grow without bound and the $\Delta\Sigma$PLL would be unstable thereby violating the assumption made above that the $\Delta\Sigma$PLL is in tracking mode.

To avoid this problem, γ must be chosen to "bias" (19) so that $d[n]$ can attain both positive and negative values. In tracking mode, $0 < \tau_n - t_n < \delta_{n+1}$, so the right side of (19) has a limited range of possible values. Because $d[n]$ does

not have a dc component during tracking mode, the maximum range of the right side of (19) that is symmetric about zero can be interpreted as the maximum phase detection range, $[-\theta_{\max}, \theta_{\max}]$.

The worst-case range of (19) occurs when the separation between t_{n+1} and t_n is at its minimum. To maximize $\theta_{\max}$, this worst-case range must be symmetric about zero, which requires that $d[n]$ equal zero when τ_n is midway between minimally separated values of t_{n+1} and t_n. From (19), this occurs when

$$\gamma = \frac{V_h \delta_{\min}}{2A_p T_p}$$

where $\delta_{\min}$ is the minimum separation between t_{n+1} and t_n. Therefore, $\theta_{\max} = V_h \delta_{\min}/2$. From (23), it follows that

$$\delta_{\min} = T_c\left(1 - \frac{\widehat{\psi}_{\max}}{2\pi}\right).$$

If $\widehat{\psi}[n]$ is kept within the no-overload range of the $\Delta\Sigma$PLL, then from the right-side term of (10)

$$\widehat{\psi}_{\max} = K_d \Delta\left[2^{N-1} - 2^{L-1}\right] = \frac{2\pi}{M}\left[2^{N-1} - 2^{L-1}\right]$$

so

$$\theta_{\max} = \frac{V_h T_c}{2}\left[1 - \frac{1}{M}\left(2^{N-1} - 2^{L-1}\right)\right]. \tag{25}$$

From (16) and the expressions derived above for K_p and K_d, it follows that

$$d_{\max} = \frac{V_h T_c}{M} \cdot 2^{L+N-2}. \tag{26}$$

Substituting (26) and (25) into the inequality $d_{\max} \leq \theta_{\max}$ gives

$$M \geq 2^{L+N-1} + 2^{N-1} - 2^{L-1}. \tag{27}$$

Therefore, if M satisfies this inequality and $\widehat{\psi}[n]$ is within the no-overload range of the $\Delta\Sigma$PLL, then tracking mode can be maintained. For example, if a two-bit A/D converter is used in the $\Delta\Sigma$PLL of Fig. 8(a), then $L = N = 2$ so (27) reduces to $M \geq 8$. It follows that tracking mode can be maintained if f_m is at least eight times greater than f_c and $-2\pi/M < \widehat{\psi}[n] < 0$ for all n.

Simulations indicate that, under these conditions, the $\Delta\Sigma$PLL can achieve tracking mode from an otherwise arbitrary initial state provided the state variable of the analog integrator is clipped so that it does not exceed the no-overload range of the A/D converter. For example, if the integrator consists of an operational amplifier with a feedback capacitor, this requires that the operational amplifier output be limited to the no-overload range of the A/D converter.

Fig. 10 shows the in-band quantization error power, $n_{o_2}^2$, as a function of R for a simulated second-order $\Delta\Sigma$PLL mechanized as described in this section. The simulation was performed at the block diagram level of Fig. 8 using Simulink [15]. The Runge–Kutta 23 integration method was used with a minimum step-size of $1/(20f_m)$. The $\Delta\Sigma$PLL parameters were $M = 8$, $N = 2$, $V_h = 1$, and $\psi(t) = 0.0867\omega_c$. The spectral estimation and integration used to obtain the in-band

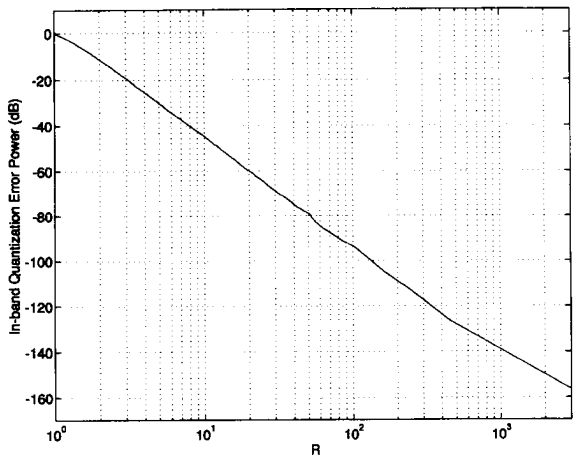


Fig. 10. In-band quantization error power from a simulated second-order $\Delta\Sigma$PLL of the form shown in Fig. 8(a).

quantization error were performed as described in Section III for the simulations corresponding to Fig. 6(b). As predicted by theory, the in-band quantization error power is virtually identical to that of the second-order $\Delta\Sigma$PLL simulated in Section III. Although not shown, the quantization error from the simulated $\Delta\Sigma$PLL has a PSD that is similarly indistinguishable from that of the second-order $\Delta\Sigma$PLL simulated in Section III.

The mechanization presented above illustrates an important point on which $\Delta\Sigma$PLL's are not analogous to $\Delta\Sigma$ modulators. In a multi-loop $\Delta\Sigma$ modulator, the noise introduced by the D/A converter does not undergo filtering as does the noise introduced by the A/D converter [5]. For this reason, the overall precision of practical $\Delta\Sigma$ modulator A/D converters employing multi-bit quantization is often limited by the precision of the D/A converter reference voltages. Moreover, greater than double-loop $\Delta\Sigma$ modulators do not enjoy widespread use because the benefits they offer with respect to better in-band quantization noise rejection usually are mitigated by their sensitivity to D/A conversion noise. However, the $\Delta\Sigma$PLL mechanization presented above does not contain an explicit D/A converter. Instead, the the D/A converter function is performed by the $2M - 1$ up-counter, and the D/A converter output levels correspond to the times at which the D flip–flop is cleared. Therefore, the accuracy of the $\Delta\Sigma$PLL is not limited by errors in D/A converter reference voltages, but rather by the jitter introduced by the master clock. Since it is considerably easier to generate low-jitter clock signals than high-precision reference voltages, the use of multi-bit quantization in $\Delta\Sigma$PLL's does not present the same level of difficulties as in the case of $\Delta\Sigma$ modulators.

V. Conclusion

A new class of ADPLL's, referred to as $\Delta\Sigma$PLL's, has been presented. The $\Delta\Sigma$PLL's have been shown to compare favorably to conventional ADPLL's in that their quantization error is well behaved and they can be implemented using practical DCO's without inducing nonlinear tracking mode behavior. With external digital filtering to remove out-of-band quantization error, the $\Delta\Sigma$PLL's can be used to accurately

estimate the instantaneous frequency of an analog angle-modulated input signal. Moreover, the estimated instantaneous frequency can be discrete-time integrated modulo-2π to obtain an instantaneous phase estimate that does not drift away from the actual instantaneous phase. Consequently, $\Delta\Sigma$PLL's can be used for coherent demodulation of continuous phase modulation communication signals in addition to the usual ADPLL frequency demodulation applications. An analogy between $\Delta\Sigma$PLL's and $\Delta\Sigma$ modulators has been established, and existing $\Delta\Sigma$ modulator theory has been applied to predict the performance of $\Delta\Sigma$PLL-based frequency and phase demodulators. A specific mechanization of the general architecture that consists of easily implemented components also has been presented. Additional research is necessary to characterize the performance of $\Delta\Sigma$PLL's during acquisition mode, and with nonideal components and noisy input signals.

APPENDIX

Theorem A1: In Fig. 5 for each positive integer L, let $S_L(z)$ be the transfer function between the $\widehat{\psi}[n]$ input and the output, let $N_L(z)$ be the transfer function between the $\varepsilon[n]$ input and the output, and let $Q_L(z)$ be the transfer function between the $\varepsilon[n]$ input and the node corresponding to $q[n]$. Then

$$S_L(z) = \frac{1}{K_d}, \qquad N_L(z) = (1 - z^{-1})^L$$

and

$$Q_L(z) = -z^{-1} \sum_{n=0}^{L-1} (1 - z^{-1})^n.$$

Proof: The proof involves the application Mason's Gain Formula to the signal flow graph equivalent of Fig. 5 [16]. The first step is to find the determinant of Fig. 5, $\Delta_L(z)$. By inspection

$$\Delta_L(z) = 1 - \frac{-z^{-1} \sum_{n=0}^{L-1} (1 - z^{-1})^n}{(1 - z^{-1})^L}. \tag{28}$$

Therefore, for any positive integer k

$$\Delta_{k+1}(z) - \Delta_k(z) = \frac{z^{-1}}{(1 - z^{-1})^{k+1}}.$$

If $\Delta_k(z) = (1 - z^{-1})^{-k}$, this implies $\Delta_{k+1}(z) = (1 - z^{-1})^{-(k+1)}$. From (28), $\Delta_1(z) = (1 - z^{-1})^{-1}$, so, by the principle of induction

$$\Delta_L(z) = (1 - z^{-1})^{-L} \tag{29}$$

for all positive integers L. Dividing the corresponding forward path transfer functions by $\Delta_L(z)$ yields the expressions for $S_L(z)$, $N_L(z)$, and $Q_L(z)$. □

Theorem A2: Suppose that the A/D converter in the $\Delta\Sigma$PLL of Fig. 3 performs uniform quantization with step-size Δ and no-overload range (β_l, β_h). Then the $\Delta\Sigma$PLL will not overload at time n provided it has not overloaded at times $n-1, n-2, \cdots, n-L$, and

$$K_d\left[\beta_l + (2^L - 1)\frac{\Delta}{2}\right] < \widehat{\psi}[n] < K_d\left[\beta_h - (2^L - 1)\frac{\Delta}{2}\right]. \tag{30}$$

Proof: In the system of Fig. 5, the transfer function between the $\widehat{\psi}[n]$ input and the node corresponding to $q[n]$ is $S_L(z) = K_d^{-1}$, and the transfer function between the $\varepsilon[n]$ input and the node corresponding to $q[n]$ is

$$Q_L(z) = -z^{-1} \sum_{n=0}^{L-1} (1 - z^{-1})^n.$$

Therefore, $q[n]$ only depends on the current value of the input sequence and the previous L values of the quantization noise sequence. Since the A/D converter did not overload at any of the previous L sample-times, it follows that $|\epsilon[k]| \le \Delta/2$ for $k = n-1, n-2, \cdots, n-L$. Therefore

$$\frac{\widehat{\psi}[n]}{K_d} - \frac{\Delta}{2} Q_{L_{\max}} \le q[n] \le \frac{\widehat{\psi}[n]}{K_d} + \frac{\Delta}{2} Q_{L_{\max}} \tag{31}$$

where

$$Q_{L_{\max}} = \sum_n |q_L[n]|$$

and $q_L[n]$ is the impulse response associated with $Q_L(z)$. It follows from the expression for $Q_L(z)$ and the definition of the z-transform that $Q_{L_{\max}} = Q_L(-1)$. Thus, $Q_{L_{\max}} = \sum_{n=0}^{L-1} 2^n$, or, equivalently, $Q_{L_{\max}} = 2^L - 1$.

To avoid overload at time n, it is sufficient to have

$$\beta_l < q[n] < \beta_h.$$

Therefore, from (31) the following two conditions are sufficient to ensure that overload does not occur at time n:

$$\frac{\widehat{\psi}[n]}{K_d} - \frac{\Delta}{2}(2^L - 1) > \beta_l$$

and

$$\frac{\widehat{\psi}[n]}{K_d} + \frac{\Delta}{2}(2^L - 1) < \beta_h.$$

These can be rearranged and combined as (30). □

Theorem A3: In the $\Delta\Sigma$PLL of Fig. 3 with $L > 1$, the zero-frequency component of the output of the sampled phase detector, $d[n]$, is zero during tracking mode. Moreover, if the modulator loop is in tracking mode at time n, then

$$|d[n]| \le K_p 2^{L-2}[\widehat{\psi}_{\max} - \widehat{\psi}_{\min}] + K_p K_d 2^{L-2}(2^L - 1)\Delta \tag{32}$$

where $\widehat{\psi}_{\max} = \max_n\{\widehat{\psi}[n]\}$ and $\widehat{\psi}_{\min} = \min_n\{\widehat{\psi}[n]\}$ are the upper and lower limits of $\widehat{\psi}[n]$, respectively.

Proof: In Fig. 5, let $D_{\widehat{\psi}}(z)$ be the transfer function between the $\widehat{\psi}[n]$ input and the node corresponding to $d[n]$, and let $D_\varepsilon(z)$ be the transfer function between the $\varepsilon[n]$ input and the node corresponding to $d[n]$. It follows from (29) and Mason's Gain Formula that

$$D_{\widehat{\psi}}(z) = K_p(1 - z^{-1})^{L-1}$$

and

$$D_\varepsilon(z) = -K_p K_d z^{-1}(1 - z^{-1})^{L-1} \sum_{n=0}^{L-1} (1 - z^{-1})^n.$$

Both of these transfer functions have a zero at zero-frequency, so the zero-frequency component of $d[n]$ must be zero provided $\widehat{\psi}[n]$ and $\varepsilon[n]$ are bounded (as is the case during tracking mode).

Let

$$D_{\widehat{\psi}_{\max}} = \sum_n \left|d_{\widehat{\psi}}[n]\right| \qquad \text{and} \qquad D_{\varepsilon_{\max}} = \sum_n \left|d_{\varepsilon}[n]\right|$$

where $d_{\widehat{\psi}}[n]$ and $d_{\varepsilon}[n]$ are the impulse responses associated with $D_{\widehat{\psi}}(z)$ and $D_{\varepsilon}(z)$, respectively. It follows from the expressions for $D_{\widehat{\psi}}(z)$ and $D_{\varepsilon}(z)$ and the definition of the z-transform that $D_{\widehat{\psi}_{\max}} = D_{\widehat{\psi}}(-1) = K_p 2^{L-1}$ and $D_{\varepsilon_{\max}} = D_{\varepsilon}(-1) = K_p K_d 2^{L-1}(2^L - 1)$.

From the expression for $D_{\widehat{\psi}}(z)$, it follows that the largest possible contribution to $\left|d[n]\right|$ from $\widehat{\psi}[n]$ occurs when $\widehat{\psi}[n]$ alternates between $\widehat{\psi}_{\max}$ and $\widehat{\psi}_{\min}$. Thus, the contribution to $\left|d[n]\right|$ from $\widehat{\psi}[n]$ is less than or equal to $\frac{1}{2}\left[\widehat{\psi}_{\max} - \widehat{\psi}_{\min}\right] D_{\widehat{\psi}_{\max}}$. The largest possible contribution to $\left|d[n]\right|$ from $\varepsilon[n]$ is $D_{\varepsilon_{\max}}$ times the largest value of $\left|\varepsilon[n]\right|$ over the previous $2L-1$ time indices. Because the $\Delta\Sigma$PLL is in tracking mode at time n, it follows that this value is bounded by $\Delta/2$. Therefore

$$\left|d[n]\right| \le \frac{1}{2}\left[\widehat{\psi}_{\max} - \widehat{\psi}_{\min}\right] D_{\widehat{\psi}_{\max}} + \frac{\Delta}{2} D_{\varepsilon_{\max}}$$

from which (32) follows. □

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