A Robust Parallel Delta-Sigma A/D Converter Architecture

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ABSTRACT

This paper presents an A/D converter architecture in which four 4^{th} order $\Delta\Sigma$ modulator channels are operated in parallel at a time-oversampling ratio of 10 to obtain an ideal signal-to-quantization error ratio corresponding to 18-bits. The architecture has the property that any x-bit decrease in individual $\Delta\Sigma$ modulator conversion performance due to non-ideal circuit behavior causes an $x+1$-bit decrease in the overall A/D conversion performance. The additional error caused by gain and offset mismatches among the four channels is either tolerable or removable using a simple digital compensation scheme. Thus, much of the robustness of $\Delta\Sigma$ modulators is preserved.

INTRODUCTION

Because of their amenability to VLSI implementation, $\Delta\Sigma$ modulator A/D converters have received increasing interest from researchers in industry and academia in recent years. A major drawback of the $\Delta\Sigma$ modulator A/D conversion approach is the requirement of time-oversampling. With current technology, the oversampling requirement for large bandwidth applications such as video processing is prohibitive [1]. A new A/D converter architecture, referred to as the $\Pi\Delta\Sigma$ modulator A/D converter, for which the oversampling requirement is greatly reduced, has been presented [2]. A low quantization error floor is obtained by operating M P^{th} order $\Delta\Sigma$ modulators in parallel at a moderate oversampling ratio N. This paper describes a specific design example of the new architecture for which extensive simulations and an estimate of the hardware complexity are presented. Two important results are that the system is relatively insensitive to various types of non-ideal circuit behavior, and the digital portion of the circuitry has low complexity relative to conventional $\Delta\Sigma$ modulator A/D converters.

ARCHITECTURE

The oversampling $\Pi\Delta\Sigma$ modulator A/D converter architecture example is shown in Figure 1. It consists of four channels that all operate on the 10-fold oversampled input sequence, $x[n]$. On each channel, the input sequence is multiplied by a channel-specific periodic ±1 sequence (the multiplication is not shown explicitly for the upper channel since the sequence is all ones), then $\Delta\Sigma$ modulated, lowpass filtered, 10-fold downsampled, and multiplied by a delayed version of the channel-specific ±1 sequence. The outputs of the four channels are added to produce the overall output, $y[n]$.

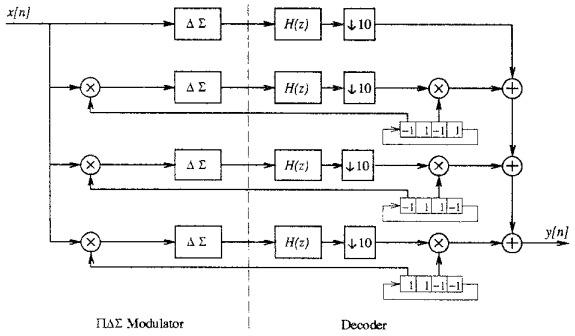

Figure 1: The 4-channel, 10-fold oversampling $\Pi\Delta\Sigma$ADC architecture example.

Each ±1 sequence is called a *Hadamard sequence* because it is constructed by periodically repeating one row of a 4×4 *Hadamard matrix*, $\mathbf{H}$. The Hadamard matrix consists exclusively of plus and minus ones and has the property that $\mathbf{H}^T\mathbf{H} = 4\mathbf{I}$ where $\mathbf{I}$ is the identity matrix. Row 0 of a Hadamard matrix can be chosen to consist of all ones, and multiplying the corresponding channel by that sequence leaves the signal unchanged. The process of multiplying by a Hadamard sequence, referred to as *Hadamard modulation*, requires the capability of analog sign inversion for the multipliers prior to the $\Delta\Sigma$ modulators, and the capability of digital sign inversion for those following the downsamplers. The architecture employs a 4^{th}-order $\Delta\Sigma$ modulator on each channel, each consisting of two 2^{nd}-order $\Delta\Sigma$ modulators in a double-loop configuration [3]. Each 2^{nd}-order $\Delta\Sigma$ modulator contains a 3-level quantizer [4]. The lowpass filter has transfer function

$$H(z) = \left(\frac{1-z^{-40}}{1-z^{-1}}\right)^5,$$

which is of a form known as a comb^5 filter.

Throughout the paper, the following terminology is used. The portion of the system containing the analog ±1 multipliers and the $\Delta\Sigma$ modulators is referred to as the *$\Pi\Delta\Sigma$ modulator*, and the portion containing the digital filters, downsamplers, digital ±1 multipliers, and channel summers is referred to as the *decoder*. The full $\Pi\Delta\Sigma$ modulator A/D converter is referred to as the *$\Pi\Delta\Sigma$ADC*. To preserve some generality in the following, the oversampling ratio and the number of channels will

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be referred to as N and M, respectively. The length of the FIR filter $H(z)$ will be referred to as J.

THE WORKINGS OF THE ΠΔΣADC

It can be shown [2], [5], that passing the input sequence $x[n]$ through the ΠΔΣADC is equivalent to subjecting it to a linear filter $H'(z)$, adding a quantization error component (a result of quantization in the ΔΣ modulators), and downsampling. Hence, the output can be considered the sum of an *overall signal component* $w[n]$ and an *overall quantization error component* $e[n]$.

An expression for $H'(z)$ is derived in [2] for slightly restricted conditions. Generalizing the result leads to

$$H'(z) = Mz^{-2} \sum_{i=-\infty}^{\infty} \sum_{k=iMN+\frac{J-N}{2}}^{iMN+\frac{J+N}{2}-1} h[k]z^{-k}.$$

Thus, the filter seen by the input sequence $x[n]$ depends on every length-N band of $h[n]$ symmetric about every MN^{th} tap relative to the center tap.

Because of oversampling, the power of the input sequence is restricted to the frequency band $(-\frac{\pi}{N}, \frac{\pi}{N})$. Since the zeros of $H'(e^{j\omega})$ lie outside this band, recovering the input sequence is possible with an equalization filter following the output of the ΠΔΣADC. The filter must approximate (a delayed version of)

$$F(e^{j\omega}) = 1/H'(e^{j\frac{\omega}{N}}), 0 \le |\omega| \le \pi.$$

An optimal odd-length FIR approximation of $F(e^{j\omega})$ can be implemented using the Parks-McClellan algorithm [6]. As an example, a length-81 FIR filter was designed such that the overall signal filter $H'(e^{j\frac{\omega}{N}})F(e^{j\omega})$ is linear phase and equiripple with a peak ripple of 0.004%. Figure 2a shows the magnitude response of this equalization filter.

Figure 2b, which shows plots of the magnitude responses of $H(e^{j\omega})$ and $H'(e^{j\omega})$, illustrates a property unique to the ΠΔΣADC compared to traditional ΔΣ modulator A/D converters. For both converter architectures, the purpose of $H(e^{j\omega})$ is to filter out as much of the quantization error as possible without distorting $x[n]$ beyond repair. In traditional ΔΣ modulator A/D converters, $H(e^{j\omega})$ cannot have zeros within the interval $(-\frac{\pi}{N}, \frac{\pi}{N})$ since $H(e^{j\omega})$ also filters $x[n]$. This restricts the amount of quantization error that can be removed from the ΔΣ modulator output. In the ΠΔΣADC architecture, however, *different* filters are applied to the signal component and the quantization error of the ΔΣ modulator output. The figure shows that $H(e^{j\omega})$ can have a much narrower passband than $(-\frac{\pi}{N}, \frac{\pi}{N})$, resulting in more efficient filtering of the quantization error.

THE ΠΔΣADC PERFORMANCE

A good measure of the ΠΔΣADC quantization error performance is the power of the overall quantization error component after equalization. An expression for the autocorrelation of the overall quantization error component before equalization is derived in [2].

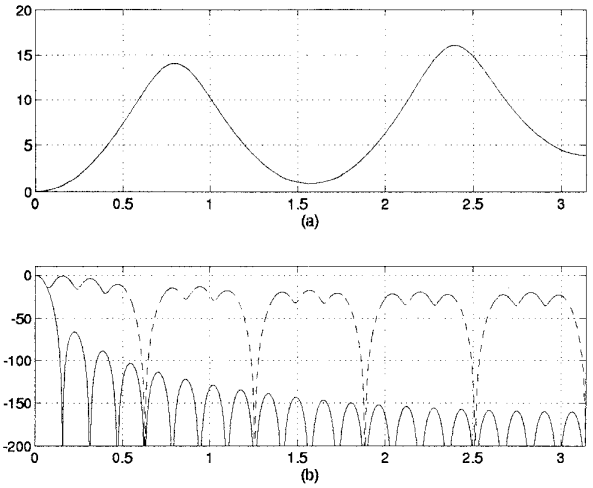

Figure 2: Magnitude response in dB of (a) the equalization filter $F(e^{j\omega})$, and (b) the lowpass filter $H(e^{j\omega})$ (solid line) and the signal filter $H'(e^{j\omega})$ (dashed line).

From this it follows that the corresponding power spectral density (PSD) is

$$\frac{\Delta^2}{12N} \sum_{n=0}^{M-1} \sum_{k=0}^{N-1} \left| N(e^{j(\frac{\omega}{N}+\frac{2\pi}{N}(\frac{n}{M}-k))}) H(e^{j(\frac{\omega}{N}+\frac{2\pi}{N}(\frac{n}{M}-k))}) \right|^2,$$

where Δ is the quantization step-size of the quantizers in the ΔΣ modulators, and $N(z) = (1-z^{-1})^4$ is the highpass filter to which the quantization error of the ΔΣ modulators is subjected. Multiplying by $\left|F(e^{j\omega})\right|^2$ and integrating gives the power of the quantization error component after equalization:

$$P_e = \frac{M\Delta^2}{24\pi} \int_{-\pi}^{\pi} \left| N(e^{j\omega}) H(e^{j\omega}) F(e^{j\omega N}) \right|^2 d\omega.$$

Numerically evaluating the expression for P_e yields -118 dB relative to Δ^2. Simulations indicate that a conservative estimate of the usable input range of the ΔΣ modulators is $(-0.4\Delta, 0.4\Delta)$, resulting in a quantization error power level corresponding to 18 bits of A/D conversion precision [7]. Figure 3a shows the calculated PSD of the equalized version of $e[n]$, and Figure 3b shows the estimated PSD of the equalized output of the ΠΔΣADC design example as obtained by computer simulation. The input was a sinusoid of amplitude 0.40Δ and frequency $\frac{875}{1024}\pi$ radians. The spectral estimation was performed by averaging 15 periodograms corresponding to half-overlapping Hanning windowed length-2^{16} segments of the simulated ΠΔΣADC output, and then scaling the result by $\left|F(e^{j\omega})\right|^2$ to achieve equalization. As is apparent from the figures, the PSD of the quantization error component obtained by removing the overall signal component matches the theoretical PSD extremely well. Furthermore, the corresponding power evaluates to -117 dB, in close agreement with the theoretical result.

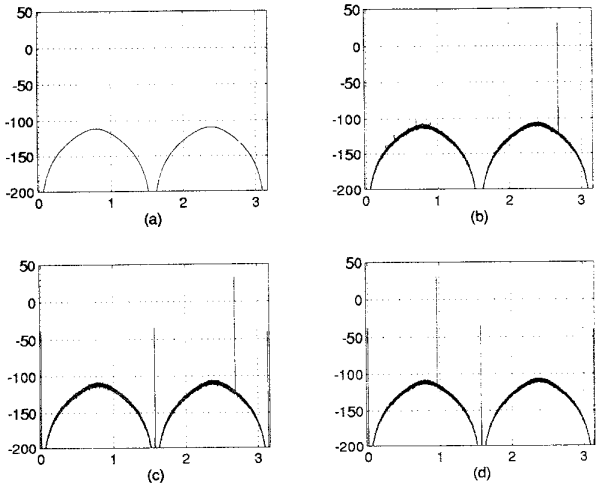

Figure 3: Power spectral density in dB relative to Δ^2 of (a) the equalized theoretical quantization error, (b) the equalized simulated output of the $\Pi\Delta\Sigma$ADC with a sinusoidal input and ideal circuit behavior, (c) the equalized simulated output of the $\Pi\Delta\Sigma$ADC with a sinusoidal input and randomly chosen value of d_r to within $\pm 10^{-4}$, and (d) the same simulation as Figure 3c, except a different frequency of the input signal.

NON-IDEAL CIRCUIT BEHAVIOR

In practice, non-ideal circuit behavior reduces the conversion precision below that predicted by the above analysis. Non-ideal circuit behavior will add a 3rd term, the *overall circuit error component*, to the output of the converter. Since the $\Pi\Delta\Sigma$ADC employs $\Delta\Sigma$ modulators, it suffers from the same types of non-ideal circuit behavior as $\Delta\Sigma$ modulator A/D converters. There are, additionally, circuit errors that are unique to the $\Pi\Delta\Sigma$ADC, and the overall circuit error component can therefore be considered the sum of two subcomponents: the *conversion error subcomponent* (CES) and the *reconstruction error subcomponent* (RES). The CES originates from all types of non-ideal $\Delta\Sigma$ modulator performance arising from non-ideal circuit behavior except for $\Delta\Sigma$ modulator signal component gain and offset errors, and the RES originates from all non-ideal circuit behavior that is not part of the CES. Because of the decorrelating effect of the digital Hadamard modulation, the components of the CES from each channel add in power, not amplitude, when the channel outputs are summed. Since the architecture consists of 4 channels, an extra 6dB is added to the power of the overall ciruit error component originating from the $\Delta\Sigma$ modulators. As an example, the noise floor originating from input-referred electronic noise of the $\Delta\Sigma$ modulators is 6dB higher at the output of the $\Pi\Delta\Sigma$ADC than it would be at the output of the corresponding conventional $\Delta\Sigma$ modulator A/D converter with the same oversampling ratio.

The RES is unique to the $\Pi\Delta\Sigma$ADC and results from non-ideal analog Hadamard modulator behavior and from mismatches among the signal component gains and offsets of the $\Delta\Sigma$ modulators. In the following, let $u_r[n]$ denote the ± 1 sequence of the rth channel of the modulator and let $v_r[n]$ denote the ± 1 sequence of the rth channel of the decoder. Figure 4a and Figure 4b show the signal path with ideal and non-ideal circuit behavior, respectively. All circuit errors specific to the $\Pi\Delta\Sigma$ADC can be included in the equivalent circuit of Figure 4b. Ideally, the signal component of the output of the $\Delta\Sigma$ modulator on the r^{th} channel is of the form $x[n-2]u_r[n-2]$. From Figure 4b, it follows that with non-ideal circuit behavior, the signal component of the output of the $\Delta\Sigma$ modulators is of the form

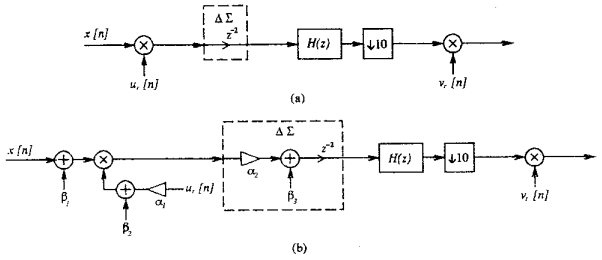

Figure 4: Signal equivalent circuits for (a) ideal circuit behavior, and (b) non-ideal circuit behavior.

$$(1+a_r)x[n-2]u_r[n-2]+b_r x[n-2]+c_r u_r[n-2]+d_r,$$

where $a_r = \alpha_1\alpha_2 - 1$, $b_r = \alpha_2\beta_2$, $c_r = \alpha_1\alpha_2\beta_1$, and $d_r = \alpha_2\beta_1\beta_2 + \beta_3$.

Deriving an expression for the overall circuit error component leads to

$$\sum_{k=0}^{\infty} h[k-2]x[nN-2]\sum_{r=0}^{M-1} v_r[n](a_r u_r[nN-2]+b_r)+$$

$$\sum_{k=0}^{\infty} h[k-2]\sum_{r=0}^{M-1} v_r[n](c_r u_r[nN-2]+d_r),$$

from which it can be verified that random deviations of a_r, b_r, c_r, and d_r from zero result in A/D conversion errors of the same order of magnitude. Figures 5 and 6 show simulation data that demonstrate the effect of increasing magnitude of the RES on the spurious-free dynamic range and the power of the sum of the quantization error component and the RES, respectively. For each plot, only one of a_r, b_r, c_r, or d_r was non-zero, thereby isolating the effect of each of the four terms of the RES. The frequency of the sinusoidal input signal was $\frac{875}{1024}\pi$ radians. The circuit errors were chosen randomly such that each of a_r, b_r, c_r, and d_r could maximally assume values of 10^{-6}, 10^{-5}, 10^{-4}, 10^{-3}, and 10^{-2}. Four $\Pi\Delta\Sigma$ADCs with different random number seeds were simulated, and the corresponding simulation data was plotted with point types +, $*$, o, and x. The solid lines represent averages of the plotted data. From both figures it is apparent that the performance is insensitive to c_r, little sensitive to b_r, somewhat sensitive to a_r, and most sensitive to d_r.

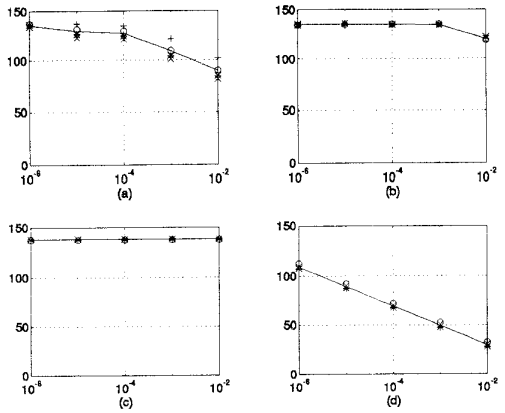

Figure 5: Spurious-free dynamic range in dB of the equalized $\Pi\Delta\Sigma$ADC output vs. magnitude of randomly chosen values of (a) a_r, (b) b_r, (c) c_r and (d) d_r, respectively.

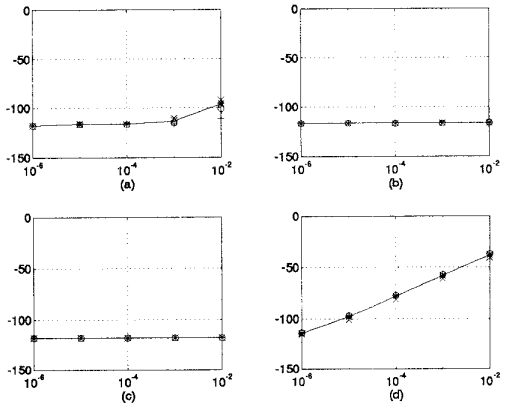

Figure 6: Power in dB relative to Δ^2 of the sum of the quantization error component and the reconstruction error subcomponent of the equalized $\Pi\Delta\Sigma$ADC output vs. magnitude of randomly chosen values of (a) a_r, (b) b_r, (c) c_r and (d) d_r, respectively.

For example, as can be seen from Figure 5a, if the channel gains are ideal to within 0.1%, more than 100dB of spurious-free dynamic range is retained. Figure 3c and 3d show the PSD of the equalized $\Pi\Delta\Sigma$ADC output for the case where the DC offset introduced by the $\Delta\Sigma$ modulators was chosen randomly so as to obtain a value of d_r within $\pm 10^{-4}$ for sinusoidal inputs of frequency $\frac{875}{1024}\pi$ radians and $\frac{625}{2048}\pi$ radians, respectively. The figures show that this causes a DC offset plus half-rate and full-rate sinusoidal components to superimpose on the $\Pi\Delta\Sigma$ADC output. Note, in particular, that, as predicted by theory, these components do not depend on the input signal. Since the error components represent half-rate and full-rate sinusoids, digitally compensating for the effects of d_r is possible by simply adding appropriately scaled ± 1 sequences to the output. Of course, to do this, the scale factors must be known or measured.

HARDWARE COMPLEXITY

In conventional $\Delta\Sigma$ modulator A/D converter architectures, the circuit area required to implement the decimation filter is typically more than an order of magnitude larger than that required for the $\Delta\Sigma$ modulator. It is therefore of interest to obtain an estimate of the number of multipliers, adders and delay elements needed to implement the decoder and the equalization filter for the $\Pi\Delta\Sigma$ADC.

The decoder employs 4 comb^5 filters and 3 adders to sum the channels. As shown in [1], each of the comb^5 filters requires 5 adders clocked at the sample-rate of $x[n]$ and 5 adders clocked at the output sample-rate. Referring the rate of additions to the rate of $x[n]$, this corresponds to 5.25 additions per unit time (APUs). Furthermore, 25 delay elements are required. Considering all four channels, the decoder requires a total of 21.15 APUs and 100 delay elements. The equalization filter is of length 81 with symmetric coefficients. Therefore an implementation requires 4 APUs, 2 multiplications per unit time (MPUs) and 80 delay elements. The total requirement for decoder and equalization filter is, thus, 25.15 APUs, 2 MPUs and 180 delay elements. Additional hardware is necessary to realize a digital compensation circuit that removes the effects of non-zero $\Delta\Sigma$ modulator DC-offset. Since this amounts to adding two scaled versions of ± 1 corresponding to half-rate and full-rate sinusoids, this should not require more than 0.1 APUs and no MPUs . By comparison, the corresponding computational complexity for a conventional 4^{th}-order $\Delta\Sigma$ modulator A/D converter [3] is 58.42 APUs and 12.3 MPUs assuming that the oversampling ratio is referred to 10. Implementing the decoder and equalization filter therefore promises to be hardware efficient relative to the complexity of the decimation and equalization filters in conventional $\Delta\Sigma$ modulator A/D converters.

ACKNOWLEDGEMENTS

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