Higher-Order Delta-Sigma Frequency-to-Digital Conversion

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ABSTRACT

Techniques have recently been proposed for simultaneously performing angle-demodulation and A/D conversion that offer the potential of reduced circuit complexity over conventional approaches. The techniques give rise to systems that operate on the instantaneous frequency of an angle modulated input signal in the same manner that $\Delta\Sigma$ modulators operate on instantaneous amplitude. This paper presents various new structures that are analogous to higher-order $\Delta\Sigma$ modulators in terms of their quantization noise shaping capabilities. The tradeoffs associated with the higher-order systems are discussed, and simulations are presented.

INTRODUCTION

Phase-tracking circuits are used in a multitude of communications and instrumentation applications such as phase-coherent demodulation, carrier tracking, timing recovery, bit synchronization, and Doppler measurement. Because of the trend toward digital signal processing, it is increasingly necessary to perform analog-to-digital (A/D) conversion in addition to phase-tracking. In such cases, phase-tracking and A/D conversion are usually performed separately, and relatively precise analog circuitry is required for even moderate levels of digital conversion accuracy. Two related techniques have recently been proposed that simultaneously perform phase-tracking and A/D conversion and offer the potential of reduced analog circuit complexity [1], [2]. This paper extends the technique proposed in [1].

The technique gives rise to a family of systems referred to as delta-sigma frequency-to-digital converters ($\Delta\Sigma$FDCs). Like a phase-locked loop, each $\Delta\Sigma$FDC tracks the phase and frequency of its input signal. However, unlike a phase-locked loop, it performs coarse analog phase measurements using a low resolution A/D converter sampled at many times the Nyquist rate of the modulation bandwidth, and employs quantization noise shaping and decimation filtering to obtain an accurate digital estimate of the instantaneous frequency of its input. Accordingly, $\Delta\Sigma$FDCs operate on instantaneous frequency in the manner that $\Delta\Sigma$ modulator A/D converters operate on amplitude.

This paper briefly reviews the basic idea presented in [1] and then develops an extension of the idea that allows $\Delta\Sigma$FDCs with higher-order noise shaping capability to be developed. Like higher-order $\Delta\Sigma$ modulator A/D converters, higher-order $\Delta\Sigma$FDCs offer the potential of increased digital conversion accuracy for a given circuit clock rate. Furthermore, as discussed below, higher-order $\Delta\Sigma$FDCs offer advantages with respect to settling time.

THE $\Delta\Sigma$FDC APPROACH

In the following, it is assumed that each $\Delta\Sigma$FDC operates on a signal of the form:

$$x_r(t) = A\cos\Big(2\pi f_c t + 2\pi\int_{-\infty}^{t}\phi(\tau)d\tau\Big) + n(t),$$

where A is a constant amplitude, f_c is a constant carrier frequency, $\phi(t)$ is a frequency modulation signal with bandwidth $B \ll f_c$, and $n(t)$ is an undesired noise term that will be referred to as *channel noise*. The purpose of each $\Delta\Sigma$FDC is to produce an accurate digitized estimate of $\phi(t)$.

The high-level structure of each $\Delta\Sigma$FDC is shown in Figure 1. It is similar to that of a $\Delta\Sigma$ modulator A/D converter in that it consists of a *modulator loop* and a *lowpass decimation filter*. The modulator loop operates on the input signal, $x_r(t)$, and produces a coarsely quantized sequence, $y[n]$, at a sample rate many times the Nyquist rate of $\phi(t)$. As discussed in [1], the modulator loop output can be considered the sum of three components: a component corresponding to $\phi(t)$, a component corresponding to $n(t)$, and a component corresponding to quantization error. The component corresponding to $\phi(t)$ is restricted to a low frequency portion of the spectrum because of the high sampling rate, and the modulator loop shapes the spectra of the other components so that most of the their power resides at high frequencies. The decimation filter preserves the component corresponding to $\phi(t)$ while removing the out-of-band portions of the other components. The result, $\tilde{\phi}[m]$, is a multi-bit digitized representation of $\phi(t)$.

The simplest $\Delta\Sigma$FDC modulator loop is the first order structure shown in Figure 2 [1]. It consists of a phase detector, a sample-and-hold, a $(K_v K_p T_s)^{-1}$ gain element, an N-bit A/D converter, and a controlled oscillator. Ideally, the phase detector produces a voltage equal to a positive constant, K_p, times the difference in phase of its two analog inputs (ignoring any amplitude modulation), and the controlled oscillator produces a continuous-phase sinusoid with instantaneous frequency equal to f_c plus a positive constant, K_v, times its input value. The subsystem consisting of the phase detector,

sample-and-hold, and controlled oscillator is common to all of the higher order modulator loops and will be referred to as the modulator front end (MFE).

At the n^{th} sample time, the output of the sample-and-hold can be written as

$$d[n] = K_p\Big[\int_{-\infty}^{nT_s}\phi(\tau)d\tau - K_v\int_{-\infty}^{nT_s}y(\tau)d\tau\Big],$$

where $y(t)$ is the zero-order hold continuous-time version of $y[n]$, and $T_s = 1/f_s$ is the sample interval. This can be simplified as

$$d[n] = K_p\sum_{k=-\infty}^{n}\Big[\widehat{\phi}[k] - K_v y[k-1]T_s\Big],$$

where

$$\widehat{\phi}[n] = \int_{(n-1)T_s}^{nT_s}\phi(\tau)d\tau.$$

Hence, the MFE can be interpreted as the system shown in Figure 3. This implies that the system of Figure 2 is equivalent to a first-order $\Delta\Sigma$ modulator [3] in terms of how it processes $\widehat{\phi}[n]$. Because f_s is much greater than the Nyquist rate of $\phi(t)$, it follows that $\widehat{\phi}[n] \approx T_s\phi(nT_s)$ with a high degree of accuracy. With the definition that *quantization noise*, $\epsilon[n]$, is the difference between the output and the input of the A/D converter at time n, a network analysis shows that the output of the modulator loop is

$$y[n] \approx \frac{1}{K_v}\phi(nT_s) + e[n].$$

where $e[n] = \epsilon[n] - \epsilon[n-1]$. The sequence $e[n]$ is the error at the output of the modulator loop due to the quantization performed by the A/D converter and is referred to as *quantization error*. The modulator loop thus subjects the quantization noise to the first-order highpass filter $1 - z^{-1}$. As a result, the quantization error has zero DC power and tends to be weighted toward high frequencies.

Higher-order modulator loops subject the quantization noise to sharper highpass filters, so the quantization error power tends to be weighted toward still higher frequencies. As with $\Delta\Sigma$ modulators, increasing the order offers the potential of increased digital conversion precision for a given sampling rate. Another potential benefit of higher-order $\Delta\Sigma$FDC modulator loops relates to settling time. The speed at which a $\Delta\Sigma$FDC settles after the modulator loop coarsely locks to an input signal is a function of the group delay of the decimation filter which is inversely related to the filter transition bandwidth. Since for a given digital conversion accuracy, the transition bandwidth of the filter can be increased with the $\Delta\Sigma$FDC modulator loop order, higher-order $\Delta\Sigma$FDCs can be made to settle faster than lower-order $\Delta\Sigma$FDCs with the same digital conversion accuracy.

It follows that any $\Delta\Sigma$ modulator with a front-end equivalent to the system of Figure 3 has a corresponding $\Delta\Sigma$FDC modulator loop. For example, a second-order $\Delta\Sigma$FDC was proposed in [1] based on the classic double-loop second-order $\Delta\Sigma$ modulator. However, a problem with this and other such structures arises because one of the feedback paths is through the controlled oscillator, and the other is through a traditional D/A converter. It is desirable to avoid structures requiring a D/A converter in addition to the controlled oscillator because generating sinusoids at precise frequencies is considerably easier than generating precise D/A reference levels. This is especially important for modulator loops that employ multi-bit A/D converters because as in the case of $\Delta\Sigma$ modulators, the error introduced by the D/A converters is not noise-shaped [3].

MULTI-LOOP STRUCTURES

This need for a separate D/A converter is avoided in the modulator loop of Figure 4a. Redrawing the system with the MFE replaced by the system of Figure 3, results in the system of Figure 4b which has the form of a single-stage second-order $\Delta\Sigma$ modulator [3]. Hence, this modulator loop operates on the instantaneous frequency of its input signal as a single-stage second-order $\Delta\Sigma$ modulator. Accordingly,

$$y[n] \approx \frac{1}{K_v}\phi(nT_s) + e[n],$$

where $e[n] = \epsilon[n] - 2\epsilon[n-1] + \epsilon[n-2]$.

The idea involves the equivalent of both frequency and phase modulating the controlled oscillator. In the modulator loop of Figure 4a, the transfer function between the A/D converter and the controlled oscillator is $2 - z^{-1}$. Thus, the controlled oscillator is controlled by the sum of the A/D converter output, $y[n]$, and its discrete-time derivative, $y[n] - y[n-1]$. The effect of the discrete-time derivative is to modulate the phase of the controlled oscillator (as measured at each sample time). Thus the phase detector and controlled oscillator gains control the gain of both feedback paths in Figure 4b.

The approach can be used to generate still higher-order $\Delta\Sigma$FDCs. For example, the modulator loop of Figure 5 corresponds to a three-loop, third-order $\Delta\Sigma$ modulator [3]. For an L^{th}-order modulator loop of this form, the feed-forward path contains $L-1$ discrete-time integrators and the transfer function between the A/D converter and controlled oscillator is

$$\sum_{k=0}^{L-1}(1 - z^{-1})^k.$$

As with the corresponding $\Delta\Sigma$ modulator, such an L^{th}-order modulator loop is unconditionally stable only if it has an L-bit or greater precision A/D converter.

Computer simulations support these results. For example, Figure 6 shows the estimated power spectral densities of the simulated outputs of the modulator loops of Figures 4a and 5. The FM modulation signal was a sinusoid of frequency $0.0098f_s$, and the spectral estimation was performed by averaging overlapping Hanning windowed periodograms of length 4096 from an array of 163,840 points. The smoother of the two curves corresponds to the third-order modulator loop, and the

rougher curve corresponds to the second-order modulator loop. The data are clearly consistent with the theory.

MULTI-STAGE STRUCTURES

Modulator loops corresponding to multi-stage $\Delta\Sigma$ modulators can be generated using a similar technique. For example, the multi-stage modulator loop of Figure 7a operates on the instantaneous frequency of its input signal as the two-stage second-order $\Delta\Sigma$ modulator of Figure 7b [3]. Accordingly,

$$y[n] \approx \frac{1}{K_v}\phi(nT_s) + 2e[n],$$

where $e[n] = \epsilon_2[n] - 2\epsilon_2[n-1] + \epsilon_2[n-2]$, and $\epsilon_2[n]$ is the quantization noise introduced by the upper A/D converter shown in Figure 7a. The modulator loop uses the same frequency and phase modulation principle as the modulator loop of Figure 4a It consists of two stages: the lower modulator loop stage controls the frequency modulation of both controlled oscillators while the upper modulator loop only controls the phase modulation of its own controlled oscillator. Hence, the frequency tracking dynamics are controlled solely by the lower modulator loop.

Provided the phase detectors approximate linear behavior, gain matching of the stages in the two-stage second-order modulator loop of Figure 7a is determined completely by the controlled oscillators. This is because there is no connection from inside the feedback loop of one stage to the other. Therefore, there is no need to match the gains of the individual stages as there is in two-stage second-order $\Delta\Sigma$ modulators. The two-stage second-order modulator loop appears to be special in this respect. Higher-order multi-stage modulator loops with this property are not known to the author.

The modulator loop of Figure 7a is is has an important special property. Unlike the second-order modulator loop of Figure 4a, this modulator loop is unconditionally stable, and has a non-zero *no-overload range* with only one-bit A/D converters. Specifically, the one-bit A/D converters within the modulator loop will not overload provided $|\phi(t)| < K_v/2$ for all t. Moreover, with one-bit A/D converters the modulator loop is not sensitive to variations in phase detector gain. This is evident from Figure 7a where the only gain terms dependent upon K_p immediately precede the one-bit D/A converters (where their magnitudes have no effect on the A/D converter outputs). The gain, K_p, of most practical phase detectors is input amplitude dependent, so without such K_p insensitivity, the gain and no-overload range of a modulator loop will depend upon the amplitude of the input signal. Therefore, the modulator loop of Figure 7a is appropriate in cases (e.g., low input SNR cases) where bandpass limiting $x_r(t)$ prior to the modulator loop is undesirable.

MFE CONSIDERATIONS

The modulator loops presented in the previous section require controlled oscillators with multi-bit inputs. Moreover, they are sensitive to frequency errors in their controlled oscillators just as $\Delta\Sigma$ modulators are sensitive to level errors in their D/A converters. Fortunately, generating sinusoids at precise frequencies is considerably easier than generating precise D/A reference levels. For example, very high-precision frequency control can be achieved using a direct digital synthesizer (DDS). Moreover, the DDS technique is amenable to efficient VLSI implementation. For example, VLSI DDS's are widely available with bandwidths exceeding 40MHz (e.g., the Analog Devices AD9955).

Moreover, simulations indicate that high-precision D/A converters are not necessary for the DDS approach. For example, Figure 8a shows the estimated power spectral density of the output of a simulated ideal two-stage second-order modulator loop, and Figure 8b shows the corresponding data for a simulation wherein a 6-bit D/A converter was used for the DDS. Although degradation of the noise shaping is evident, it is not severe. This is generally true because quantization noise introduced by the controlled oscillators tends to be noise-shaped along with the quantization noise from the A/D converters.

Phase detector non-linearity and wrap-around can be problematic in $\Delta\Sigma$FDCs as they are in phase-locked loops. For example, multiplier type phase detectors introduce a sinusoidal non-linearity into the loop, and can only resolve phase differences between $\pm\pi$ radians. If the sample-rate, f_s, is large compared to the controlled oscillator gain, K_v, and the signal to channel noise ratio (SNR) of the input signal, $x_r(t)$, is large, then such phase detectors behave approximately as linear phase detectors, and phase wrap-around is not a problem. For example, the simulation data shown in Figure 8c was generated in the same manner as that of Figure 8a except that a phase detector with a sinusoidal non-linearity was used. In this high-SNR case, no performance degradation is evident. However, the phase modulation approach utilized to develop the structures described above assumes phase detector linearity. Therefore, as the SNR of $x_r(t)$ decreases, the performance of these modulator loops degrade. This is evident in the simulation of Figure 8d which corresponds to that of Figure 8c except that the input SNR was 20dB.

ACKNOWLEDGMENT

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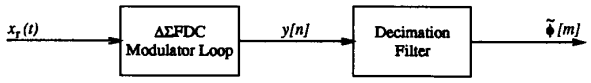

Figure 1: The high-level structure of a $\Delta\Sigma$FDC.

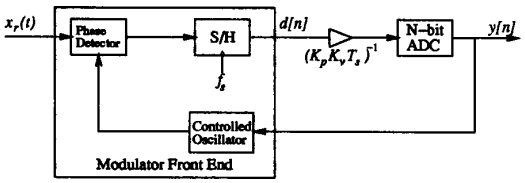

Figure 2: The first-order $\Delta\Sigma$FDC modulator loop.

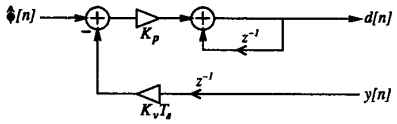

Figure 3: MFE equivalent system.

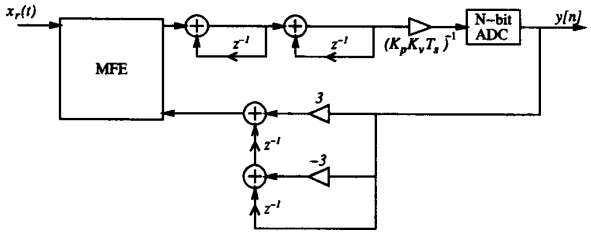

Figure 5: A 3-loop 3rd-order modulator loop.

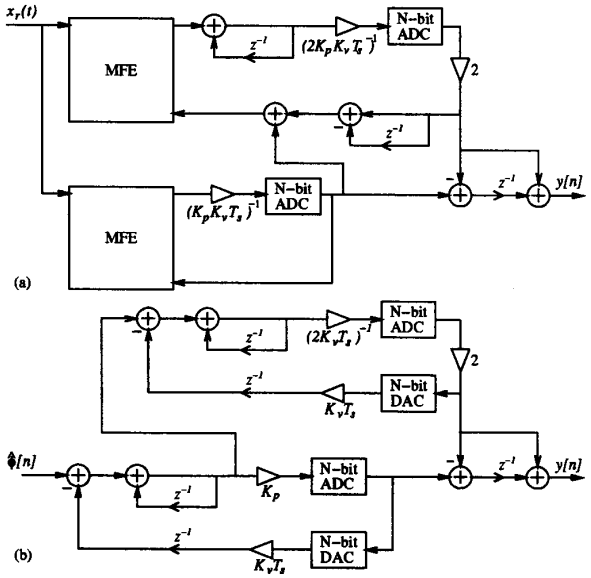

Figure 7: a) A 2-stage, 2nd-order modulator loop, b) the corresponding $\Delta\Sigma$ modulator.

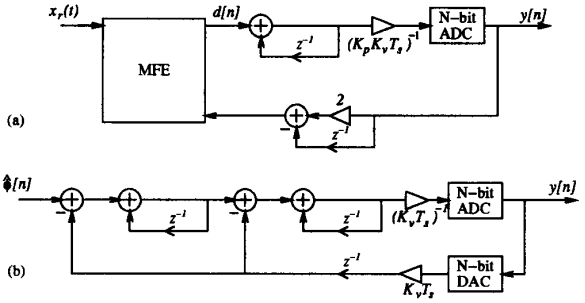

Figure 4: a) A 2-loop, 2nd-order modulator loop, b) the corresponding $\Delta\Sigma$ modulator.

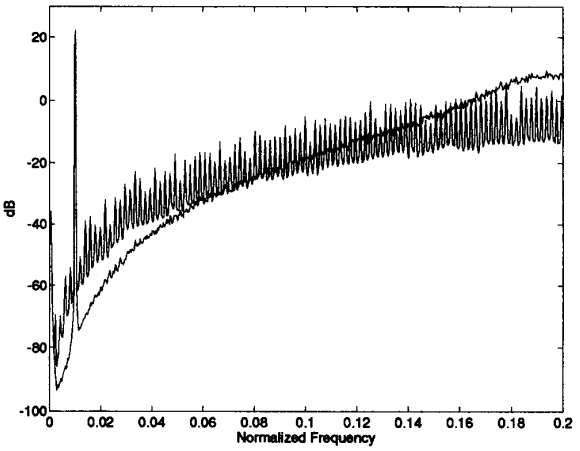

Figure 6: Estimated power spectra of simulated 2nd and 3rd-order modulator loops.

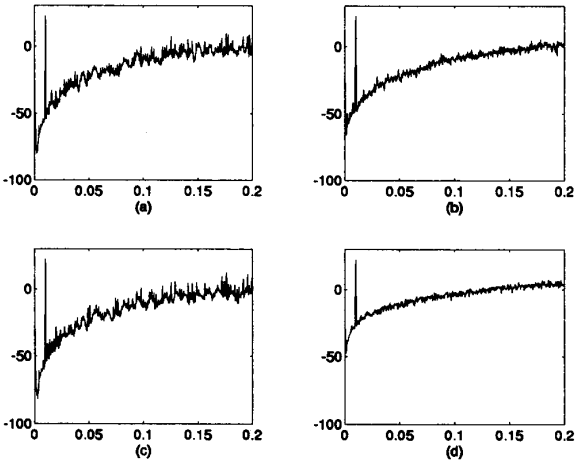

Figure 8: Estimated power spectra of simulated 2-stage 2nd-order modulator loops.