Combined RF Phase Extraction and Digitization

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Abstract—Phase-tracking problems are ubiquitous in communication systems, and the trend toward digital signal processing is rapidly necessitating the juxtaposition of RF phase-tracking and A/D conversion. This paper presents a new technique for simultaneously performing these functions. The approach offers the potential of reduced analog circuit complexity and cost over the traditional method of performing the functions separately.

I. Introduction

In most radio receivers that perform angle demodulation or carrier synchronization, it is necessary to extract phase information from the received signal. In digital radio receivers, analog intermediate frequency (IF) downconversion of the radio frequency (RF) signal is usually necessary prior to phase extraction and digitization. This is partly because A/D converters with sufficient bandwidth to directly sample radio frequency (RF) signals are only just becoming available, but mainly because prohibitively fast and complex digital circuitry is required to extract phase information from directly sampled RF signals. Unfortunately, the precise analog circuitry necessary for downconversion and IF digitization usually requires trimmed components and is not suitable for implementation using cheap, high-density VLSI processes.

This paper proposes a new approach that combines phase extraction and A/D conversion in a single system capable of operating directly on RF input signals. The ability to operate directly at RF stems from the use of very simple analog components. Aside from the economy gained by eliminating the need for IF downconversion and combining two previously separate functions, a major advantage of the approach is that it is relatively insensitive to non-ideal analog circuit behavior. Because it places most of the accuracy burden on digital signal processing, the analog circuit requirements are minimal. Therefore, the approach is well suited to VLSI implementation.

The remainder of the paper is divided into three sections. Section II describes the approach and considers two simple systems based on it. Section III discusses various circuit component considerations, and Section IV presents simulation results.

II. The Delta-Sigma FDC Principle

The approach gives rise to a family of systems. Each member of the family will be referred to as a delta-sigma frequency-to-digital converter ($\Delta\Sigma$FDC) because it processes the frequency modulation of its input in much the same way that a delta-sigma ($\Delta\Sigma$) modulator-based A/D converter operates on the amplitude of its input signal.

The input signal will be taken to have the following form:

$$x_r(t) = A\cos\left(2\pi f_c t + 2\pi\int_{-\infty}^{t}\phi(\tau)d\tau\right) + n(t),$$

where A is a constant amplitude, f_c is a constant carrier frequency, $\phi(t)$ is a frequency modulation signal with bandwidth $B \ll f_c$, and $n(t)$ is an undesired noise term that will be referred to as *channel noise*. The purpose of each of the $\Delta\Sigma$FDCs is to produce an accurate digitized estimate of $\phi(t)$.

Each $\Delta\Sigma$FDC consists of a *modulator loop* and a *lowpass decimation filter*. The modulator loop operates on the input signal, $x_r(t)$, and produces a coarsely quantized sequence at a sample rate, f_s, that is many times the Nyquist rate of $\phi(t)$. As discussed below, the output can be considered the sum of three components: a component corresponding to $\phi(t)$, a component corresponding to $n(t)$, and a component corresponding to quantization error. The component corresponding to $\phi(t)$ is restricted to a low frequency portion of the spectrum because of the above-Nyquist sampling rate. As will be shown, the modulator loop shapes the spectra of the other components so that most of the their power resides at high frequencies. The decimation filter functions as a lowpass digital filter of bandwidth B followed by a decimator. Its purpose is to preserve the output component corresponding to $\phi(t)$ while removing the out-of-band portions of the other output components and reduce the output sample rate to the Nyquist rate of $\phi(t)$. The result is a multi-bit digitized representation of $\phi(t)$.

The simplest $\Delta\Sigma$FDC is the first-order system of Figure 1. Its modulator loop consists of a phase detector, a sample-and-hold, a hard limiter, and a *binary voltage controlled oscillator* (VCO). The binary VCO differs from traditional VCOs in that it need only be capable of generating one of two sinusoids during each clock cycle. In the next section, some of the issues surrounding non-ideal circuit behavior will be considered, but for now it will suffice to assume that the VCO produces a continuous-phase sinusoid with instantaneous frequency equal to f_c plus a positive constant, K_v, times its input voltage. Similarly, for now the phase detector will be assumed to produce a voltage equal to a positive constant, K_p, times the difference in phase of its two analog

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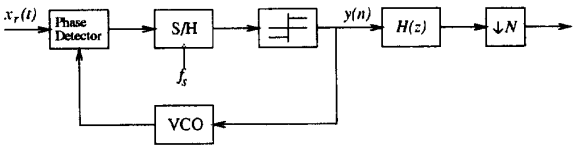

Figure 1: The first order delta-sigma FDC.

inputs (ignoring any amplitude modulation). Because of the hard limiter, the output of the modulator loop, $y(n)$, is a one-bit sequence.

By virtue of the sample-and-hold the modulator loop can be considered to consist of a continuous-time and a discrete-time portion. In reality, signals following the sample-and-hold are still continuous-time signals, but are only updated at the sample times. However, when it is convenient to refer to a sampled-and-held variable, say $y(t)$, as the corresponding discrete-time sequence, it will be denoted as $y(n)$ and should be interpreted as the value of $y(t)$ just after the n^{th} sample time.

It is illustrative to first consider the following simple case. Suppose that $\phi(t) = \phi_0$ is a constant where $|\phi_0| < K_v$, and that $n(t)$ is zero. Thus, $x_r(t)$ is a pure sinusoid of frequency $f_c + \phi_0$. At each sample time, the output of the sample-and-hold is updated with the difference between the phase of $x_r(t)$ and the phase of the VCO output. If at some sample time this value is positive, the output of the hard limiter will be a positive one and the instantaneous frequency of the VCO will be updated (if necessary) to $f_c + K_v$. Since $f_c + K_v > f_c + \phi_0$, at some time in the future the output of the phase detector must go negative. Provided the sample rate, f_s, is greater than $2K_v$, the output of the sample-and-hold will also eventually go negative and the instantaneous frequency of the VCO will be updated to $f_c - K_v$. Similarly, if at some sample time the output of the sample-and-hold is negative, the output of the hard limiter will be a negative one and the instantaneous frequency of the VCO will be updated (if necessary) to $f_c - K_v$. Again provided f_s is greater than $2K_v$, the output of the sample-and-hold will eventually go positive because $f_c - K_v < f_c + \phi_0$. This argument is still valid if applied to sufficiently narrow-band angle modulated signals centered near f_c.

By this reasoning, it is evident that the first-order modulator loop "loosely" tracks the phase and frequency of the input signal. To prove that the corresponding $\Delta\Sigma$FDC produces a high-precision digital conversion of $\phi(t)$ in the absence of channel noise, it remains to show that the spectrum of the output component corresponding to quantization error occupies predominantly high frequencies while the component corresponding to $\phi(t)$ is not spectrally distorted. As discussed above, this allows the lowpass decimation filter to remove much of the quantization error without significantly distorting the component of the output corresponding to $\phi(t)$.

The manner in which the first-order modulator loop processes $\phi(t)$ is shown in Figure 2a. The integrator following the input converts the frequency modulation term, $\phi(t)$, into an absolute phase. Similarly, the integrator in the feedback loop converts the VCO frequency modulation into an absolute phase. The phase detector

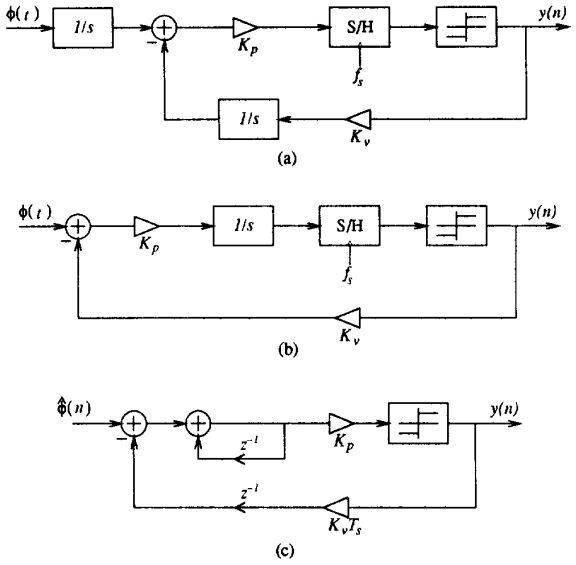

Figure 2: The operation of the first-order modulator loop on the frequency modulation of $x_r(t)$.

corresponds to the differencer shown in the figure. The K_v and K_p scalar multipliers arise from the VCO and phase detector gains, respectively. Because integration is linear, the two integrators in Figure 2a can be moved to the right of the phase detector and combined without changing the system as shown in Figure 2b. Just after the n^{th} sample time, the output of the sample-and-hold must be

$$d(n) = \int_{-\infty}^{nT_s} K_p\big[\phi(\tau) - K_v y(t)\big]d\tau,$$

where $T_s = 1/f_s$ is the sampling interval. Since $y(t)$ is a sampled-and-held signal, this equation can be rewritten as the difference equation:

$$d(n) = \sum_{i=-\infty}^{n} K_p\big[\widehat{\phi}(i) - K_v T_s y(i-1)\big],$$

where

$$\widehat{\phi}(n) = \int_{(n-1)T_s}^{nT_s} \phi(\tau)d\tau.$$

It follows that the system of Figure 2b can be redrawn in a discrete-time form as shown in Figure 2c. The two systems are equivalent in the sense that they produce the same output sequences. Moreover, because f_s is much greater than the Nyquist rate of $\phi(t)$, it follows that $\widehat{\phi}(n) \approx \phi(nT_s)$ with a high degree of accuracy.

Note that aside from the K_vT_s and K_p gain elements, the system shown in Figure 2c is a first-order $\Delta\Sigma$ modulator [1]. The K_p gain element has no effect on the behavior of the system because of the hard limiter, and it is easily verified that the K_vT_s gain element does not effect the quantization noise shaping behavior of the

system. Accordingly, the first-order ΔΣFDC modulator loop operates on the frequency modulation of its input signal in the same manner that a first-order ΔΣ modulator operates on the amplitude of its input signal. With the definition that *quantization noise*, $\epsilon(n)$, is the difference between the output and input of the hard limiter at time n, a network analysis shows that the output of the modulator loop is

$$y(n) = \frac{1}{K_v T_s}\widehat{\phi}(n) + e(n),$$

where $e(n) = \epsilon(n) - \epsilon(n-1)$. The sequence $e(n)$ is the error at the output of the modulator loop due to the one-bit quantization performed by the hard limiter and is referred to as *quantization error*. The modulator loop thus subjects the quantization noise to the first-order highpass filter $1 - z^{-1}$. As a result, the quantization error has zero DC power and tends to be weighted toward high frequencies. It follows that the ΔΣFDC performs oversampling A/D conversion on the frequency modulation term $\phi(t)$. The *oversampling ratio* is f_s/f_N, where f_N is the Nyquist rate of $\phi(t)$. Existing ΔΣ modulator results indicate that the precision of the A/D conversion should increase by approximately 1.5 bits [2] for every doubling of the oversampling ratio. This result is supported by computer simulations one of which is presented in Section IV.

Having established the analogy between the first-order ΔΣFDC modulator loop and the first-order ΔΣ modulator, the next logical step is to search for ΔΣFDC modulator loops analogous to higher order ΔΣ modulators. By subjecting the quantization noise to sharper highpass filtering such structures hold the promise of greater conversion accuracy at a given oversampling ratio.

A simple extension of the first-order ΔΣFDC modulator loop leading to a second-order structure is shown in Figure 3. An analysis similar to that performed above for the first-order modulator loop shows that this structure operates on $\widehat{\phi}(n)$ as the single-loop second-order ΔΣ modulator of Figure 4, and subjects the quantization noise to the second-order highpass filter $(1 - z^{-1})^2$. Existing ΔΣ modulator results indicate that the precision of the digital conversion increases by approximately 2.5 bits [2] for every doubling of the oversampling ratio.

Now consider the effect of random channel noise. There are two basic types of performance degradation that can arise from channel noise. The first arises because the channel noise generates a frequency modulation term of its own in $x_r(t)$ that the ΔΣFDC demodulates along with $\phi(t)$. This phenomenon is well known [3] and will not be discussed further since it affects all FM demodulators. The second arises from channel noise that passes to the output of the phase detector.

In the first-order modulator loop, such noise is injected just prior to the sample-and-hold, and is therefore sampled and subjected to the same first-order highpass filter, $1 - z^{-1}$, seen by the quantization noise. Similar observations apply to the second-order modulator loop. Therefore, like quantization error, this type of channel

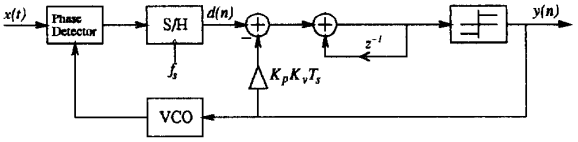

Figure 3: A second order modulator loop.

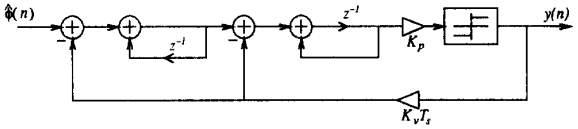

Figure 4: The operation of the second-order modulator loop on the frequency modulation of $x_r(t)$.

noise error will tend to be weighted toward high frequencies. However, the picture is more complicated. If the noise power is sufficiently high, the magnitude of the quantizer input can exceed the hard limiter output by more than half the step size. This phenomenon is known as *quantizer overload* and results in performance degradation similar to that observed in ΔΣ modulators [2]. Moreover, high noise power levels can cause *cycle slipping* wherein the difference between the phase of $x_r(t)$ and the VCO slips by one or more cycles in either direction. Both quantizer overload and cycle slipping can severely degrade performance if their frequency of occurrence is high. Nevertheless, simulations, some of which are discussed below, indicate that the ΔΣFDC is quite robust with respect to channel noise. Further theoretical work will be necessary to quantify this observation

III. Circuit Component Considerations

In each ΔΣFDC, the binary VCO and phase detector are the only RF components in the system. For example, in many applications it would be appropriate to have the RF center frequency in the 1−30GHz range and f_s to be under 100MHz. Aside from these components, the ΔΣFDC circuit considerations are similar to those of ΔΣ modulator-based A/D converters. It is therefore likely that ΔΣFDCs will share many of the robust properties of ΔΣ modulator-based A/D converters with respect to non-ideal circuit behavior. The main issue in establishing the practical viability of the ΔΣFDC technology concerns the effect of non-ideal VCO and phase detector behavior.

A common non-ideality in phase detectors is nonlinearity. Because the phase detector is followed by a hard limiter in the first-order modulator loop, nonlinearities which do not change the sign of the result are completely masked by the one-bit quantization. Since a sinusoidal phase detector will produce a result of the correct sign even in the region where it is highly nonlinear, a conventional RF mixer design will suffice for the phase detector.

Another common non-ideality is the presence of DC offsets. DC offsets can occur in the phase detector, the sample-and-hold, and the hard limiter. When the one-bit quantizer produces the wrong output due to an offset, the incorrect input to the binary VCO will increase the phase error, rather than decreasing it. When the

phase error has increased to the point where the offset is canceled the output will be corrected. The built-up mean phase error will remain and continue to cancel the offset. Provided that the DC offsets are not large enough to overload the quantizer, i.e., the sum of the RF signal's detected frequency modulation and the offset does not exceed the quantizer's range, the ΔΣFDC will thus be self-calibrating for DC offsets.

Noise in the phase detector, the sample-and-hold, and the one-bit quantizer can be mitigated by operating the phase detector with sufficiently high gain K_p that the noise is small with respect to the level of the detected phase signal. The reduction of the no-overload region caused by DC offsets will also be mitigated by such a design. If the input levels are allowed to vary over a wide dynamic range, the gain of mixer-type phase detectors will vary with the input. While the dynamic range of such phase detectors may be set by providing a high-level signal from the VCO, and the one-bit quantizer masks the effect of these gain changes on the phase measurement, the effect of circuit noise will vary as the gain changes. Ultimately the dynamic range of the ΔΣFDC may be determined by the combination of the gain of the phase detector and the hard limiter sensitivity. As a result, in high dynamic range systems, the RF front-end should either employ limiting or automatic gain control to maintain the RF signal power at the phase detector.

The most challenging component of the ΔΣFDC is the binary VCO. Varactor-tuned VCOs typically used in digital tuned oscillators operate at switching rates in excess of 20 MHz; however, thermal effects cause post-tuning drift on the range of 1 MHz in the VCO outputs, over time periods from 1 μsec to 50 μsec [4]. This drift acts as a time-varying gain on the detected frequency modulation, imposing a signal-dependent amplitude modulation on the digitized frequency. As such, conventional varactor-tuned VCOs may be undesirable for some applications.

For applications requiring high digitized frequency accuracy and stability, binary VCOs may be constructed from separate oscillators locked to a common phase and frequency reference. In this configuration, the hard limiter output drives switches to switch between the two oscillators. Microwave GaAs MMIC switches are available with settling times of as little as 2 nsec, allowing f_s up to 500 MHz.

A very important issue relates to the amenability of ΔΣFDCs to VLSI implementation. As mentioned above, aside from the phase detector and VCO, the components that make up the ΔΣFDC are the same as those used in ΔΣ modulator-based A/D converters. As such, many of the VLSI design issues are similar and have been studied extensively [1]. One approach is therefore to integrate all of the ΔΣFDC on a single mixed-mode CMOS VLSI integrated circuit except for the phase detector and VCO which would be implemented separately using high-frequency bipolar or GaAs components. Since a multitude of phase detector and VCO circuits are widely available, well understood, and relatively inexpensive, this is a reasonable approach. On the other hand, integrating the entire ΔΣFDC on a single low-cost mixed-mode VLSI integrated circuit offers the potential of increased reliability and decreased cost. However, because of the analog limitations imposed by fine-line VLSI processes, the phase detector and VCO are likely to be the limiting factors in overall performance.

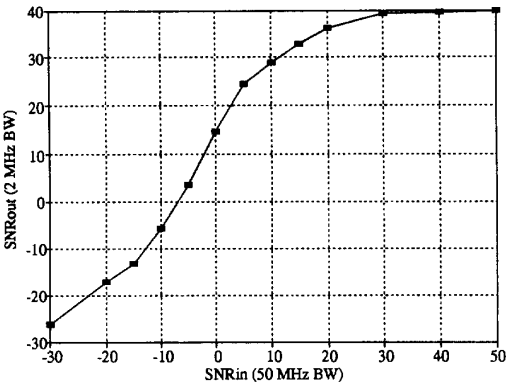

Figure 5: Noise performance of a 25-times oversampling delta-sigma FDC.

III. Simulation Results

Figure 5 shows the detected SNR for a wideband FM signal at various input SNRs. The simulated signal was at a center frequency of 2.1 GHz, and modulated by a 2 MHz sine wave at a peak frequency deviation of 3.5 MHz. The simulated system was sampled at f_s = 100 MHz, for an oversampling ratio of 25. The figure shows classic FM noise behavior with signal suppression at low SNRs and enhancement at high SNRs. For this 25× oversampled system, the ΔΣFDC quantization noise limits the output SNR to approximately 40 dB, in agreement with theoretical results for the first-order ΔΣ modulator [2].

Acknowledgment

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