An ISI Scrambling Technique for Dynamic Element Matching Current-Steering DACs

Jason Remple, Andrea Panigada, and Ian Galton, *Fellow, IEEE*

***Abstract*—The linearity of high-resolution current-steering digital-to-analog converters (DACs) is often limited by inter-symbol interference (ISI). While dynamic element matching (DEM) can be applied to convert a portion of the ISI to uncorrelated noise instead of nonlinear distortion, DEM alone fails to prevent ISI from at least introducing strong second-order nonlinear distortion. This paper addresses this problem by proposing, analyzing, and experimentally demonstrating a low-cost add-on technique, called ISI scrambling, that, in conjunction with DEM, causes a DAC's ISI to be free of nonlinear distortion. The ISI scrambling technique is demonstrated in a 1-GS/s, 14-bit DEM DAC implemented in 90 nm CMOS technology. The DAC's measured linearity is in line with the state of the art and its measured output power spectra closely match those predicted by the paper's theoretical results.**

***Index Terms*— DAC, ISI, DEM, current-steering, non-return-to-zero.**

I. Introduction

INTER-SYMBOL interference (ISI) often limits the linearity of high-resolution current-steering digital-to-analog converters (DACs). It is caused by parasitic memory effects within the DAC's constituent 1-bit DACs, which cause each 1-bit DAC output waveform to depend not only on the 1-bit DAC's current input bit value but also on one or more of its prior input bit values.

Dynamic element matching (DEM) is often applied to multi-bit current-steering DACs to cause error from clock skew and component mismatches to be noise-like waveforms instead of nonlinear distortion [1-9]. It also causes some of the ISI to be a pseudo-random waveform, but even with DEM the ISI contains at least a strong second-order distortion component [10].

The most effective previously-published means of mitigating DAC ISI is to implement the constituent 1-bit DACs as return-to-zero (RZ) 1-bit DACs. RZ 1-bit DACs are reset to a signal-independent state at the end of each clock period. This mitigates ISI because it reduces the dependence of the 1-bit DACs on past input bit values. Unfortunately, the technique's efficacy degrades with clock frequency because of the reduced time available to discharge signal-dependent 1-bit DAC circuit nodes during the reset phase. RZ 1-bit DACs are also significantly more sensitive to clock jitter than their non-return-to-zero (NRZ) counterparts, particularly at high clock frequencies, and they typically consume more than twice the power of comparable NRZ 1-bit DACs.

Other previously published ISI-mitigation techniques measure and then suppress ISI by trimming the delays in the 1-bit DAC switch drivers [11], canceling part of the ISI in either the digital or analog domain [10, 12-14], or dynamically reordering the 1-bit DACs to minimize the ISI [15-16]. The downsides of these techniques are that they require analog-to-digital converter (ADC) based ISI measurement circuitry, their accuracy is limited by that of the measurement circuitry, and they are foreground calibration techniques so they do not track changes in voltage or temperature.

All-digital ISI-mitigation techniques have also been published in which a modified DEM algorithm spectrally shapes the ISI [17-20]. These techniques are useful in oversampling continuous-time delta-sigma data converters. However, as proven in [10], it is not possible for any such technique to suppress nonlinear distortion across the full Nyquist band, so they are not well-suited to wideband applications that utilize the full Nyquist bandwidth of the DAC.

This paper presents a simple, low-cost, add-on technique called ISI scrambling that works in conjunction with DEM to address these problems. By pseudo-randomly scrambling each 1-bit DAC's transient error, the technique converts the ISI error component that would otherwise have been nonlinear distortion into a noise-like waveform that is free of nonlinear distortion. The paper presents a rigorous mathematical analysis of the technique, presents a 90 nm CMOS, 1-GS/s, 14-bit DEM DAC enabled by the technique that achieves linearity in line with the present state of the art, and shows that the measured results closely match the performance predicted by the mathematical analysis. Furthermore, the paper presents the first published experimental demonstration of a key theoretical result presented in [10] in that when the technique is disabled, the ISI nonlinearity manifests primarily as second-order distortion.

II. ISI Scrambling Technique

A conventional DEM DAC consists of a DEM encoder that drives multiple 1-bit DACs, the outputs of which are summed to form the DEM DAC's output [21]. The output of the i^{th} conventional 1-bit DAC is

$$y'_i(t) = \left(c'_i[n_t] - \tfrac{1}{2}\right) K_i \Delta + e'_i(t), \qquad (1)$$

where $c'_i[n]$, which takes on values of 0 and 1, is the 1-bit DAC's binary input sequence, K_i is the 1-bit DAC's weight, Δ is the overall DEM DAC's minimum step-size, $e'_i(t)$ represents the 1-bit DAC's error waveform, $n_t = \lfloor f_s t \rfloor$ is the largest integer

This work was supported by the National Science Foundation under Award 1909678 and Microchip Technology Inc. Jason Remple and Andrea Panigada are with Zeku Inc., San Diego, CA, 92130, USA. Ian Galton is with the Electrical and Computer Engineering Department of the University of California at San Diego, La Jolla, CA 92092-0407, USA.

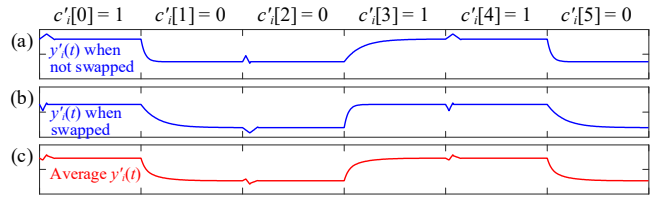

Fig. 1 Example 1-bit DAC outputs with the transient errors: (a) not swapped, (b) swapped, and (c) averaged.

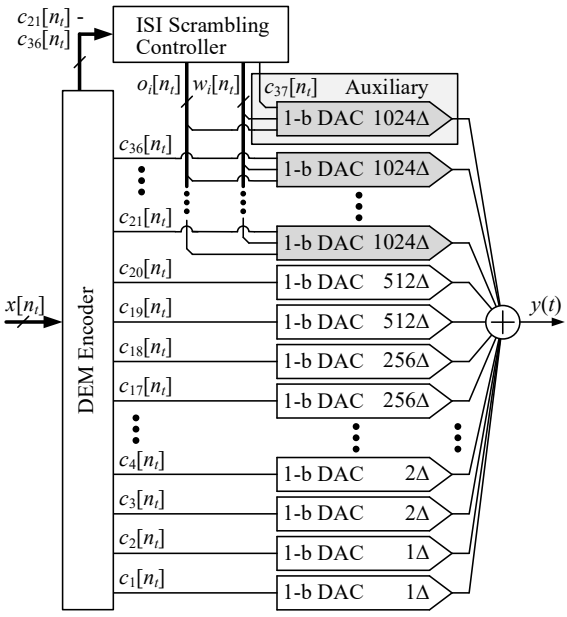

Fig. 2 ISI scrambling DEM DAC block diagram.

less than or equal to $f_s t$, and f_s is the 1-bit DAC's sample rate [10].†

The ISI scrambling technique is a supplement to DEM that converts what would otherwise have been nonlinear ISI error into pseudo-random noise. It incorporates 1-bit DACs that are modified to periodically swap the transient errors that cause nonlinear distortion in conventional 1-bit DACs. Each modified 1-bit DAC, called an ISI scrambling 1-bit DAC in the remainder of the paper, can be configured in real-time to be taken offline and to swap its transient errors.

The idea is to control each of the ISI-scrambling 1-bit DACs such that it spends an equal amount of time with its transient errors swapped and not swapped on average, which causes the average rise and fall transient errors to be symmetric. This is illustrated in Fig. 1. Fig. 1(a) shows an example 1-bit DAC output waveform, Fig. 1(b) shows the corresponding output waveform with its transient errors swapped, and Fig. 1(c) shows the average of the two cases.

Each ISI scrambling 1-bit DAC is taken offline when it transitions from swapping to not swapping its transients, or vice versa. This reduces the disturbance to the overall DAC output caused by inverting the swap state. When an ISI scrambling 1-bit DAC is offline, an auxiliary 1-bit DAC is used temporarily in its place.

A block diagram of the implemented ISI scrambling DEM

† The prime character is used in this paper to denote variables that pertain to conventional 1-bit DACs.

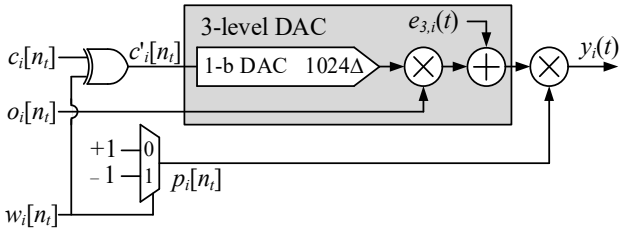

Fig. 3 ISI scrambling 1-bit DAC block diagram.

DAC is shown in Fig. 2. It consists of the digital DEM encoder presented in [4], a digital ISI scrambling controller, 20 conventional 1-bit DACs, and 17 ISI scrambling 1-bit DACs. The ISI scrambling 1-bit DACs are shaded in Fig. 2. The conventional 1-bit DACs have weights 1, 1, 2, 2, 4, 4, … , 512, 512, and the ISI scrambling 1-bit DACs all have a weight of 1024. As proven in Section IV, only the 1024-weight 1-bit DACs contribute nonlinear ISI error to the overall DEM DAC output, so the other 1-bit DACs need not be ISI scrambling 1-bit DACs. The top 1024-weight ISI scrambling 1-bit DAC shown in Fig. 2 is the auxiliary 1-bit DAC. The remaining 1024-weight 1-bit DACs are called the *primary* ISI scrambling 1-bit DACs.

The ISI scrambling controller coordinates taking the primary ISI scrambling 1-bit DACs offline and inverting their swap states. It generates the $o_i[n_t]$ and $w_i[n_t]$ binary sequences that control the online state and the swap state, respectively, of each ISI scrambling 1-bit DAC.‡ The ISI scrambling controller waits a random number of clock cycles between taking randomly-selected individual primary ISI scrambling 1-bit DACs offline. The number of wait cycles is chosen from 1 to N_{Delay} with equal probability where N_{Delay} is a register setting that ranges from 16 to 65536. The purposes of the random wait time are to prevent the ISI errors from being correlated with the input and to avoid introducing periodic disturbances to the overall DEM DAC output that could result in spurs. When selected by the ISI scrambling controller, each primary ISI scrambling 1-bit DAC is taken offline for 8 clock cycles and its swap state is inverted after being offline for 4 clock cycles. The auxiliary 1-bit DAC is offline when it is not taking the place of one of the primary ISI scrambling 1-bit DACs. When the auxiliary 1-bit DAC is offline, the ISI scrambling controller randomly inverts or does not invert its swap state with the objective of ensuring that its rise and fall transient errors are symmetric on average.

A behavioral block diagram of each ISI scrambling 1-bit DAC is shown in Fig. 3. It contains a conventional 1-bit DAC with additional components that implement the ISI-scrambling features. The components within the shaded box together behave as a 3-level DAC with ideal outputs –512Δ, 0, and 512Δ, where the output level of 0 corresponds to the offline state ($o_i[n_t] = 0$). The error, $e_{3,i}(t)$, represents the error of the 3-level DAC. It includes the error of the conventional 1-bit DAC as well as that of the $o_i[n_t]$ multiplier.

The ISI scrambling controller swaps the ISI errors of the conventional 1-bit DAC by setting $w_i[n_t] = 1$, which causes two inversions in the signal path of $c_i[n_t]$. The first inversion is caused

‡ A sequence indexed with n_t is technically a continuous-time function, but is referred to as a sequence because it remains constant over each sample period.

by the XOR gate and the second inversion is caused by the $p_i[n_t]$ multiplier. In the ideal case where $e_{3,i}(t) = 0$ and the multipliers are error-free, $y_i(t)$ is an exact analog representation of $c_i[n_t]$ when the 1-bit DAC is online ($o_i[n_t] = 1$), because the input signal passes through the XOR gate and the multiplier unchanged if swapping is disabled ($w_i[n_t] = 0$), and the two inversions in the signal path cancel each other out if swapping is enabled ($w_i[n_t] = 1$). The error, $e_{3,i}(t)$, only passes through a single inversion when the transients are swapped which allows its polarity in $y_i(t)$ to be controlled by the ISI scrambling controller.

III. Circuit Details

In conventional DEM DACs with NRZ 1-bit DACs, the nonlinear portion of the ISI error primarily consists of second-order and third-order distortion [10, 22]. However, to the extent that the output of each 1-bit DAC is negligibly affected by the states of the other 1-bit DACs, the ISI error consists of just second-order distortion [10]. The ISI scrambling technique mitigates second-order distortion, so the circuit architecture was chosen to separately mitigate third-order distortion by minimizing the extent to which the 1-bit DACs influence each other as described below.

Figure 4 shows the current-steering cell and switch driver that comprise each 1-bit DAC. Transistor M_1 sets the signal-bearing portion of the 1-bit DAC current, so its dimensions are large to facilitate good matching [23]. The dimensions of M_2 are comparatively small to reduce the current source's parasitic output capacitance and thereby reduce ISI [24].

Transistors $M_{k\,a}$ and $M_{k\,b}$ for k = 3, 4, and 5 steer the 1-bit DAC's signal-bearing current to one or the other of its two output terminals or divert it away from both output terminals depending on the states of $c_i[n_t]$ and $o_i[n_t]$ according to the timing diagram shown in Fig. 5. A quad switching technique is used wherein the transistors $M_{k\,a}$ and $M_{k\,b}$ for k = 3, 4, or 5 each conduct the 1-bit DAC's signal-bearing current for half of each clock cycle [25-28]. This improves DAC linearity because, as implied by Fig. 5, exactly one switch turns on and exactly one switch turns off at each clock edge which causes the disturbance to the sources of $M_{k\,a}$ and $M_{k\,b}$ to be largely independent of the 1-bit DAC input [26]. The gate voltages of $M_{k\,a}$ and $M_{k\,b}$ are such that each transistor is in saturation when it conducts current, which increases the 1-bit DAC's output impedance.

Thick oxide transistors M_6 through M_9 implement the 1-bit DAC's transient swapping feature. When the 1-bit DAC is online, i.e., when $o_i[n_t] = 1$, they swap or do not swap the connections between their sources and the two 1-bit DAC outputs depending on $w_i[n_t]$. Toggling $w_i[n_t]$ while the 1-bit DAC is online would result in different transient errors than toggling $c_i[n_t]$ and contribute significant distortion to the DAC output. Hence, $w_i[n_t]$ is only toggled when the 1-bit DAC is offline. Toggling $w_i[n_t]$ when the 1-bit DAC is offline still causes unwanted charge to be injected into the DAC's output terminals, but much of this charge is cancelled because rising and falling transitions of the gate voltages of M_6 and M_9 coincide with falling and rising transitions of the gate voltages of M_7 and M_8, respectively. Furthermore, d and $\overline{d}$ change state at random times so any error from charge injection is independent of the DAC's

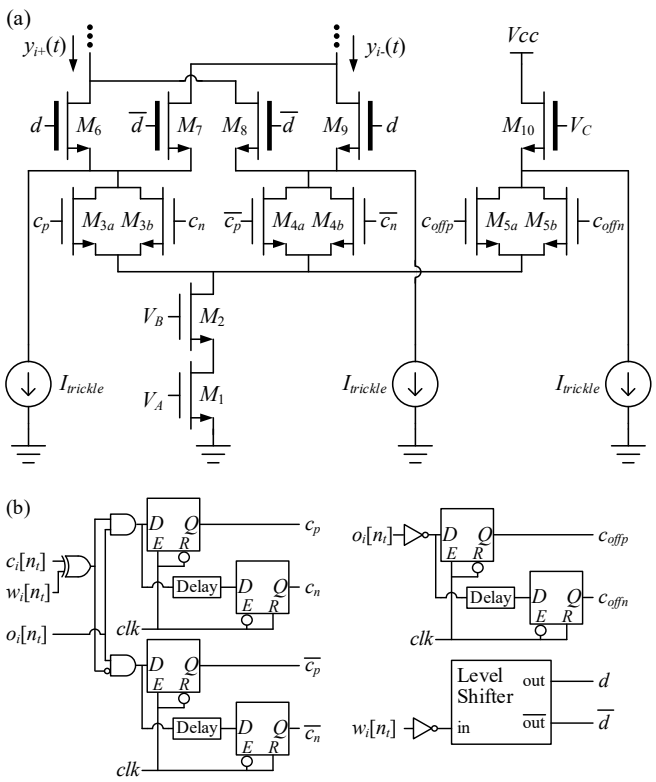

Fig. 4 ISI scrambling 1-bit DAC implementation, (a) current-steering cell, (b) switch driver.

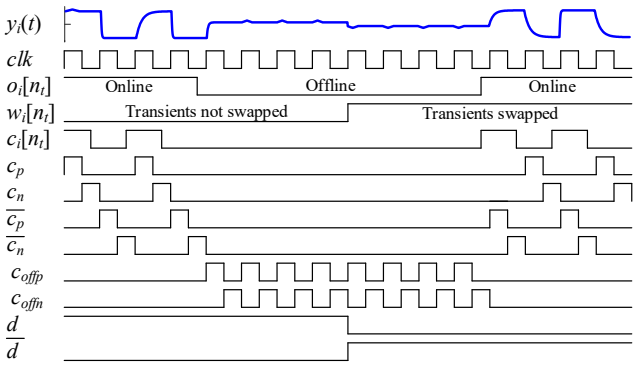

Fig. 5 Switch driver timing diagram.

input code and does not contribute harmonic distortion.

The level-shifter in Fig. 4(b) that drives the gates of M_6 through M_9 is powered by an on-chip LDO similar to that presented in [29], except that an external bypass capacitor is used instead of an internal Miller capacitor. The LDO output voltage is such that when d is high and $\overline{d}$ is low, M_6 and M_9 are in saturation and M_7 and M_8 are off, and when d is low and $\overline{d}$ is high, M_6 and M_9 are off and M_7 and M_8 are in saturation. Keeping M_6 through M_9 in saturation when conducting the 1-bit DAC's signal-bearing current increases the 1-bit DAC's output impedance, thereby reducing the dependence of its transient error on the overall DEM DAC's output [22, 30]. Hence, in addition to implementing the transient swapping feature, M_6 through M_9 perform the function of the cascode stages commonly used in conventional current-steering 1-bit DACs [7, 12-13, 15-16, 22, 27, 31]. As such, they improve overall DEM DAC linearity at the expense of a small reduction in headroom. The $I_{trickle}$ current

sources shown in Fig. 4(a) prevent M_6 through M_{10} from turning off when not conducting the 1-bit DAC's signal-bearing current, thereby reducing nonlinear distortion that would otherwise be caused by code-dependent output capacitance variations [31].

Two versions of the IC were fabricated that differ only in that each 1-bit DAC in the second version includes an extra cascode stage. The second version was fabricated to evaluate the effect of further increasing the 1-bit DAC output impedances. The measured performance of the two versions was found to be indistinguishable, which supports the assumption made in the analysis in Section IV that the error caused by finite 1-bit DAC output impedance is negligible, at least relative to the linearity achieved by the IC as reported in Section V. Hence, this paper presents the details of only the first version of the chip.

The main sources of transient errors that cause nonlinear ISI are the skews between the rising and falling edges of the gate voltages of M_{3a}, M_{3b}, M_{4a}, and M_{4b}, and mismatches among M_{3a}, M_{3b}, M_{4a}, and M_{4b}. The transient swapping feature implemented by M_6 through M_9 swaps these transient errors, but does not swap any additional transient error introduced by mismatches among M_6 through M_9. However, the impedance looking into the sources of M_6 through M_9 is relatively low, so mismatches among M_6 through M_9 do not cause significant transient errors. Monte Carlo simulations support this assertion. With mismatches applied only to M_6 through M_9, they predict a second harmonic of less than −97 dBc for a full-scale sinusoidal input sequence. In contrast, with mismatches applied to all transistors except M_6 through M_9, ISI scrambling disabled, and the same full-scale input sequence, they predict a second harmonic of −72 dBc.

As explained in Section II each 1-bit DAC has a weight K_i = 1, 2, 4, 8, ..., or 1024. The overall DEM DAC's minimum-step size, Δ, is 2.4 μA, so the nominal signal-bearing current sourced by M_1 and M_2 in the K_i = 1 1-bit DAC is 1.2 μA. The current-steering cells in the K_i = 2, 4, and 8 1-bit DACs were implemented by increasing the widths of M_1 and M_2 by factors of 2, 4, and 8, respectively, relative to those in the K_i = 1 1-bit DAC while keeping the dimensions of the other transistors unchanged. The current-steering cells of weights K_i = 16, 32, ..., and 256, were implemented by replicating each transistor in the K_i = 8 current-steering cell 2, 4, 8, ..., and 32 times, respectively, with the replicated transistors connected in parallel. The 1-bit DACs of weight 512 and 1024 were implemented as parallel copies of the K_i = 256 1-bit DAC.

In the current-steering cells of weight K_i = 1, 2, 4, and 8 in which M_6 through M_{10} are each implemented with unit-weight transistors, the nominal value of $I_{trickle}$ is 280 nA. In the current-steering cells of weights K_i = 16, 32, ..., and 256, in which M_6 through M_{10} are each implemented by connecting $2^{-3}K_i$ unit-weight transistors in parallel, the nominal value of $I_{trickle}$ is 3% of the signal-bearing current.

Better matching could have been achieved by implementing each K_i-weight current-steering cell for $K_i \geq 2$ by simply connecting K_i unit-weight current-steering cells in parallel. However, doing so would have significantly increased the required current-steering cell drive strength for $K_i \geq 2$, which would have correspondingly increased the area and current consumption of the switch drivers.

In the absence of other considerations, the best switch driver scaling strategy to match the 1-bit DAC transients is to have the weight of each switch driver be proportional to the weight of the current-steering cell it drives. The switch driver latches are as described in [31], and in TSMC 90 nm technology a minimum-size latch has more drive strength than is required to drive a K_i = 1 current-steering cell. Consequently, if the latches were scaled in proportion to the current-steering cells they would consume far more area and power than necessary. Instead, all current-steering cells are driven by copies of a switch driver that is optimized to drive a K_i = 256 current-steering cell. Dummy transistors are used to load the switch drivers in each 1-bit DAC with a weight of K_i = 128 and lower, so the loads driven by all the switch drivers are approximately equal to the load of a K_i = 256 current-steering cell.

As proven in Section IV, ISI scrambling is not necessary in 1-bit DACs 1-20. Hence, the ISI scrambling feature is disabled in these 1-bit DACs by setting $o_i[n_t]$ and $w_i[n_t]$ to 1 and 0, respectively, for i = 1, 2, …, 20 and all t. Alternatively, the ISI-scrambling circuitry could have been omitted from 1-bit DACs 1-20, but this would have degraded matching.

The clock input buffer is a two-stage differential to single-ended amplifier. The first stage is a differential pair with diode-connected load transistors, and the second stage is a differential pair with a current mirror load. The clock input buffer drives a clock tree that distributes the clock to the 1-bit DACs. The targeted total jitter of the clock input buffer and clock tree is 100 fs RMS, and was verified via simulation. The jitter target ensures that the jitter does not limit the noise performance of the DAC when DEM is enabled.

The placed and routed (P/R) digital block, clock input buffer, bias circuitry, and set of switch drivers are each powered by their own power domain to reduce coupling through the supplies. The power and ground are distributed via wide traces to reduce supply impedance, and extensive on-chip decoupling fills most of the unused area in the chip.

IV. Analysis

This section along with the appendices presents a mathematical derivation that quantifies the behavior of the ISI scrambling technique. It also develops theoretical DAC output PSD expressions that are compared against and closely match the corresponding measured power spectra in Section V. The section and appendices may be skipped without loss of continuity by those who are not interested in the mathematical details.

A. ISI Scrambling 1-Bit DAC Output Model

In conventional current-steering DACs, particularly significant types of errors include mismatches among the 1-bit DACs, transient errors, ISI, and clock feedthrough. For most current-steering DACs, these errors are dominant and $e'_i(t)$ in (1) is well-modeled as

$$e'_i(t) = \begin{cases} e_{11i}(t), & \text{if } c'_i[n_t - 1] = 1,\ c'_i[n_t] = 1, \\ e_{01i}(t), & \text{if } c'_i[n_t - 1] = 0,\ c'_i[n_t] = 1, \\ e_{00i}(t), & \text{if } c'_i[n_t - 1] = 0,\ c'_i[n_t] = 0, \\ e_{10i}(t), & \text{if } c'_i[n_t - 1] = 1,\ c'_i[n_t] = 0, \end{cases} \tag{2}$$

where $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$, are T_s-periodic ($T_s = 1/f_s$) waveforms that correspond to the errors made by the 1-bit DAC for the four possible combinations of the current and previous 1-bit DAC input bit values [10]. During each clock cycle, $e'_i(t)$ is equal to one of the four T_s-periodic error waveforms. Formulating $e'_i(t)$ in terms of these waveforms simplifies the subsequent analysis. It does not impose any restrictions on the 1-bit DAC input sequence, nor does it cause $e'_i(t)$ to be periodic.

As shown in [10], an equivalent form of (1) is

$$\begin{aligned} y'_i(t) = {} & x'_i[n_t]\alpha_i(t)K_i\Delta + \beta_i(t) + x'_i[n_t - 1]\gamma_i(t) \\ & + x'_i[n_t]x'_i[n_t - 1]\eta_i(t), \end{aligned} \tag{3}$$

where

$$x'_i[n_t] = c'_i[n_t] - \tfrac{1}{2}, \tag{4}$$

and $\alpha_i(t)$, $\beta_i(t)$, $\gamma_i(t)$, and $\eta_i(t)$ are linear combinations of $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ so they are T_s-periodic waveforms. The $x'_i[n_t]x'_i[n_t - 1]\eta_i(t)$ term in (3) is a second-order nonlinearly distorted version of the 1-bit DAC's input sequence and is caused by ISI. When the rise and fall transients of the 1-bit DAC output waveform are asymmetric, such as illustrated in Fig. 1(a), $\eta_i(t)$ is nonzero which causes the 1-bit DAC to introduce second-order nonlinear ISI error. Without DEM, this would cause the overall DAC to introduce second-order and several higher-order nonlinear distortion terms, but, as shown in [10], DEM prevents all but second-order nonlinear distortion.

It follows from Fig. 3 that $p_i^2[n_t] = 1$,

$$p_i[n_t] = 1 - 2w_i[n_t], \quad \text{and } c'_i[n_t] = \left(c_i[n_t] - \tfrac{1}{2}\right)p_i[n_t] + \tfrac{1}{2}, \tag{5}$$

so (1) and Fig. 3 imply that

$$y_i(t) = x_i[n_t]o_i[n_t]K_i\Delta + e_i(t), \tag{6}$$

where

$$x_i[n_t] = c_i[n_t] - \tfrac{1}{2}, \tag{7}$$

and $e_i(t)$ represents all error from non-ideal behavior. To the extent that the $p_i[n_t]$ multiplier is ideal, Fig. 3 implies that

$$e_i(t) = p_i[n_t]e_{3,i}(t). \tag{8}$$

Given that $e_{3,i}(t)$ during the nth clock period depends on whether the ISI scrambling 1-bit DAC is offline or online during the nth and $(n-1)$th clock periods, it is convenient for the following analysis to define sequences that are 1 or 0 depending on the four combinations of offline and online statuses during the two clock periods. Specifically, these sequences are defined as

$$o_{++,i}[n_t] = o_i[n_t - 1]o_i[n_t], \tag{9}$$

$$o_{+\times,i}[n_t] = o_i[n_t - 1]\left(1 - o_i[n_t]\right), \tag{10}$$

$$o_{\times+,i}[n_t] = \left(1 - o_i[n_t - 1]\right)o_i[n_t], \tag{11}$$

and

$$o_{\times\times,i}[n_t] = \left(1 - o_i[n_t - 1]\right)\left(1 - o_i[n_t]\right), \tag{12}$$

which have the property that one of $o_{++,i}[n_t]$, $o_{+\times,i}[n_t]$, $o_{\times+,i}[n_t]$, and $o_{\times\times,i}[n_t]$ is 1 and the rest are 0 during each clock cycle.†

† The subscript characters + and × denote "online" and "offline" respectively.

In the error formulation of the conventional 1-bit DAC, a specific T_s-periodic error waveform is defined for each combination of the 1-bit DAC's current and previous input bit values. This results in the $2^2 = 4$ T_s-periodic error waveforms used in (2) to formulate $e'_i(t)$. Applying similar reasoning to the 3-level DAC in the shaded box in Fig. 3 results in $3^2 = 9$ T_s-periodic error waveforms used to formulate

$$\begin{aligned} e_{3,i}(t) = {} & o_{++,i}[n_t]e'_i(t) \\ & + o_{+\times,i}[n_t]\left[c'_i[n_t - 1]e_{1\times i}(t) + \left(1 - c'_i[n_t - 1]\right)e_{0\times i}(t)\right] \\ & + o_{\times+,i}[n_t]\left[c'_i[n_t]e_{\times 1i}(t) + \left(1 - c'_i[n_t]\right)e_{\times 0i}(t)\right] \\ & + o_{\times\times,i}[n_t]e_{\times\times i}(t), \end{aligned} \tag{13}$$

where $e_{1\times i}(t)$, $e_{0\times i}(t)$, $e_{\times 1i}(t)$, $e_{\times 0i}(t)$, and $e_{\times\times i}(t)$ are 5 of the 9 T_s-periodic error waveforms and the remaining 4 T_s-periodic error waveforms are contained in the definition of $e'_i(t)$, which is given by (2).

Thus, $e_i(t)$ is given by (8) with $e_{3,i}(t)$ given by (13) provided the error introduced by the $p_i[n_t]$ multiplier in Fig. 3 is negligible. Otherwise, it is necessary to define two error waveforms, $e_{3,i}^{+}(t)$ and $e_{3,i}^{-}(t)$, that have forms similar to the right side of (13) except that their constituent T_s-periodic error waveforms correspond to the cases of $p_i[n_t] = 1$ and $p_i[n_t] = -1$ respectively. Then, $e_i(t) = e_{3,i}^{+}(t)$ when $p_i[n_t] = 1$ and $e_i(t) = -e_{3,i}^{-}(t)$ when $p_i[n_t] = -1$. In this case ISI scrambling does not completely eliminate ISI-induced second-order nonlinear distortion because $e_{3,i}^{+}(t) \neq e_{3,i}^{-}(t)$. Yet as supported by the experimental results presented in Section V, the error introduced by the $p_i[n_t]$ multiplier in Fig. 3 is indeed negligible. The reason is that the $p_i[n_t]$ multiplier is implemented as a swapper cell as explained in Section III so it only introduces error when $p_i[n_t]$ changes state and this only happens when the 1-bit DAC is offline.

B. ISI Scrambling DEM DAC Output Model

Equations (6)-(13) were formulated to model ISI scrambling 1-bit DACs, but with $o_i[n_t] = 1$ and $w_i[n_t] = 0$ for all t they can also be used to model conventional 1-bit DACs. This is because a conventional 1-bit DAC is equivalent to an ISI scrambling 1-bit DAC that never goes offline and never has its transient errors swapped. Consequently, in the following analysis all the 1-bit DACs in Fig. 2 are modelled via (6)-(13) but with $o_i[n_t] = 1$ and $p_i[n_t] = 1$ for $i = 1, 2, \ldots, 20$ and for all t.

As proven in [4], the DEM encoder's outputs, $c_i[n_t]$, cause the $x_i[n_t]$ sequences, which are given by (7) and take on values that are restricted to ½ and −½, to satisfy

$$x_i[n_t] = \frac{m_i x[n_t] + \lambda_i[n_t]}{\Delta}, \tag{14}$$

where

$$\sum_{i=1}^{36} K_i m_i = 1, \text{ and } \sum_{i=1}^{36} K_i \lambda_i[n_t] = 0. \tag{15}$$

Given that the ISI scrambling technique causes the auxiliary 1-bit DAC to sometimes take the place of one of the primary ISI scrambling 1-bit DACs, (15) implies

$$\sum_{i=1}^{37} K_i m_i o_i[n_t] = 1 \quad \text{and} \quad \sum_{i=1}^{37} K_i \lambda_i[n_t] o_i[n_t] = 0. \tag{16}$$

At the circuit level, the summation operation in Fig. 2 is implemented by connecting the outputs of the current-steering 1-bit DACs. Under the assumption that the impedance of each 1-bit DAC is high enough that its output is negligibly affected by the states of the other 1-bit DACs, an assumption which is supported by the measured results presented in Section V, it follows that the output of the overall DAC is given by

$$y(t) = \sum_{i=1}^{37} y_i(t) \,. \tag{17}$$

Substituting (6) with $e_i(t) = 0$ and (14) into (17), and simplifying the result using (16) results in

$$y(t) = x[n_t] \,, \tag{18}$$

which represents the overall DEM DAC output in the absence of non-ideal behavior. In contrast, as shown in Appendix A, the 1-bit DAC errors cause the overall DAC output to degrade to

$$y(t) = \alpha(t) x[n_t] + \beta(t) + e_{DAC}(t) \,, \tag{19}$$

where $\alpha(t)$ and $\beta(t)$ are T_s-periodic waveforms and $e_{DAC}(t)$ represents the overall DAC's remaining non-ideal performance.

The first term on the right side of (19) is the desired signal component of the DAC output. As shown in [10], its continuous-time Fourier transform (CTFT) is

$$\Im_{CT}\left\{\alpha(t) x[n_t]\right\} = A_p\left(j\omega\right) X\left(e^{j\omega T_s}\right), \tag{20}$$

where $A_p(j\omega)$ is the CTFT of

$$\alpha_p(t) = \begin{cases} \alpha(t) & \text{if } 0 \le t < T_s, \\ 0 & \text{otherwise,} \end{cases} \tag{21}$$

and $X(e^{j\omega Ts})$ is the discrete-time Fourier transform (DTFT) of $x[n]$. Ideally, $\alpha(t) = 1$ in which case the $\alpha(t)x[n_t]$ term in (19) reduces to the right side of (18), and (20)-(21) imply that $|A_p(j\omega)| = \sin(\pi T_s f\,)/\pi f$. This corresponds to the classic zero-order-hold frequency response roll-off of an ideal DAC. In practice, 1-bit DAC errors cause $\alpha(t)$ to deviate from unity, but, as implied by (20) and (21), this just affects the frequency response roll-off without introducing nonlinear distortion. Moreover, the effect on the frequency roll-off typically is not significant in current steering DACs [10].

The $\beta(t)$ term in (19) introduces fixed tones in the DAC output at integer multiples of f_s. Such tones occur in all types of DACs, e.g., as a result of clock feedthrough. They do not fall within any Nyquist band of the DAC output and do not depend on the DAC input, so they do not cause problems in typical DAC applications [10].

In contrast, the $e_{DAC}(t)$ term in (19) limits performance in typical applications. As proven in Appendix A it can be written as

$$e_{DAC}(t) = e_{MM}(t) + e_{ISI-linear}(t) + e_{ISI-noise}(t) \,, \tag{22}$$

where $e_{MM}(t)$ is caused by mismatches among the 1-bit DACs and the remaining two terms are caused by ISI.

The expression for $e_{MM}(t)$ is

$$e_{MM}(t) = \frac{1}{\Delta} \sum_{i=1}^{37} o_{++,i}[n_t] \lambda_i[n_t] \varepsilon_i(t) \,, \tag{23}$$

where each $\varepsilon_i(t)$ is a T_s-periodic waveform defined in Appendix A and DEM causes the $\lambda_i[n_t]$ sequences to be zero-mean, pseudo-random sequences that are uncorrelated with the DAC's input sequence, $x[n_t]$, i.e.

$$\left.\begin{aligned} &\mathrm{E}\{\lambda_i[n_t]\} = 0 \\ &\mathrm{E}\{\lambda_i[n_t]\lambda_i[m_t]\} = 0 \text{ for } m_t \ne n_t \end{aligned}\right\} \text{ regardless of } x[n_t] \,, \tag{24}$$

where $\mathrm{E}\{u\}$ denotes the expected value of u [4]. Without DEM the $\lambda_i[n_t]$ sequences would be nonlinearly related to the DAC input, so $e_{MM}(t)$ would contain nonlinear distortion. With DEM $e_{MM}(t)$ is a zero-mean pseudo-random noise waveform because of the behavior of the $\lambda_i[n_t]$ sequences [10].

The expression for $e_{ISI\text{-}linear}(t)$ is

$$e_{ISI-linear}(t) = x[n_t - 1]\gamma(t) \,, \tag{25}$$

where $\gamma(t)$ is a T_s-periodic waveform defined in Appendix A. The 1-bit DAC errors cause $\gamma(t)$, and hence $e_{ISI\text{-}linear}(t)$, to deviate from 0, but the argument applied above to show that the $\alpha(t)x[n_t]$ term in (19) does not introduce nonlinear distortion also applies to $e_{ISI\text{-}linear}(t)$. While the 1-bit DAC errors cause $\alpha(t)$ to deviate slightly from its ideal value of $\alpha(t) = 1$, they cause $\gamma(t)$ to deviate slightly from its ideal value of $\gamma(t) = 0$, so in addition to not introducing nonlinear distortion, $e_{ISI\text{-}linear}(t)$ typically has much lower power than $\alpha(t)x[n_t]$.

The expression for $e_{ISI\text{-}noise}(t)$ is

$$e_{ISI-noise}(t) = e_{DEM}(t) + e_{IS}(t) \,, \tag{26}$$

where $e_{DEM}(t)$ and $e_{IS}(t)$ are error waveforms resulting from ISI that comprise noise instead of nonlinear distortion because of DEM and ISI scrambling, respectively. The expression for $e_{DEM}(t)$ is

$$\begin{aligned} e_{DEM}(t) = {} & \frac{1}{\Delta} \sum_{i=1}^{37} \lambda_i[n_t - 1]\left[o_{++,i}[n_t]\gamma_i(t) + z_i[n_t]\lambda_i[n_t]\right] \\ & + \frac{1}{\Delta} \sum_{i=21}^{37} \Big(o_{+\times,i}[n_t]\gamma_{+\times,i}(t)\lambda_i[n_t - 1] \\ & \qquad + \Delta \cdot o_{\times+,i}[n_t]\varepsilon_{\times+,i}(t)\lambda_i[n_t] \\ & \qquad + 2^{-14} \cdot z_i[n_t]\left[x[n_t - 1]\lambda_i[n_t] + x[n_t]\lambda_i[n_t - 1]\right]\Big), \end{aligned} \tag{27}$$

where $\varepsilon_{\times+,i}(t)$ and $\gamma_{+\times,i}(t)$ are defined in Appendix A, and $z_i[n_t] = o_{++,i}[n_t]p_i[n_t]\eta_i(t)/\Delta$. Every term on the right side of (27) contains one or both of $\lambda_i[n_t]$ and $\lambda_i[n_t - 1]$, so, as in the case of $e_{MM}(t)$, DEM causes $e_{DEM}(t)$ to comprise zero-mean pseudo-random noise instead of nonlinear distortion.

The expression for $e_{IS}(t)$ is

$$\begin{aligned} e_{IS}(t) = \sum_{i=21}^{37} \Big(& e_i(t) + p_i[n_t]\Big[o_{++,i}[n_t]\beta_i(t) + o_{+\times,i}[n_t]\beta_{+\times,i}(t) \\ & \qquad + o_{\times+,i}[n_t]\beta_{\times+,i}(t) + o_{\times\times,i}[n_t]e_{\times\times i}(t)\Big] \\ & + 2^{-14} x[n_t]\left[\tilde{o}_{++,i}[n_t]\varepsilon_i(t) + \tilde{o}_{\times+,i}[n_t]\varepsilon_{\times+,i}(t)\right] \\ & + 2^{-14}\Delta^{-1} x[n_t - 1]\left[\tilde{o}_{++,i}[n_t]\gamma_i(t) + \tilde{o}_{+\times,i}[n_t]\gamma_{+\times,i}(t)\right]\Big), \end{aligned} \tag{28}$$

where

$$e_i(t) = \frac{1}{2^{28}\Delta^2} q_i[n_t] x[n_t] x[n_t - 1]\eta_i(t) \,, \tag{29}$$

$$q_i[n_t] = o_{++,i}[n_t] p_i[n_t] \,, \tag{30}$$

and the factors in (28) that are not defined above are defined in Appendix A. To show that $e_{IS}(t)$ does not introduce nonlinear distortion, it is sufficient to show that

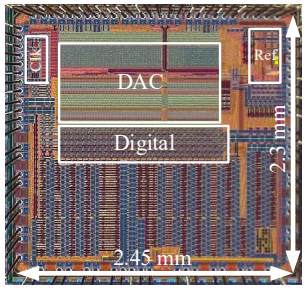

Fig. 6 Die photograph.

$$\mathrm{E}\left\{e_{IS}(t)\,f\left(x[n_t], x[n_t-1], x[n_t-2], \ldots\right)\right\} = 0 \qquad (31)$$

holds for every deterministic nonlinear function of the DEM DAC's input sequence, $f(x[n_t], x[n_t - 1], x[n_t - 2], \ldots)$. Given that $x[n_t]$ is deterministic, it follows from (31) that it is sufficient to show

$$\mathrm{E}\left\{e_{IS}(t)\right\} = 0 \;\text{ regardless of } x[n_t] \text{ for all } t\,. \qquad (32)$$

Every term on the right side of (28) contains either $p_i[n_t]$, $\tilde{o}_{++,i}[n_t]$, $\tilde{o}_{+\times,i}[n_t]$, or $\tilde{o}_{\times+,i}[n_t]$, all of which, by definition, are zero-mean random sequences that are independent of $x[n_t]$ for all t. In addition, $p_i[n_t]$ is independent of the other stochastic sequences in (28), and so it follows from (28) that (32) holds.

If ISI scrambling were not enabled, $p_i[n_t] = 1$ and $o_{++,i}[n_t] = 1$ for all t, which would cause the $e_i(t)$ terms in (28) to contribute second-order nonlinear distortion. In contrast, the other terms in (28) as well as those in (23) and (27) either have zero means regardless of $x[n_t]$ or have no dependence on $x[n_t]$, so they do not contribute nonlinear distortion in either the absence or presence of ISI scrambling.

As shown in [4], $m_i = 0$ for $i = 1, 2, \ldots, 20$, so (14) and (7) imply that the $c_i[n_t]$ outputs of the DEM encoder for these values of i do not contain components proportional to $x[n_t]$. This is why the summation in (28) starts from $i = 21$, and why the bottom 20 1-bit DACs in Fig. 2 need not be ISI scrambling 1-bit DACs.

To show that $e_{IS}(t)$ does not introduce spurious tones, it is sufficient to show that

$$\lim_{\tau\to\infty} \mathrm{E}\left\{e_{IS}(t)e_{IS}(t+\tau)\right\} = 0 \quad \text{regardless of } x[n_t] \text{ for all } t. \quad (33)$$

By definition, $x[n_t]$ is deterministic, and, for sufficiently large τ and any i and j, $o_i[n_t]$, $o_j[n_{t+\tau}]$, $p_i[n_t]$, and $p_j[n_{t+\tau}]$ are independent, and $p_i[n_t]$ and $p_j[n_{t+\tau}]$ are zero mean. As explained in Appendix A, $\tilde{o}_{**,i}[n]$ is the zero-mean portion of $o_{**,i}[n]$ where $**$ is a placeholder for $++$, $+\times$, $\times+$, or $\times\times$. Therefore, (9)-(12) imply that $\tilde{o}_{ab,i}[n_t]$, $\tilde{o}_{cd,j}[n_{t+\tau}]$, $p_i[n_t]$, and $p_j[n_{t+\tau}]$ are independent for sufficiently large τ and any i and j, where a, b, c, and d are any combination of + and ×. Expanding $\mathrm{E}\{e_{IS}(t)e_{IS}(t+\tau)\}$ using (28) and applying the above observations, verifies that (33) holds.

C. *Effect of ISI Scrambling for Sinusoidal Inputs*

As explained above, the $e_i(t)$ terms in (28) would contribute nonlinear distortion if it were not for ISI scrambling, so the properties of these terms are of particular interest. The power spectral density (PSD) of $e_i(t)$ is derived in Appendices B and C for a full-scale input signal, $x[n_t] = 8192\Delta\sin(2\pi n_t f_0/f_s)$, where f_0/f_s satisfies

$$0 < f_0/f_s < \tfrac{1}{2} \quad \text{and} \quad f_0/f_s \neq \tfrac{1}{4}\,, \qquad (34)$$

to avoid the degenerate cases of either the fundamental or the second harmonic of the input signal aliasing to zero frequency in $x[n_t]$.

The derivation involves two key components. Appendix B proves that the $q_i[n_t]$ factor of $e_i(t)$ with n_t replaced by n is a wide-sense stationary (WSS) discrete-time random process, and derives an expression for its autocorrelation, $R_{q,i}[k]$. Appendix C applies this result to show that $e_i(t)$ is a cyclo-stationary continuous-time random process, and derives expressions for its time-average autocorrelation, $\bar{R}_{e,i}(\tau)$, and PSD, $S_{e,i}(j\omega)$.

Given that each $e_i(t)$ term in (28) is proportional to $p_j[n_t]$ if and only if $j = i$, and, by definition, $p_i[n]$ is independent of $p_j[n]$ when $i \neq j$, it follows that $e_i(t)$ and $e_j(t)$ are independent when $i \neq j$. Consequently, the PSD of the portion of $e_{DAC}(t)$ that would be nonlinear distortion if ISI scrambling were not applied is

$$S_{e_{IS}}(j\omega) = \sum_{i=21}^{37} S_{e,i}(j\omega)\,. \qquad (35)$$

Theoretical curves calculated from (35) and its supporting equations in Appendices B and C are shown in Section V to closely match measurement results. The theoretical results prove and the measured results demonstrate that the ISI scrambling technique converts what would otherwise be ISI-induced second-order harmonic distortion spurs to noise "bumps" centered at the spur frequencies, e.g., at frequencies of 0 and $2f_0$ Hz in the DAC's first Nyquist band. The peak amplitudes of the noise bump PSDs decrease as the average ISI scrambling 1-bit DAC transient swapping rate is increased. Hence, they decrease as N_{Delay} is decreased.

V. Measurement Results

The IC was implemented in a TSMC 90 nm process. A die photograph of it is shown in Fig. 6. The die measures 2.3 mm × 2.45 mm and its active area is 1.48 mm^2. The incremental circuit area required to implement ISI scrambling is 0.08 mm^2 of which 0.03 mm^2 corresponds to digital logic. The IC was tested in a QFN64 package and all grounds were down-bonded to the package's ground paddle. In addition to the DAC core, the IC contains LVDS interface circuitry interspersed throughout the pad ring and a direct digital synthesizer (DDS) integrated in the P/R digital block. The DDS was used for all measurements presented in this section.

The packaged IC was mounted to a test circuit board with an Ironwood elastomer socket. The clock signal applied to the test circuit board was generated by passing the single-ended output of a low-jitter laboratory signal generator through a passive bandpass filter to suppress noise and spurious tones. A balun and associated passive matching circuitry on the test circuit board converts the clock signal to differential form prior to the IC. A transformer and associated passive matching circuitry on the test circuit board converts the differential DAC output to a single-ended signal that was measured via a laboratory signal analyzer to obtain the results presented in this section.

Fig. 7 shows representative DAC output power spectra for a 481.4 MHz single-tone input sequence. Compared to the case with both DEM and ISI scrambling disabled, the results indicate

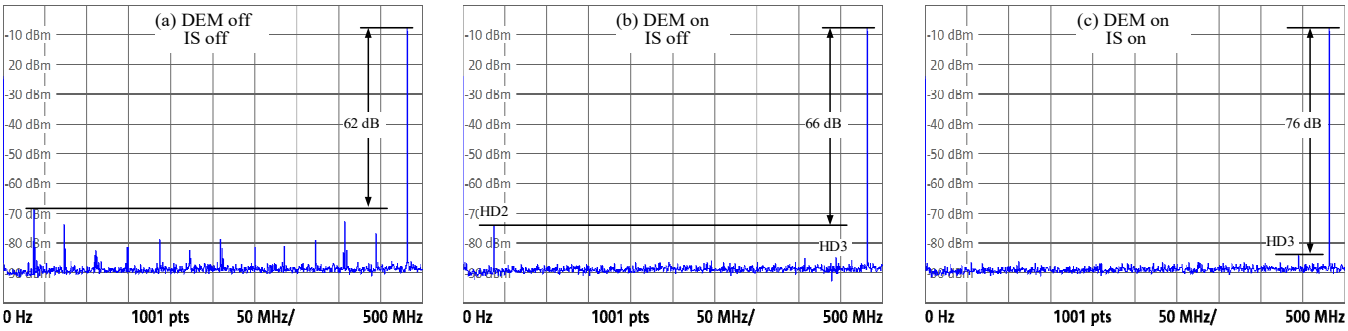

Fig. 7 Measured output power spectra for a full-scale 481.4 MHz input signal.

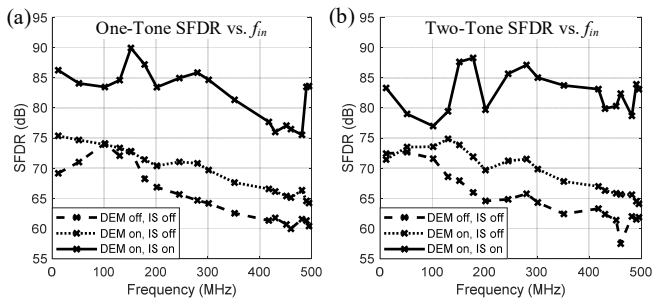

Fig. 8 Measured SFDR vs. frequency (a) one-tone input signals, and (b) two-tones input signals separated by 3.52 MHz.

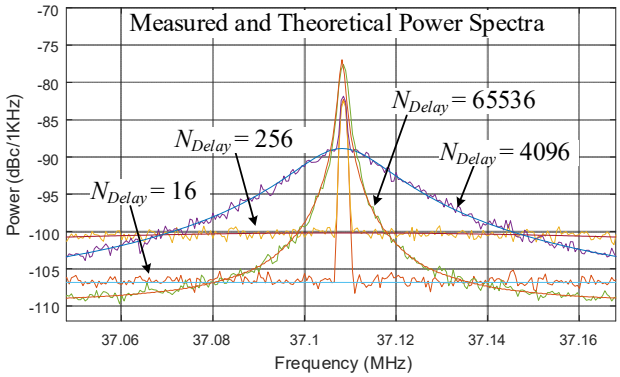

Fig. 9 Measured and theoretical power spectra around aliased second harmonic for full-scale 481.4 MHz single-tone input signal.

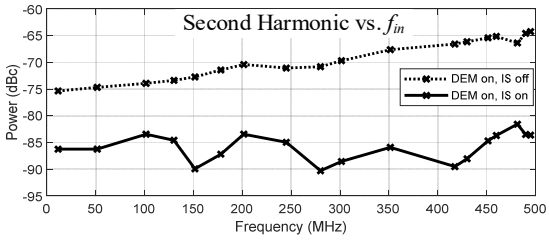

Fig. 10 Measured second harmonic versus frequency for a full-scale single-tone input signal.

that enabling just DEM improves the spurious-free dynamic range (SFDR) by only 4 dB whereas enabling both DEM and ISI scrambling improves the SFDR by 14 dB. With DEM enabled and ISI scrambling disabled, the measured SFDR is limited by an aliased second harmonic caused by ISI as predicted by the corresponding theoretical result presented in [10]. As predicted by the theoretical results presented in this paper, the measured second harmonic is highly attenuated when both DEM and ISI scrambling are enabled.

Similar results also hold for other input signals. Fig. 8 shows measured SFDR values versus signal frequency for single-tone and two-tone DAC input sequences. The data demonstrate that ISI scrambling significantly increases the measured SFDR values relative to the cases where ISI scrambling is disabled.

Fig. 9 shows several measured and theoretically calculated power spectra corresponding to a 481.4 MHz single-tone DAC input sequence with DEM and ISI scrambling enabled. To demonstrate the correspondence between theory and measurement, the power spectra are shown over a zoomed-in frequency band centered on the frequency at which the limiting aliased second harmonic occurs in the absence of ISI scrambling. A pair of power spectra, one measured and one calculated, are superimposed for each of N_{Delay} = 16, 256, 4096, and 65536. The calculated power spectra were obtained via the equations derived in Section IV and the appendices with a noise floor added to match that of the measured power spectra, $\alpha(t)$ approximated as unity (its ideal value), and each $\eta_i(t)$ approximated as a constant taken to be that which yielded the best overall match between the calculated and measured power spectra.

As predicted by the analysis in Section IV and demonstrated in Fig. 9, ISI scrambling converts what would otherwise be second-order nonlinear distortion into a spectral noise "bump" and the height of the bump decreases with N_{Delay}. Except for a −82 dBc residual second-order spur in the measured results, the measured and corresponding calculated power spectra shown in Fig. 9, are in very close agreement.

The authors believe that the residual second-order spur is the result of differential path mismatches from transistors M_6 through M_9 in Fig. 4(a) through the test circuit board's output network up to the transformer. Evidence in support of this belief is that the residual spur was not predicted by simulations in the absence of such mismatches, and it was found to vary somewhat across different copies of the IC and test circuit board.

With DEM and ISI scrambling enabled, the DAC's SFDR for input frequencies above 300 MHz is limited by higher third-order distortion than was predicted by simulations prior to IC fabrication. The authors subsequently realized they had made a mistake in the simulation setup which caused the impedance of the ground bond wires to be underestimated. The measured third-order distortion was reproduced in simulation when the mistake was corrected. Nearly identical third order distortion was observed in simulation when ISI scrambling was disabled and M_7 and M_8 in Fig. 4(a) were removed, which shows that ISI scrambling is not the cause of the third-order distortion. If the

TABLE I
NSD/SNDR MEASURED OVER FIRST NYQUIST BAND

	NSD (dBc/Hz)			SNDR (dB)		
f_{in} (MHz)	DEM off IS off	DEM on IS off	DEM on IS on	DEM off IS off	DEM on IS off	DEM on IS on
51	–163.4	–147.1	–146.3	63.6	59.9	59.4
180	–158.1	–145.8	–145.2	62.4	58.6	58.3
481	–150.8	–144.8	–144.8	60.3	57.8	57.8

TABLE II
KEY SPECIFICATIONS OF RECENT STATE-OF-THE-ART DACS

	Process (nm)	Resolution (bits)	Sample Rate (GHz)	Full Scale (mA)	Power (mW)	Technique
This Work	90	14	1000	20	238*	DEM / IS
[5]	40	16	1600	16/20	40	DEMDRZ
[7]	16	16	6000	40	350	Static Cal
[8]	22	14	600	16	202	MNC
[9]	28	14	10000	16	162	OIC
[13]	65	16	9000	16	1080	DPD
[15]	140	14	200	20	270	DMM
[16]	65	16	3200	20	240	3DSC
[30]	90	12	1250	16	128	DRRZ

*1.2 mW is due to ISI scrambling

problem caused by the DAC ground impedance were fixed, simulations suggest that the third-order distortion would be limited by the 1-bit DAC output impedance [22, 30-32].

Fig. 10 shows the effect of ISI scrambling on the second-harmonic for full-scale single tone input sequences. With DEM enabled and ISI scrambling disabled, the ratio of the power of the desired signal component to the power of the second-harmonic decreases with input frequency. In contrast, with both DEM and ISI scrambling enabled, the ratio of the two components does not increase with frequency.

These observations are predicted by the analysis presented in Section IV. The CTFT of the DAC's desired signal component given by (20) is proportional to $A_p(j\omega)$, which is the CTFT of the T_s-duration pulse, $\alpha_p(t)$, equal to one period of $\alpha(t)$. The second-order distortion caused by ISI is represented by the $e_i(t)$ terms in (28). By the same reasoning that led to (20), the CTFT of $e_i(t)$ is proportional to $H_{p,i}(j\omega)$, which is the CTFT of a T_s-duration pulse, $\eta_{p,i}(t)$, equal to one period of $\eta_i(t)$. While $\alpha_p(t)$ is approximately constant for most of $0 \le t < T_s$, $\eta_{p,i}(t)$ is the result of 1-bit DAC transient errors so it is non-zero mainly over a short interval close to $t = 0$. Consequently, $|H_{p,i}(j\omega)|$ decreases less over the first Nyquist band than $|A_p(j\omega)|$ such that the second-order distortion exhibits less frequency roll-off than the desired signal component. In contrast, the residual second-order distortion term that remains when ISI-scrambling is enabled is not caused by ISI, so it does not appear in $e_i(t)$ and is not subject to this effect.

Five randomly-selected copies of the IC were tested. For full-scale single-tone input sequences with frequencies spanning the Nyquist band, the worst measured second harmonic of the five copies is –64 dBc with DEM enabled and ISI scrambling disabled and –78 dBc with both DEM and ISI scrambling enabled. The power spectra and SFDR measurements presented in this section are from the IC copy with the worst second-order distortion when ISI scrambling is disabled.

The full-scale single-tone noise performance of the IC is shown in Table I. Enabling DEM reduces the SNDR by about 3 dB, which is expected; DEM increases the number of 1-bit DAC transitions and causes the 1-bit DAC rise and fall transition mismatches to increase the overall DEM DAC's output noise. The same degradation in SNDR was observed in simulation when DEM was enabled. In contrast, the RZ 1-bit DACs used in [4, 8] have the same number of output transitions regardless of whether DEM is enabled, so enabling DEM does not degrade the SNDR for full-scale input signals in those cases. Enabling ISI scrambling in addition to DEM reduces the SNDR by up to 0.5 dB, which shows that the noise caused by DEM dominates the noise floor. As expected, the noise performance of the IC is worse than those of DACs that incorporate 1-bit DAC mismatch error calibration [7-8, 13, 15-16, 34]. However, the ISI scrambling technique's low circuit area and power consumption makes it inexpensive to combine with previously published techniques that calibrate 1-bit DAC mismatch errors.

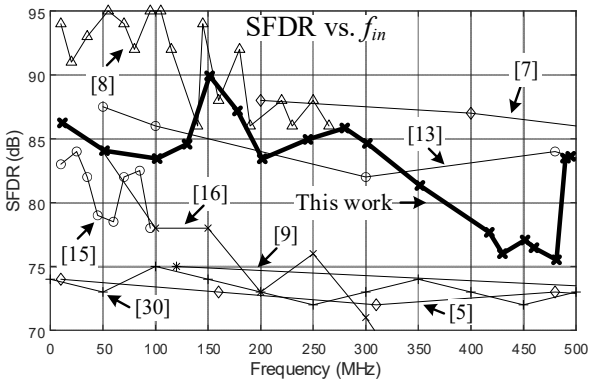

Fig. 11 SFDR comparison of recent state-of-the-art DACs.

Table II and Fig. 11 present key specifications of the IC along with those of several other published state-of-the-art DACs. The P/R digital block includes the DEM encoder, ISI scrambling controller and DDS, and consumes 105 mW from a 1.2 V supply. The analog circuitry consumes the remaining 133 mW from 1.2 V and 3.3 V supplies (the DAC output current is sourced from the 3.3 V supply). The data show that the IC exhibits better SFDR performance than all but the DACs presented in [7], [8], and [13]. The DAC presented in [13] achieves high linearity, but it requires manual laboratory measurements to iteratively configure its foreground calibration technique which limits its applicability. The DAC presented in [8] uses RZ 1-bit DACs to avoid being limited by nonlinear ISI (measurements show that its SFDR drops by 10 dB when its 1-bit DACs are operated in NRZ mode). Had the DAC presented in [8] been augmented with ISI scrambling, it is likely that it could have used NRZ 1-bit DACs and thereby avoided the downsides of RZ 1-bit DACs without sacrificing linearity. The DAC presented in [7] uses NRZ 1-bit DACs and no ISI-mitigation techniques are mentioned in [7]. This suggests that excellent design and layout practices as well as the advanced 16 nm CMOS IC technology in which it is implemented are likely responsible for keeping its nonlinear ISI in check. Yet the analysis in Section IV shows that its NRZ 1-bit DACs must be introducing significant nonlinear ISI, so it is reasonable to expect that it too could have benefited from ISI scrambling.

VI. Appendix A

Substituting (7) into the right-most equation in (5) and substituting the result into (13) yields

$$\begin{aligned} e_{3,i}(t) &= o_{++,i}[n_t]e'_i(t) \\ &+o_{+\times,i}[n_t]\left[\beta_{+\times,i}(t)+x_i[n_t-1]p_i[n_t-1]\gamma_{+\times,i}(t)\right] \\ &+o_{\times+,i}[n_t]\left[\beta_{\times+,i}(t)+x_i[n_t]p_i[n_t]\varepsilon_{\times+,i}(t)\Delta\right] \\ &+o_{\times\times,i}[n_t]e_{\times\times i}(t), \end{aligned} \tag{36}$$

where

$$\beta_{+\times,i}(t)=\frac{1}{2}\left[e_{1\times i}(t)+e_{0\times i}(t)\right],\quad \beta_{\times+,i}(t)=\frac{1}{2}\left[e_{\times 1i}(t)+e_{\times 0i}(t)\right], \tag{37}$$

$$\gamma_{+\times,i}(t)=e_{1\times i}(t)-e_{0\times i}(t),\ \text{and}\ \varepsilon_{\times+,i}(t)=\frac{1}{\Delta}\left[e_{\times 1i}(t)-e_{\times 0i}(t)\right]. \tag{38}$$

As explained in Section II, $p_i[n_t]$ only changes when the ISI scrambling 1-bit DAC has been offline for multiple clock cycles. This implies that $p_i[n_t] = p_i[n_t-1]$ whenever $o_{\times\times,i}[n] = 0$. In such cases, both $p_i[n_t]p_i[n_t-1] = 1$ and $p_i^2[n_t] = 1$, because $p_i[n_t]$ takes on values of only 1 and −1. Consequently, (36) implies

$$\begin{aligned} p_i[n_t]e_{3,i}(t) &= o_{++,i}[n_t]p_i[n_t]e'_i(t) \\ &+o_{+\times,i}[n_t]\left[p_i[n_t]\beta_{+\times,i}(t)+x_i[n_t-1]\gamma_{+\times,i}(t)\right] \\ &+o_{\times+,i}[n_t]\left[p_i[n_t]\beta_{\times+,i}(t)+x_i[n_t]\varepsilon_{\times+,i}(t)\Delta\right] \\ &+o_{\times\times,i}[n_t]p_i[n_t]e_{\times\times i}(t). \end{aligned} \tag{39}$$

As explained in Section IV-A, $o_{+\times,i}[n_t] = o_{\times+,i}[n_t] = o_{\times\times,i}[n_t] = 0$ when $o_{++,i}[n_t] = 1$. Thus, (6), (8), and (39) imply that the output of the ith ISI scrambling 1-bit DAC is

$$y_i(t)=x_i[n_t]K_i\Delta+p_i[n_t]e'_i(t), \tag{40}$$

when $o_{++,i}[n_t] = 1$. Performing an analysis nearly identical to that applied in [10] to derive (3) from (1) and (2), and applying $p_i[n_t]p_i[n_t-1] = 1$ and $p_i^2[n_t] = 1$ results in

$$y_i(t)=x_i[n_t]\alpha_i(t)K_i\Delta+e_{++,i}(t), \tag{41}$$

when $o_{++,i}[n_t] = 1$, where

$$\begin{aligned} e_{++,i}(t) &= p_i[n_t]\beta_i(t)+x_i[n_t-1]\gamma_i(t) \\ &+p_i[n_t]x_i[n_t]x_i[n_t-1]\eta_i(t). \end{aligned} \tag{42}$$

Given that one of $o_{++,i}[n_t]$, $o_{+\times,i}[n_t]$, $o_{\times+,i}[n_t]$, and $o_{\times\times,i}[n_t]$ is 1 and the rest are 0 during each clock cycle and $o_i[n_t] = 1$ when $o_{++,i}[n_t] = 1$, it follows from (6), (8), (39), and (41) that

$$\begin{aligned} y_i(t) &= x_i[n_t]o_i[n_t]K_i\Delta \\ &+o_{++,i}[n_t]\left[x_i[n_t]\varepsilon_i(t)\Delta+e_{++,i}(t)\right] \\ &+o_{+\times,i}[n_t]\left[p_i[n_t]\beta_{+\times,i}(t)+x_i[n_t-1]\gamma_{+\times,i}(t)\right] \\ &+o_{\times+,i}[n_t]\left[p_i[n_t]\beta_{\times+,i}(t)+x_i[n_t]\varepsilon_{\times+,i}(t)\Delta\right] \\ &+o_{\times\times,i}[n_t]p_i[n_t]e_{\times\times i}(t), \end{aligned} \tag{43}$$

where

$$\varepsilon_i(t)=K_i(\alpha_i(t)-1). \tag{44}$$

The random sequences $o_{++,i}[n_t]$, $o_{+\times,i}[n_t]$, $o_{\times+,i}[n_t]$, and $o_{\times\times,i}[n_t]$ can each be written as

$$o_{**,i}[n]=\tilde{o}_{**,i}[n]+\overline{o}_{**,i}, \tag{45}$$

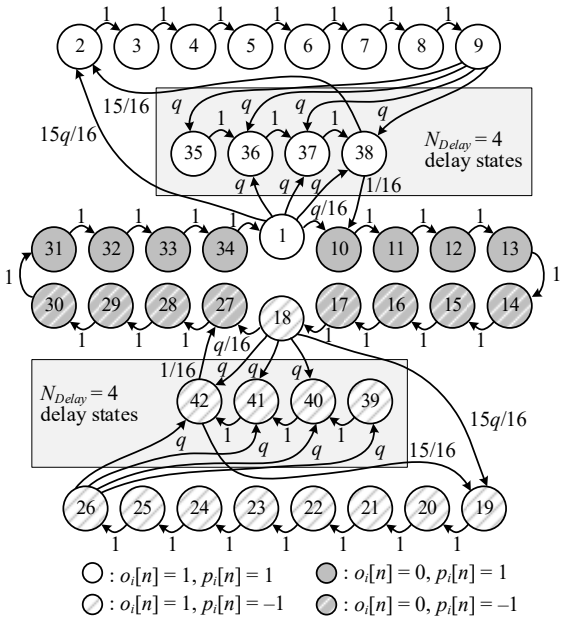

Fig. 12 Markov state transition diagram corresponding to the primary ISI scrambling 1-bit DACs.

where ** is a placeholder for ++, +×, ×+, or ××, $\tilde{o}_{**,i}[n]$ is the zero-mean portion of $o_{**,i}[n]$, and $\overline{o}_{**,i}$ is the mean of $o_{**,i}[n]$.

The DEM encoder causes $m_i = 0$ for $1 \le i \le 20$ and $m_i = 2^{-14}$ for $21 \le i \le 36$ [4]. Therefore, substituting (43) with (45) and (14) into (17), simplifying the result with (16), and applying $o_i[n_t] = 1$ for all i = 1, 2, …, 20 results in (19), (22), (23), and (25)-(28), where

$$\alpha(t)=1+2^{-14}\sum_{i=21}^{37}\left(\overline{o}_{++,i}\varepsilon_i(t)+\overline{o}_{\times+,i}\varepsilon_{\times+,i}(t)\right), \tag{46}$$

$$\beta(t)=\sum_{i=1}^{20}\beta_i(t), \tag{47}$$

and

$$\gamma(t)=\frac{2^{-14}}{\Delta}\sum_{i=21}^{37}\left(\overline{o}_{++,i}\gamma_i(t)+\overline{o}_{+\times,i}\gamma_{+\times,i}(t)\right). \tag{48}$$

VII. Appendix B

The autocorrelation of $q_i[n]$ for i = 21, 22, …, 37 is derived in this appendix using a Markov chain to model the states of each ISI-scrambling 1-bit DAC. An analysis is first presented that applies to the primary 1-bit DACs, i.e., to $q_i[n]$ for i = 21, 22, …, 36. Then an analysis is presented that applies to the auxiliary 1-bit DAC, i.e., to $q_i[n]$ for i = 37.

Fig. 12 shows a Markov chain state diagram that applies to the ith ISI-scrambling 1-bit DAC for the example case of N_{Delay} = 4, where i = 21, 22, …, 36. The example uses N_{Delay} = 4 to simplify the figure and its explanation, but the results derived below apply to the general case.

Each of the states in Fig. 12 with a single output state transition probability of 1 implements a one clock delay wait period. For example, States 10-17 implement the 8 clock delays during which the ith 1-bit DAC is offline and its transients are changed from not swapped to swapped.

The hashmarks in Fig. 12 denote states in which the ith 1-bit DAC's transients are swapped. For example, the 1-bit DAC's

transients are swapped in the second half of States 10-17 as indicated by the hashmarks on the symbols for States 14-17.

As explained in Section II, whenever a primary ISI-scrambling 1-bit DAC goes from its offline to online state, all of the primary ISI-scrambling 1-bit DACs remain online for X clock periods where X is a random variable that takes on integer values from 1 to N_{Delay}, each with probability $q = 1/N_{Delay}$. Hence, if the ith 1-bit DAC is in State 1 at time index n, then the probability that one of the primary ISI-scrambling 1-bit DACs will be taken offline at time index n+1 is q. As there are 16 such 1-bit DACs, the probability that the ith 1-bit DAC will be taken offline at time index n+1 is q/16, and the probability that one of the other 1-bit DACs will be taken offline at time index n+1 is 15q/16. These two cases correspond States 10 and 2, respectively, in Fig. 12. If none of the primary 1-bit DACs are taken offline for another 1, 2, or 3 clock cycles, then the ith 1-bit DAC enters State 38, 37, or 36, respectively. Similar reasoning can be applied to each of the subsequent states to verify that the Markov chain correctly models the states of each primary ISI-scrambling 1-bit DAC per the explanation in Section II.

The number of Markov chain states, N_{States}, depends on N_{Delay}, which can be set via the SPI and can be as large as 65536. The example described above uses $N_{Delay} = 4$ which resulted in $N_{States} = 42$. In general, $N_{States} = 34+2N_{Delay}$ because the consecutive clock periods during which none of the primary 1-bit DACs are offline are represented by $2N_{Delay}$+2 possible states. Specifically, these states are States 1, 18, *C*-*D*, and *E*-*F*, where

$$\begin{aligned} C &= 35, & D &= 35 + N_{Delay} - 1, \\ E &= 35 + N_{Delay}, & F &= 35 + 2N_{Delay} - 1. \end{aligned} \tag{49}$$

It follows from (9), (30), and the Markov chain's definition that

$$q_i[n] = \begin{cases} 1, & \text{if } s_i[n] \in S_1, \\ -1, & \text{if } s_i[n] \in S_{-1}, \\ 0, & \text{otherwise}, \end{cases} \tag{50}$$

where $s_i[n]$ is the state of the Markov chain during the nth clock cycle, $S_1 = \{2, 3, \ldots, 9, C, C+1, \ldots, D\}$, and $S_{-1} = \{19, 20, \ldots, 26, E, E+1, \ldots, F\}$. Therefore,

$$\begin{aligned} E\{q_i[n]q_i[n+k]\} = &\sum_{u\in S_1}\sum_{v\in S_1} \Pr\left(s_i[n]=u,\, s_i[n+k]=v\right) \\ &+ \sum_{u\in S_{-1}}\sum_{v\in S_{-1}} \Pr\left(s_i[n]=u,\, s_i[n+k]=v\right) \\ &- \sum_{u\in S_1}\sum_{v\in S_{-1}} \Pr\left(s_i[n]=u,\, s_i[n+k]=v\right) \\ &- \sum_{u\in S_{-1}}\sum_{v\in S_1} \Pr\left(s_i[n]=u,\, s_i[n+k]=v\right), \end{aligned} \tag{51}$$

where $\Pr(s_i[n] = u, s_i[n+k] = v)$ is the joint probability that the Markov chain states at time indices n and $n+k$ are u and v, respectively.

The values of $\Pr(s_i[n] = u, s_i[n+k] = v)$ can be derived via the Markov chain's $N_{States} \times N_{States}$ state transition matrix, $\mathbf{P} = [p_{u,v}]$, where $p_{u,v}$ is the element on the uth row and vth column of $\mathbf{P}$ and is the probability that the Markov chain will be in State v at any time index m given that it was in State u at time index $m-1$. Although $\mathbf{P}$ has a relatively large dimension, most of its elements are zero. Specifically, the Markov chain's definition implies that the only non-zero elements of $\mathbf{P}$ are:

$$\begin{aligned} &p_{34,1} = p_{m,m+1} = 1 \text{ for all } m \notin \{1,9,18,26,34,D,E\}, \\ &p_{1,2} = p_{18,19} = 15q/16,\ p_{1,10} = p_{18,27} = q/16, \\ &p_{D,2} = p_{F,19} = 15/16,\ p_{D,10} = p_{F,27} = 1/16, \\ &p_{9,C+m} = p_{26,E+m} = q, \ \text{ for } 0 \le m < N_{Delay}, \\ &p_{1,C+m} = p_{18,E+m} = q, \ \text{ for } 1 \le m < N_{Delay}. \end{aligned} \tag{52}$$

The Markov chain's definition further implies that there is a non-zero probability of the system successively entering States 1-9, *C*-*D*, 10-26, *E*-*F*, 27-34, 1, which is a loop that includes all N_{States} states. This implies that every state can be reached from every other state, so the Markov chain satisfies the definition of being *irreducible*.

By the same reasoning, regardless of the system's state at any given time index n, there is a non-zero probability that it will return to the same state at time index $n+m$, where $m = N_{States}$. The Markov chain's definition also implies that there is a non-zero probability of the system successively entering the states in the order listed above but skipping either State *C* or State *E*. This implies that regardless of the system's state at any given time index n, there is a non-zero probability that it will return to the same state at time index $n+m$, where $m = N_{States}-1$. Given that the greatest common divisor of N_{States} and $N_{States}-1$ is 1 regardless of the value to which N_{States} is set, this implies that the Markov chain satisfies the definition of being *aperiodic*.

As the Markov chain is irreducible, aperiodic, and has a finite number of states, it approaches a steady state in that the sequence of its states' probability distributions as a function of time index n converges to a unique steady-state probability distribution as $n \to \infty$ [33]. This implies that

$$\begin{bmatrix} \pi_1 & \pi_2 & \cdots & \pi_{N_{States}} \end{bmatrix} = \begin{bmatrix} \pi_1 & \pi_2 & \cdots & \pi_{N_{States}} \end{bmatrix} \mathbf{P} \tag{53}$$

where π_u is the steady-state probability of the system being in State u. This matrix equation along with the probability distribution property that $\pi_1 + \pi_2 + \cdots + \pi_{N_{States}} = 1$ can be solved to find the values of $\pi_1, \pi_2, \cdots \pi_{N_{States}}$.

As the objective of this appendix is to derive the steady-state autocorrelation of $q_i[n]$, the Markov chain is taken to have converged to its steady state in the following analysis, i.e.,

$$\Pr\left(s_i[n] = u\right) = \pi_u \quad \text{for all } n. \tag{54}$$

Therefore,

$$\Pr\left\{s_i[n] = u,\ s_i[n+k] = v\right\} = \pi_u p_{u,v}(k) \tag{55}$$

where $p_{u,v}(k)$ is the probability that the Markov chain's state at time index $n+k$ is v given that it was in State u at time index n. Substituting this into (51) leads to an expression for $\mathrm{E}\{q_i[n]q_i[n+k]\}$ that is independent of n. This implies that $\mathrm{E}\{q_i[n]q_i[n+k]\} = \mathrm{E}\{q_i[n]q_i[n-k]\}$. Furthermore, the definition of $q_i[n]$ implies that $\mathrm{E}\{q_i[n]\} = 0$, so the mean of $q_i[n]$ is also independent of n. It follows that $q_i[n]$ is WSS. Substituting (55) into (51) and applying these observations implies that the autocorrelation of $q_i[n]$ can be written as

$$\begin{aligned} R_{q,i}[k] = &\sum_{u\in S_1} \pi_u \left[\sum_{v\in S_1} p_{u,v}\left(|k|\right) - \sum_{w\in S_{-1}} p_{u,w}\left(|k|\right) \right] \\ &+ \sum_{r\in S_{-1}} \pi_r \left[\sum_{s\in S_{-1}} p_{r,s}\left(|k|\right) - \sum_{t\in S_1} p_{r,t}\left(|k|\right) \right]. \end{aligned} \tag{56}$$

The properties of Markov chains imply that

$$\left[\, p_{u,1}(k) \quad p_{u,2}(k) \quad \ldots \quad p_{u,N_{States}}(k) \,\right] = \mathbf{b}_u \mathbf{P}^k, \qquad (57)$$

where $\mathbf{b}_u$ is a row vector of length N_{States} with a 1 in column u and zeros in all other columns [33]. Matrix equation (57) with the definition of $\mathbf{P}$ via (52) is used to calculate the values of $p_{u,v}(k)$ in (56).

The above analysis applies only to the primary ISI-scrambling 1-bit DACs, but it can be modified to apply to the auxiliary ISI-scrambling 1-bit DAC as follows. The properties of the $o_{37}[n]$ and $p_{37}[n]$ stochastic sequences described in Section II imply that the auxiliary ISI-scrambling 1-bit DAC's states can be modeled via a Markov chain with an $N_{States} \times N_{States}$ state transition matrix, $\mathbf{P} = [p_{u,v}]$, that is similar to that described above for the primary ISI-scrambling 1-bit DACs. The only non-zero elements of the state transition matrix are still given by (52) except with $p_{1,2} = p_{18,19} = p_{1,10} = p_{18,27} = q/2$ and $p_{D,2} = p_{F,19} = p_{D,10} = p_{F,27} = 1/2$ because of the 50% chance that the swap state of the auxiliary ISI-scrambling 1-bit DAC gets inverted each time it goes offline.

By the same reasoning applied previously, $\mathbf{P}$ is irreducible and aperiodic, and $q_{37}[n]$ is given by (50) with $i = 37$, $S_1 = \{3, 4, \ldots, 9, 28, 29, \ldots, 34\}$, and $S_{-1} = \{11, 12, ..., 17, 20, 21, \ldots, 26\}$. Consequently, $R_{q,37}[k]$ is given by (56) with probability distributions calculated via (53) and (57) using the version of $\mathbf{P}$ corresponding to the auxiliary ISI-scrambling 1-bit DAC.

VIII. Appendix C

Suppose $x[n_t] = 8192\Delta\sin(\omega_0 n_t)$, where $\omega_0 = 2\pi f_0/f_s$, and f_0/f_s satisfies (34). As $e_i(t)$ has zero mean and $x[n_t]$ is deterministic, the autocorrelation of $e_i(t)$ can be written as

$$R_{e,i}(t,\tau) = g_i(t)\, g_i(t+\tau)\, \mathrm{E}\{q_i[n_t]\, q_i[n_{t+\tau}]\}, \qquad (58)$$

with

$$g_i(t) = 2^{-2}\, \eta_i(t) \sin(\omega_0 n_t) \sin\left(\omega_0 (n_t - 1)\right). \qquad (59)$$

The DAC's input sequence is generated digitally, so f_0/f_s is a rational number. This implies that $g_i(t)$ is periodic with a period, T_g, where T_g is an integer multiple of T_s. As $\eta_i(t)$ is periodic with a period of T_s by definition, this implies that $g_i(t)g_i(t+\tau)$ is periodic in t with a period, T_g.

As proven in Appendix B, the discrete-time stochastic sequence, $q_i[n]$, is WSS, so the expectation term in (58) can be written as

$$\mathrm{E}\{q_i[n_t]\, q_i[n_{t+\tau}]\} = R_{q,i}[n_{t+\tau} - n_t], \qquad (60)$$

the right side of which is given by (56) with k replaced by $n_{t+\tau} - n_t$. The quantity $n_{t+\tau}$ can be written as $n_{t+\tau} = \lfloor n_t + \langle f_s t\rangle + n_\tau + \langle f_s \tau\rangle \rfloor$ where, for any real number x, $\lfloor x \rfloor$ denotes the largest integer less than or equal to x, and $\langle x\rangle = x - \lfloor x \rfloor$ is the fractional part of x. For any real numbers x and y, $\lfloor x \rfloor - \lfloor y \rfloor$ can be written as $\lfloor x - \lfloor y \rfloor \rfloor$, so

$$n_{t+\tau} - n_t = \left\lfloor \langle f_s t\rangle + n_\tau + \langle f_s \tau\rangle \right\rfloor. \qquad (61)$$

The only term that contains t on right side of (61) is $\langle f_s t\rangle$, which is T_s-periodic, so (60) must be T_s-periodic in t. Given $g_i(t)g_i(t+\tau)$ is periodic in t with a period, T_g, and T_g is an integer multiple of T_s, it follows from (58) and (60) that $R_{e,i}(t, \tau)$ is periodic in t with a period of T_g. Consequently, $e_i(t)$ is a cyclostationary random process and its average PSD is the Fourier transform of the average of $R_{e,i}(t,\tau)$ over one T_g period of t, i.e., the Fourier transform of

$$\bar{R}_{e,i}(\tau) = \frac{1}{T_g} \int_0^{T_g} g_i(t) g_i(t+\tau) R_{q,i}[n_{t+\tau} - n_t]\, dt\,. \qquad (62)$$

Substituting (59) into (62) and applying sinusoid product-to-sum identities shows that the integrand of (62) can be written as

$$\begin{aligned} f_\tau(t) \Big[& 2\cos^2(\omega_0) \\ & + \cos\left(2\omega_0 (n_{t+\tau} - n_t)\right) + \cos\left(2\omega_0 (n_{t+\tau} + n_t - 1)\right) \\ & - 2\cos(\omega_0)\cos\left(2\omega_0 n_t - \omega_0\right) \\ & - 2\cos(\omega_0)\cos\left(2\omega_0 n_{t+\tau} - \omega_0\right) \Big], \end{aligned} \qquad (63)$$

where

$$f_\tau(t) = 2^{-7}\, R_{q,i}\left[n_{t+\tau} - n_t\right] \eta_i(t) \eta_i(t+\tau)\,. \qquad (64)$$

Both $\cos(2\omega_0 n_t - \omega_0)$ and $\cos(2\omega_0 n_{t+\tau} + \omega_0)$ are constant with respect to t over successive intervals of T_s. Furthermore, they average to zero over intervals of T_g in t because the restrictions on ω_0 imposed by (34) prevent them from aliasing to zero frequency. By the same reasoning, $\cos(2\omega_0(n_{t+\tau} + n_t - 1))$ averages to zero over intervals of T_g in t, and it is constant with respect to t over two fixed sub-intervals of every successive T_s time interval. Given that $f_\tau(t)$ is T_s-periodic in t, the above observations imply that the last three terms on the right side of (63) average to zero in (62), so they do not contribute to $\bar{R}_{e,i}(\tau)$.

As explained above, (61) and, hence, $\cos(2\omega_0(n_{t+\tau} - n_t))$ are T_s-periodic in t. Given that $f_\tau(t)$ is T_s-periodic in t and $\cos^2(\omega_0)$ is constant, it follows that all the terms in (63) which contribute to $\bar{R}_{e,i}(\tau)$ are T_s-periodic in t, so (62) can be written as

$$\bar{R}_{e,i}(\tau) = \frac{1}{T_s} \int_0^{T_s} f_\tau(t) \left[2\cos^2(\omega_0) + \cos\left(2\omega_0 (n_{t+\tau} - n_t)\right) \right] dt\,. \qquad (65)$$

Equation (61) implies that

$$n_{t+\tau} - n_t = \begin{cases} n_\tau, & \text{if } \langle f_s t\rangle < 1 - \langle f_s \tau\rangle, \\ n_\tau + 1, & \text{otherwise,} \end{cases} \qquad (66)$$

so (65) with (64) can be rewritten as

$$\begin{aligned} \bar{R}_{e,i}(\tau) = {} & w_i[n_\tau] \int_0^{T_s(1 - \langle f_s \tau\rangle)} \eta_i(t) \eta_i(t+\tau)\, dt \\ & + w_i[n_\tau + 1] \int_{T_s(1 - \langle f_s \tau\rangle)}^{T_s} \eta_i(t) \eta_i(t+\tau)\, dt, \end{aligned} \qquad (67)$$

where

$$w_i[n_\tau] = \frac{2^{-7} R_{q,i}[n_\tau]}{T_s} \left[2\cos^2(\omega_0) + \cos\left(2\omega_0 n_\tau\right) \right]. \qquad (68)$$

As $\eta_i(t)$ is T_s-periodic, the $\eta_i(t+\tau)$ integrand factors in the first and second integrals on the right side of (67) can be replaced by $\eta_i(t+\tau-n_\tau T_s)$ and $\eta_i(t+\tau-(n_\tau+1)T_s)$, respectively, without changing $\bar{R}_{e,i}(\tau)$. By definition, $\langle f_s \tau\rangle = f_s \tau - n_\tau$, so these replacements can be written as $\eta_i(t + T_s\langle f_s \tau\rangle)$ and $\eta_i(t - T_s(1 - \langle f_s \tau\rangle))$, respectively. Hence, with these replacements, both integrals have integrands of the form $\eta_i(t)\eta_i(u)$ and the limits of integration are such that t and u are limited to and, together, span the range $[0, T_s]$. Therefore, (67) can be rewritten as

$$\begin{aligned} \bar{R}_{e,i}(\tau) = {} & w_i[n_\tau]\, \eta_{p^*,i}\left(\tau - n_\tau T_s\right) \\ & + w_i[n_\tau + 1]\, \eta_{p^*,i}\left(\tau - (n_\tau + 1) T_s\right), \end{aligned} \qquad (69)$$

where

$$\eta_{p^*,i}(u) = \int_{-\infty}^{\infty} \eta_{p,i}(t)\eta_{p,i}\left(t+u\right)dt \tag{70}$$

and

$$\eta_{p,i}(t) = \begin{cases} \eta_i(t) & \text{if } 0 \le t < T_s, \\ 0 & \text{otherwise.} \end{cases} \tag{71}$$

By definition, $\eta_{p^*,i}(\tau)$ is nonzero only when $-T_s < \tau < T_s$, so (69) can be rewritten as

$$\overline{R}_{e,i}(\tau) = \sum_{n=-\infty}^{\infty} w_i[n]\eta_{p^*,i}\left(\tau - nT_s\right). \tag{72}$$

Taking the CTFT of (72) yields

$$\begin{aligned} S_{e,i}\left(j\omega\right) &= H_{p^*,i}\left(j\omega\right)\sum_{n=-\infty}^{\infty} w_i[n]e^{-j\omega nT_s} \\ &= H_{p^*,i}\left(j\omega\right)W_i\left(e^{j\omega T_s}\right), \end{aligned} \tag{73}$$

where $H_{p^*,i}(j\omega)$ is the CTFT of $n_{p^*,i}(t)$ and $W_i(e^{j\omega Ts})$ is the DTFT of $w_i[n]$. Taking the DTFT of (68) with n_t replaced by n yields

$$\begin{aligned} W_i\left(e^{j\omega T_s}\right) = \frac{2^{-8}}{T_s}\Big[&4\cos^2\left(\omega_0\right)S_{q,i}\left(e^{j\omega T_s}\right) \\ &+ S_{q,i}\left(e^{j(\omega+2\omega_0)T_s}\right) + S_{q,i}\left(e^{j(\omega-2\omega_0)T_s}\right)\Big] \end{aligned} \tag{74}$$

where $S_{q,i}(e^{j\omega Ts})$ is the DTFT of $R_{q,i}[k]$ which is given by (56).

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Jason Remple received the B.S. degree from the University of California, Los Angeles, in 2005 and the M.S. degree from the University of California, San Diego, in 2012, both in electrical engineering. He is currently pursuing the Ph.D. degree at UCSD while working at Zeku.

Andrea Panigada (S'05-M'09) received the Laurea degree in electronic engineering from the University of Pavia, Italy, in 1999, and the M.S. and Ph.D degrees in electrical engineering from the University of California, San Diego, in 2009. From 2000 to 2004, he worked for STMicroelectronics as a Design Engineer, doing research on algorithms for the digital calibration of analog to digital converters (ADCs). From 2005 to 2009, he joined the Integrated Signal Processing Group as a PhD student, working with Prof. Ian Galton on a digital algorithm for the calibration of nonlinear effects introduced by analog components in ADCs. In 2009 he co-founded Linear Silicon Solutions, a start-up focused on the design of high speed data converters which was later acquired by Microchip Technology in 2011. He was with Microchip for 9 years, working on high speed pipelined ADCs and high resolution SAR ADCs. He joined Zeku in 2020. Dr. Panigada was the co-recipient of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Darlington Best Paper Award in 2008.

Ian Galton is a professor of electrical engineering at the University of California, San Diego (UCSD), where he teaches and conducts research in the field of mixed-signal integrated circuits and systems. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters and phase-locked loops. He received the Sc.B. degree from Brown University in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology in 1989 and 1992, respectively, all in electrical engineering. In 1992 and 1996 he joined the faculty at the University of California, Irvine, and UCSD, respectively. Dr. Galton has served on a corporate Board of Directors, on several corporate Technical Advisory Boards, and in several capacities for IEEE. Examples of the latter include serving as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society (SSCS) Administrative Committee, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE SSCS Distinguished Lecturer Program. Dr. Galton is an IEEE Fellow, holds the UCSD Skyworks Endowed Chair in High Performance Communications Devices and Circuits, and has received multiple IEEE best paper awards and UCSD Electrical and Computer Engineering Department best teacher awards.