Delta-Sigma FDC Enhancements for FDC-Based Digital Fractional-*N* PLLs

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***Abstract*— This paper describes all-digital enhancements for digital fractional-*N* phase-locked loops (PLLs) based on delta-sigma (ΔΣ) frequency-to-digital converters (FDCs). The enhancements include an improved dual-mode ring oscillator (DMRO)-based ΔΣ FDC architecture and a digital background calibration technique that compensates for the ΔΣ FDC's forward path gain error. The improved ΔΣ FDC has significantly relaxed timing constraints and a 3× smaller phase-frequency detector output pulse-width span relative to the prior art, which make it simpler to implement and amenable to higher-frequency reference signals. The calibration technique compensates for non-ideal DMRO frequencies in the digital domain. It eliminates the need to tune the DMRO instantaneous frequencies as a function of the PLL output frequency, thereby simplifying the DMRO implementation, and it also improves the phase noise performance of PLLs with high loop bandwidths.**

***Index Terms*— Delta-sigma (ΔΣ) modulation, digital background calibration, frequency-to-digital converter (FDC), frequency synthesizer, digital phase-locked loop (PLL).**

I. Introduction

DIGITAL fractional-*N* phase-locked loops (PLLs) based on second-order delta-sigma (ΔΣ) frequency-to-digital converters (FDCs) offer advantages of both analog and digital PLLs [1]–[12]. They have the same quantization error behavior as analog PLLs based on second-order ΔΣ modulators, but they do not require large-area analog loop filters.

This paper presents all-digital enhancements for ΔΣ FDCs that reduce implementation complexity and improve performance. The enhancements include a modified dual-mode ring oscillator (DMRO)-based ΔΣ FDC architecture and a digital background calibration technique that compensates for ΔΣ FDC forward path gain error caused by non-ideal DMRO frequencies.

The modified ΔΣ FDC architecture has relaxed timing constraints and a 3× smaller phase-frequency detector (PFD) output pulse-width span compared to prior-art ΔΣ FDCs [8]–[12]. These benefits make the new ΔΣ FDC simpler to implement [13]. They also make it amenable to higher-frequency reference signals for any given PLL output frequency, which is useful because increasing the reference frequency reduces the contributions of the reference signal phase noise, ΔΣ FDC quantization error, and DMRO phase noise to the PLL's output phase noise [11].

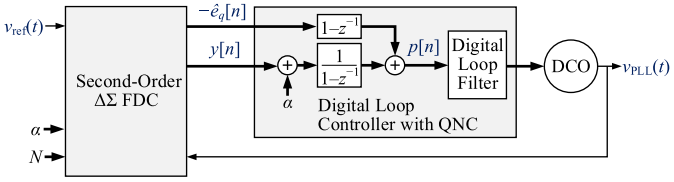

Fig. 1. High-level block diagram of a second-order ΔΣ FDC-based digital fractional-*N* PLL with quantization noise cancellation (QNC).

The DMRO in a DMRO-based ΔΣ FDC is designed to oscillate at one of two frequencies at any given time. These frequencies, denoted as f_{high} and f_{low} in this paper, ideally have a specific relationship to the PLL output frequency, f_{PLL}. In prior art DMRO-based ΔΣ FDCs, f_{high} and f_{low} are adjusted each time f_{PLL} is changed to approximate this ideal relationship, which adds complexity to the DMRO design. Furthermore, while the PLL's performance is relatively insensitive to deviations of f_{high} and f_{low} from their ideal values for low-to-moderate PLL bandwidths, this is not the case for high PLL bandwidths.

The proposed digital background calibration technique addresses these issues. Rather than dynamically adjusting f_{high} and f_{low} by controlling the DMRO's analog circuitry as a function of f_{PLL}, it dynamically adjusts digital circuitry to compensate for error that would otherwise be caused by non-ideal values of f_{high} and f_{low}. Moreover, it does so with much finer resolution than prior art ΔΣ FDCs are able to adjust the DMRO to tune f_{high} and f_{low}. These benefits greatly simplify the DMRO, which can now be designed to have fixed values of f_{high} and f_{low}, and significantly reduce phase noise for high PLL bandwidths.

The remainder of the paper consists of four main sections. Section II provides an overview of prior-art fractional-*N* PLLs that incorporate ΔΣ FDCs based on DMROs. Sections III and IV present the proposed ΔΣ FDC enhancements described above, and Section V presents simulation results that demonstrate their performance.

II. ΔΣ FDC Digital Fractional-*N* PLL Overview

A. ΔΣ FDC-Based PLL

A high-level block diagram of a second-order ΔΣ FDC-based fractional-*N* PLL is shown in Fig. 1. It consists of

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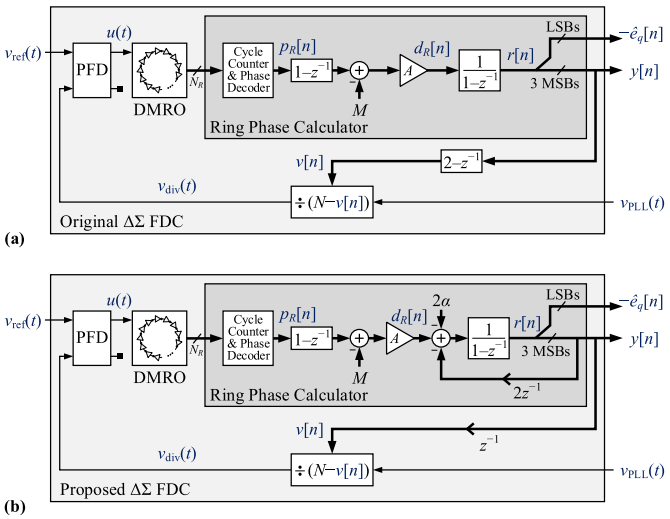

Fig. 2. (a) Simplified block diagram of the DMRO-based $\Delta\Sigma$ FDC described in [11], and (b) simplified block diagram of the proposed $\Delta\Sigma$ FDC.

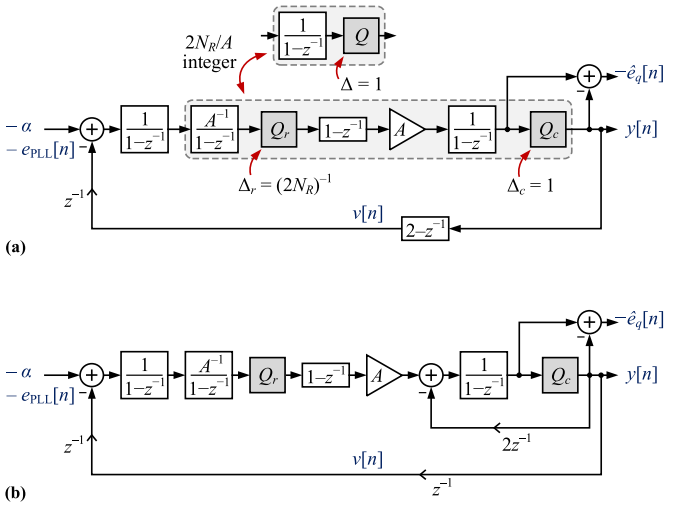

Fig. 3. Signal processing equivalents of the $\Delta\Sigma$ FDCs shown in Fig. 2(a) and Fig. 2(b) when they are locked.

a $\Delta\Sigma$ FDC, a digital loop controller (DLC) with quantization noise cancellation (QNC), and a digitally-controlled oscillator (DCO) [8]–[12]. The signal $v_{ref}(t)$ is the output of a reference oscillator with frequency f_{ref} and $v_{PLL}(t)$ is the PLL output waveform. Ideally, $v_{PLL}(t)$ is periodic with frequency $f_{PLL} = (N + \alpha) f_{ref}$, where N is a positive integer and α has a fractional value that can range from –1/2 to 1/2.

The $\Delta\Sigma$ FDC generates two f_{ref}-rate digital sequences, $y[n]$ and $-\hat{e}_q[n]$. Specifically,

$$y[n] = -\alpha - e_{PLL}[n] + \underbrace{e_q[n] - 2e_q[n-1] + e_q[n-2]}_{2^{nd}\text{-order shaped version of } e_q[n]}, \quad (1)$$

where $e_q[n]$ is the quantization error introduced by the $\Delta\Sigma$ FDC and $e_{PLL}[n]$ is a measure of the average frequency error of $v_{PLL}(t)$ over the nth reference period. The $\hat{e}_q[n]$ sequence is an estimate of $e_q[n]$. It is used to partially cancel the contribution of $e_q[n]$ at the input of the digital loop filter (DLF) within the DLC [12], [14], [15]. By cancelling the quantization error prior to the loop filter, QNC allows the PLL's bandwidth to be increased without significantly degrading the PLL's phase noise.

B. Original $\Delta\Sigma$ FDC Architecture

A simplified block diagram of the $\Delta\Sigma$ FDC presented in [11], hereafter referred to as the original $\Delta\Sigma$ FDC, is shown in Fig. 2(a). It consists of a PFD with top output $u(t)$, a multi-modulus divider with output $v_{div}(t)$, a DMRO, a digital ring phase calculator (RPC), and a $2-z^{-1}$ digital feedback block with output $v[n]$ that controls the divider. Although not shown in Fig. 2 for simplicity, the RPC's accumulator clips to keep its output in the range $-2 \le r[n] < 3$. As explained in [10], this reduces the PLL's worst-case locking time, but has no effect on the PLL's locked behavior. The PFD and divider are identical to those in analog PLLs.

Each reference period, the signal encoded in the width of the $u(t)$ pulse is accumulated by the DMRO. Then, the outputs of the DMRO, which represent a quantized version of its phase, are sampled and processed by the RPC to generate $y[n]$ and $-\hat{e}_q[n]$.

The DMRO is implemented as a ring of N_R nominally identical delay cells. Ideally, its instantaneous frequency is f_{high} when $u(t)$ is high and f_{low} when $u(t)$ is low, where

$$A\frac{(f_{high} - f_{low})}{f_{PLL}} = 1, \quad (2)$$

and A is a design parameter [11].[1]

Each reference period, the quantized DMRO phase, $p_R[n]$, is computed from the DMRO output lines. As indicated in Fig. 2(a), $p_R[n]$ is passed through a $1-z^{-1}$ block, and a positive constant, M, is subtracted from the result prior to the multiplication by A and accumulation. These operations yield $r[n]$, which is a fixed-point measure of $-\alpha - e_{PLL}[n]$ in units of cycles per reference period. The three most significant bits (MSBs) of $r[n]$ correspond to the integer part of $r[n]$, whereas the remaining least significant bits (LSBs) correspond to the fractional part of $r[n]$ [11].

The operation of the divider is such that adjacent rising edges of $v_{div}(t)$ are separated by $N - v[n]$ PLL output periods. Ideally, $v[n]$ would be set to $2r[n] - r[n-1]$, but dividers can only count integer numbers of PLL output periods and $r[n]$ contains both integer and fractional parts. Therefore, it is necessary to instead use just the integer part of $r[n]$, i.e., $y[n]$, so that $v[n] = 2y[n] - y[n-1]$ is integer-valued. Given that $y[n]$ is a quantized version of $r[n]$, the fractional part of $r[n]$, i.e., $-\hat{e}_q[n]$, is the negative of the corresponding quantization error. The DLC uses $-\hat{e}_q[n]$ to perform QNC.

As proven in [11], the behavior of the system shown in Fig. 2(a) is identical to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 3(a). The phase quantization operation performed by the DMRO is denoted by Q_r and modeled as a fine quantizer of step-size $\Delta_r = (2N_R)^{-1}$. Its quantization error, $e_{qr}[n]$, corresponds to the *residual* quantization error that is left after QNC. The quantization operation that occurs at the output of the RPC is denoted as Q_c and modeled as a *coarse* quantizer with step-size $\Delta_c = 1$. If $2N_R/A$ is integer-valued,

[1] In [11], 2^{-J}, where J is an integer, is used instead of A^{-1}, but the structures shown in Fig. 2 do not restrict A to be a power of 2.

then the blocks contained in the dashed contour in Fig. 3(a) are equivalent to an accumulator followed by a quantizer, Q, with unity step-size and associated error given by

$$e_q[n] = Ae_{qr}[n] + \hat{e}_q[n]. \tag{3}$$

In this case, $y[n]$ is given by (1) and the system's self-dithering property causes $e_q[n]$ to have a power spectral density (PSD) equivalent to that of a zero-mean white noise sequence with variance 1/12 [16], [17].

C. Original $\Delta\Sigma$ FDC Issues

The original $\Delta\Sigma$ FDC suffers from two issues. One issue is tight timing constraints on both the digital part of the $\Delta\Sigma$ FDC and the divider. The other issue is high sensitivity to non-ideal DMRO frequencies for high PLL bandwidths.

Once the $\Delta\Sigma$ FDC locks, the rising edges of $v_{\text{div}}(t)$ succeed and precede rising and falling edges of $v_{\text{ref}}(t)$, respectively [10], [11]. Therefore, as implied by Fig. 2(a), after the nth rising edge of $v_{\text{div}}(t)$, the $\Delta\Sigma$ FDC must compute $y[n]$ and use it along with $y[n-1]$ to form $v[n]$, which the divider then uses to determine the $(n+1)$th rising edge of $v_{\text{div}}(t)$. This limits the time available for the $\Delta\Sigma$ FDC to process the $u(t)$ pulse and compute $y[n]$ to approximately one reference period, and requires a divider that is capable of loading the divider modulus in the middle or toward the end of the divider count [10]. These features tend to increase the power consumption, circuit area, and complexity of the divider.

As explained in [11], $\Delta\Sigma$ FDC-based PLLs are not highly sensitive to non-ideal values of f_{high} and f_{low}, i.e., values of f_{high} and f_{low} that do not exactly satisfy (2), in much the same way that a second-order $\Delta\Sigma$ modulator is not sensitive to deviations in the gain of its second accumulator [16]. Nevertheless, the need to adjust the DMRO in the original $\Delta\Sigma$ FDC each time f_{PLL} changes so that f_{high} and f_{low} at least approximately satisfy (2) complicates the DMRO design. Moreover, as shown in Section IV, the accuracy with which (2) must be satisfied increases significantly with PLL bandwidth to the point that process, voltage, and temperature variations cause f_{high} and f_{low} to deviate from their ideal values enough to significantly degrade the PLL's phase noise.

III. Improved $\Delta\Sigma$ FDC

A. Proposed $\Delta\Sigma$ FDC Architecture

The proposed $\Delta\Sigma$ FDC is shown in Fig. 2(b).[2] It is similar to that shown in Fig. 2(a) except for the feedback digital block and the details of the RPC. Instead of feeding back $2y[n] - y[n-1]$ through the divider, $2y[n-1]$ is fed back directly to the input of the accumulator within the RPC, and only $y[n-1]$ is fed back through the divider.

An argument similar to that presented in [11] shows that the resulting system's behavior is identical to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 3(b), whose behavior is identical to that of the system shown in Fig. 3(a) provided $2N_R/A$ is integer-valued.

A feature of the original $\Delta\Sigma$ FDC is that once it locks, the DMRO locks to an average frequency of Mf_{ref}, which minimizes the potential for fractional spurs if M is integer-valued [10]. Specifically, given that $r[n]$ is bounded when the $\Delta\Sigma$ FDC is locked, the input to the accumulator within the RPC, and, hence, the M-adder output, must be zero-mean, which can only happen if the DMRO phase advances, on average, M cycles per reference period.

In the proposed $\Delta\Sigma$ FDC, the average of the M-adder output is forced to zero by subtracting 2α from the accumulator's input, so that the average DMRO frequency is given by Mf_{ref}. Reasoning similar to that presented above and (1) imply that without the 2α subtraction the local feedback around the accumulator would cause the output of the M-adder to have an average of $-2A^{-1}\alpha$. In this case, the DMRO would lock to $(M - 2A^{-1}\alpha) f_{\text{ref}}$, which would increase the potential for fractional spurs.

The 2α subtraction slightly increases the PLL's digital complexity relative to a comparable PLL based on the original $\Delta\Sigma$ FDC. For instance, in the PLL implementation described in Section V, the cycle counter and phase decoder's output, $p_R[n]$, has 10 fractional bits, α has 20 fractional bits, and $A = 1$, so the 2α subtraction nearly doubles the number of fractional bits required to represent the RPC accumulator's input. Nonetheless, the number of fractional bits in the DLF input is determined by α regardless of which $\Delta\Sigma$ FDC is used, so the proposed $\Delta\Sigma$ FDC's 2α subtraction only affects the RPC's accumulator. Hence, it represents only a minor increase in the PLLs overall digital complexity. Moreover, this increase in complexity is offset by the proposed $\Delta\Sigma$ FDC's features described below.

It follows from Fig. 3(b) that for the proposed $\Delta\Sigma$ FDC the discrete-time transfer function from the input to the second accumulator output has a pole at DC, which suggests that the system is unstable. Although the 2α term injected within the RPC causes the DC component at the output of the second accumulator to be zero, noise present at this node can cause the magnitude of the accumulator output to grow without bound. However, the second accumulation shown in Fig. 3(b) is performed by the DMRO, so this is not an issue in practice because the DMRO behaves as an accumulator with infinite output range [10]. Specifically, provided the cycle counter within the RPC does not roll-over more than once per reference period, which can be ensured by design, then the $1 - z^{-1}$ block within the RPC can unwrap the sampled DMRO phase and retrieve the information encoded in it, thereby allowing the magnitude of the second accumulator's output in Fig. 3(b) to be arbitrarily large.

While the DC pole issue is not a problem in the modified $\Delta\Sigma$ FDC as explained above, it would present practical issues if corresponding modifications were applied to the charge pump (CP)-based $\Delta\Sigma$ FDC described in [8], [9], and [12]. In CP-based $\Delta\Sigma$ FDCs, the CP performs integration in place of the DMRO, yet charge pumps do not offer the convenient roll-over feature inherent to DMROs.

[2]The sequences $v[n]$, $p_R[n]$ and $d_R[n]$ and the signals $u(t)$ and $v_{\text{div}}(t)$ in Fig. 2(b) are not identical to those in Fig. 2(a), but they play the same roles in both $\Delta\Sigma$ FDCs, which is why they share the same names.

B. Proposed ΔΣ FDC Features

1) Relaxed Timing Constraints: Fig. 4 shows example timing diagrams for the original and proposed ΔΣ FDCs, where the time sequences t_n and τ_n, for $n = 0, 1, 2, \ldots$, are the times of the nth rising edges of $v_{\text{ref}}(t)$ and $v_{\text{div}}(t)$, respectively, and the nth divider modulus is the number of PLL output periods between τ_{n-1} and τ_n. In this example, the DMRO phase is sampled at times $\gamma_n = t_n + T_{\text{ref}}/2$, where $T_{\text{ref}} = 1/f_{\text{ref}}$ is the reference period, and the nth divider modulus can be loaded at time t_n at the latest.

In the original ΔΣ FDC, the nth divider modulus is given by $N-(2y[n-1]-y[n-2])$, but as illustrated in Fig. 4(a), $y[n-1]$ cannot be computed before the DMRO phase is sampled at $\gamma_{n-1} > \tau_{n-1}$. It follows that the nth divider modulus can only be loaded once $y[n-1]$ is ready *around the middle or near the end* of the count, which increases the divider's complexity. For example, the divider in [10] required significant additional logic to meet this requirement compared to the original version of the divider presented in [18]. Furthermore, as the divider modulus must be updated before t_n, the amount of time available for the ΔΣ FDC to compute $y[n-1]$ is limited to $T_{\text{ref}}/2$.

As illustrated in Fig. 4(b), the proposed ΔΣ FDC has much more relaxed timing constraints. In this case, the nth divider modulus is given by $N - y[n-2]$. By the time of the $(n-1)$th rising edge of $v_{\text{div}}(t)$, the ΔΣ FDC has already had a duration of more than $T_{\text{ref}}/2$ to compute $y[n-2]$, so the next count can start with a known divider modulus. Alternatively, the computation of $y[n-2]$ can take up to T_{ref}, and the divider modulus can be updated *near the beginning* of the current count. In either case, compared to the original ΔΣ FDC, the proposed ΔΣ FDC allows for simpler divider topologies to be used and imposes looser digital timing constraints on the ΔΣ FDC.

2) Reduced PFD Output Span: As shown in [11], for the original ΔΣ FDC, $e_{\text{PLL}}[n]$ in (1) is given by

$$e_{\text{PLL}}[n] = \psi_{\text{PLL}}[n] - (N+\alpha)\,\psi_{\text{ref}}[n] - A\,(\psi_{\text{DMRO}}[n] - \psi_{\text{DMRO}}[n-1]), \quad (4)$$

the $e_q[n]$ sequence is bounded by

$$-1 < e_q[n] \le 0, \quad (5)$$

and the width of $u(t)$ is given by

$$\tau_n - t_n = T_{\overline{u}} + (-y[n-1] - \psi_{\text{PLL}}[n] + (N+\alpha)\,\psi_{\text{ref}}[n] - A\psi_{\text{DMRO}}[n-1] - e_q[n-1] + e_q[n-2] - \alpha)\,T_{\text{PLL}}, \quad (6)$$

where $\psi_{\text{PLL}}[n]$, $\psi_{\text{ref}}[n]$ and $\psi_{\text{DMRO}}[n]$ are the phase noise changes per reference period of $v_{\text{PLL}}(t)$, $v_{\text{ref}}(t)$ and the DMRO, respectively, and

$$T_{\overline{u}} = \frac{M - T_{\text{ref}} f_{\text{low}}}{f_{\text{high}} - f_{\text{low}}} \quad (7)$$

is the average width of the $u(t)$ pulse.

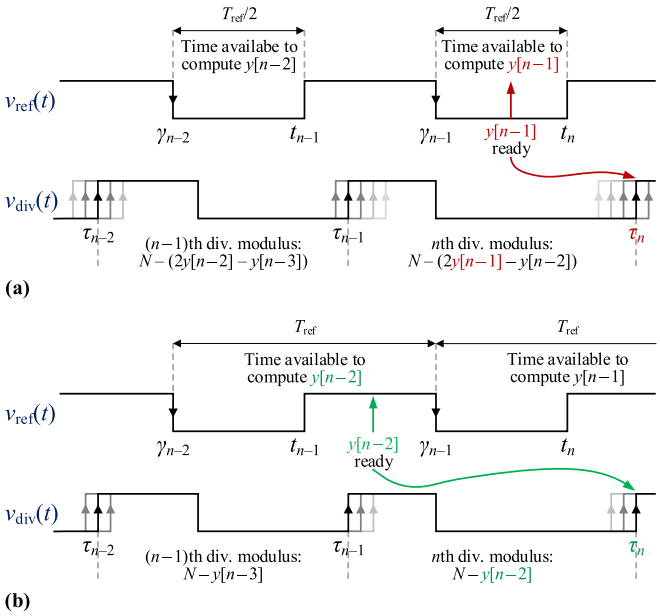

Fig. 4. Example timing diagram of (a) the original ΔΣ FDC and (b) the proposed ΔΣ FDC.

Suppose b_{PLL} and b_{DMRO} are the maximum magnitudes of $e_{\text{PLL}}[n]$ and $\psi_{\text{DMRO}}[n]$, respectively, so

$$|e_{\text{PLL}}[n]| < b_{\text{PLL}} \quad \text{and} \quad |\psi_{\text{DMRO}}[n]| < b_{\text{DMRO}} \quad (8)$$

for all n. Then, it follows from (1), (4)-(6) and (8) that the maximum span of $u(t)$, ΔT_u, which is defined as

$$\Delta T_u = 2 \max_n |\tau_n - t_n - T_{\overline{u}}|, \quad (9)$$

satisfies

$$\Delta T_u < 2\,(3 + 2b_{\text{PLL}} + Ab_{\text{DMRO}})\,T_{\text{PLL}}. \quad (10)$$

An analysis similar to that presented in [11] for the proposed ΔΣ FDC yields (4), (5), and the following expression for the width of the $u(t)$ pulse during the nth reference period:

$$\tau_n - t_n = T_{\overline{u}} + (y[n-1] - \psi_{\text{PLL}}[n] + (N+\alpha)\,\psi_{\text{ref}}[n] - A\psi_{\text{DMRO}}[n-1] - e_q[n-1] + e_q[n-2] + \alpha)\,T_{\text{PLL}}, \quad (11)$$

where $T_{\overline{u}}$ is also given by (7). Hence, (1), (4), (5), (8), (9) and (11) imply that, for the proposed ΔΣ FDC, ΔT_u satisfies

$$\Delta T_u < 2\,(1 + 2b_{\text{PLL}} + Ab_{\text{DMRO}})\,T_{\text{PLL}}. \quad (12)$$

In practice, b_{PLL}, $b_{\text{DMRO}} \ll 1$, so (10) and (12) imply that ΔT_u for the proposed ΔΣ FDC is approximately a third of that of the original ΔΣ FDC.

A smaller ΔT_u allows for a larger minimum difference between the phases of $v_{\text{ref}}(t)$ and $v_{\text{div}}(t)$, so it is beneficial as it mitigates spurs generated as a consequence of variations in the PFD supply voltage when $v_{\text{ref}}(t)$ and $v_{\text{div}}(t)$ are close in phase [19]. Additionally, reducing ΔT_u mitigates spurs from non-ideal DMRO behavior by increasing the time available for the DMRO's frequency transients to die out each reference period [10].

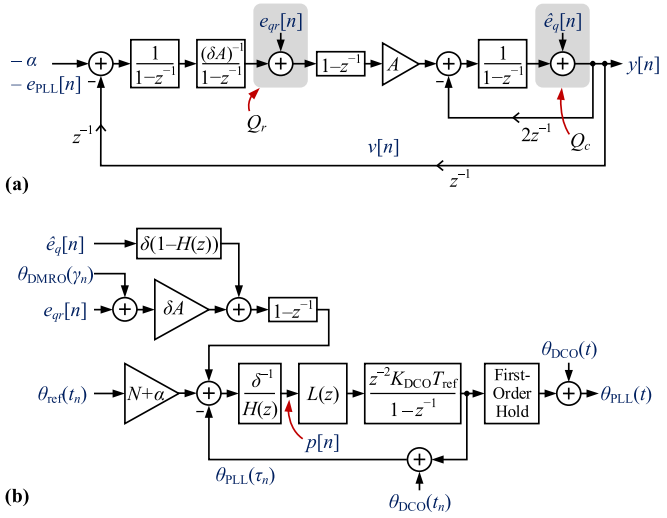

Fig. 5. (a) Behavioral model of the proposed ΔΣ FDC with (13), where Q_r and Q_c are replaced by the additive error sources $e_{qr}[n]$ and $\hat{e}_q[n]$, respectively, and (b) linearized model of the ΔΣ FDC-based PLL shown in Fig. 1 with the proposed ΔΣ FDC and (13).

3) Higher-Frequency Reference Signal: The relaxed timing constraints and smaller ΔT_u of the proposed ΔΣ FDC allows for the use of higher-frequency reference signals, which lowers the contribution to the PLL's phase noise from all noise sources within the ΔΣ FDC. As in conventional fractional-N PLLs, the contribution of the reference signal to the PLL output phase noise PSD, $S_{\mathrm{PLL}}(f)$, is proportional to $(N+\alpha)^2$ [8], [11]. Equations (1), (4) and Fig. 1 imply that the ΔΣ FDC quantization error and the DMRO phase noise appear first-order shaped at the DLF input, so their contribution to $S_{\mathrm{PLL}}(f)$ is proportional to $\sin^2(\pi T_{\mathrm{ref}} f)$. Additionally, the PSD of the quantization error is proportional to T_{ref} [11]. Therefore, increasing f_{ref} by a factor of x for a given f_{PLL} with all other things being the same reduces the contributions to the PLL's phase noise from the reference signal, ΔΣ FDC quantization error, and DMRO by $20\log(x)$, $30\log(x)$ and $20\log(x)$, respectively.

IV. Digital Gain Calibration Technique

A. Effects of ΔΣ FDC Forward Path Gain Error

As explained in Section III, the behavior of the system shown in Fig. 2(b) is identical to that of a second-order ΔΣ modulator provided (2) holds and $2N_R/A$ is integer-valued. However, in practice

$$A\frac{f_{\mathrm{high}}-f_{\mathrm{low}}}{f_{\mathrm{PLL}}}=\delta^{-1}, \tag{13}$$

where the deviation of the factor δ from its ideal value of 1 is the ΔΣ FDC's forward path gain error. This error degrades the system's self-dithering property [16], [17], and, as shown below, it reduces the extent to which QNC cancels the error introduced by the ΔΣ FDC's coarse quantization operation.

The analysis presented in [11] can be modified with (13) instead of (2) for the proposed ΔΣ FDC, which yields the behavioral model of the ΔΣ FDC shown in Fig. 5(a). The model is similar to that shown in Fig. 3(b), except that $e_{\mathrm{PLL}}[n]$ is given by (4) with δA instead of A, and the gain of the second accumulator is $(\delta A)^{-1}$ instead of A^{-1}. An analysis similar to that in [11] can also be performed to obtain a linearized model of the ΔΣ FDC PLL shown in Fig. 1 with the proposed ΔΣ FDC and (13) instead of (2). The resulting model is shown in Fig. 5(b), where $\theta_{\mathrm{ref}}(t)$, $\theta_{\mathrm{DMRO}}(t)$, $\theta_{\mathrm{DCO}}(t)$ and $\theta_{\mathrm{PLL}}(t)$ are the phase error waveforms of the reference signal, DMRO, DCO and PLL output, respectively,[3] $L(z)$ is the DLF's transfer function, K_{DCO} is the DCO gain (i.e., the amount in Hz by which the DCO frequency changes when the DCO input changes by unity) and

$$H(z)=1-\left(1-\delta^{-1}\right)z^{-2}. \tag{14}$$

It follows from Fig. 5(b) that the discrete-time transfer functions from $e_{qr}[n]$ and $\hat{e}_q[n]$ to the input of the DLF, $p[n]$, are given by

$$A\frac{\left(1-z^{-1}\right)}{H(z)}\frac{1}{1+T(z)} \quad \text{and} \quad \left(1-\delta^{-1}\right)z^{-2}\frac{\left(1-z^{-1}\right)}{H(z)}\frac{1}{1+T(z)}, \tag{15}$$

respectively, where

$$T(z)=\delta^{-1}K_{\mathrm{DCO}}T_{\mathrm{ref}}\frac{z^{-2}L(z)}{\left(1-z^{-1}\right)H(z)} \tag{16}$$

is the discrete-time loop gain of the PLL. The right-most expression in (15) implies that if $\delta=1$, then $p[n]$ does not depend on $\hat{e}_q[n]$, but if $\delta\neq 1$, then $\hat{e}_q[n]$ leaks into the DLF input. As the power of $\hat{e}_q[n]$ is much larger than that of $e_{qr}[n]$ in practice, this can be problematic, particularly for high PLL bandwidths. For instance, in the DMRO-based PLL presented in [10], $A=1$ and $N_R=13$, so $\Delta_r=1/26$ and the power of $\hat{e}_q[n]$ is approximately 28 dB larger than that of $e_{qr}[n]$ (recall that $\Delta_c=1$). In this case, (15) with $A=1$ implies that a ΔΣ FDC forward path gain error corresponding to $\delta^{-1}=1\pm 0.08$ would introduce an additional error component that depends on $\hat{e}_q[n]$ with approximately double the power of the component that depends on $e_{qr}[n]$. This would significantly increase the PLL output phase noise PSD at offset frequencies where the ΔΣ FDC quantization error contribution dominates those of the other noise sources.

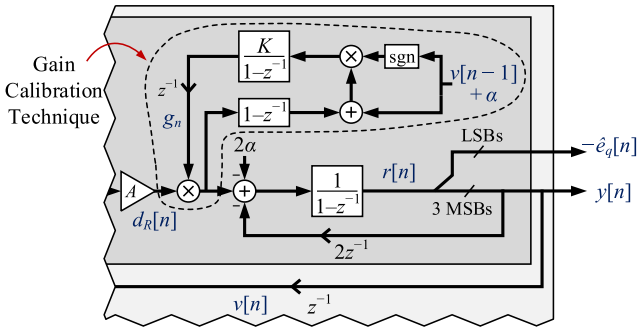

Fig. 6. Digital gain calibration technique shown in the context of the proposed DMRO-based ΔΣ FDC architecture.

[3] Reasoning similar to that presented in [8] can be applied to the linearized model shown in Fig. 5(b) to obtain expressions for the PLL output's phase noise components that depend on $\theta_{\mathrm{ref}}(t)$, $\theta_{\mathrm{DMRO}}(t)$, $\theta_{\mathrm{DCO}}(t)$, $e_{qr}[n]$ and $\hat{e}_q[n]$.

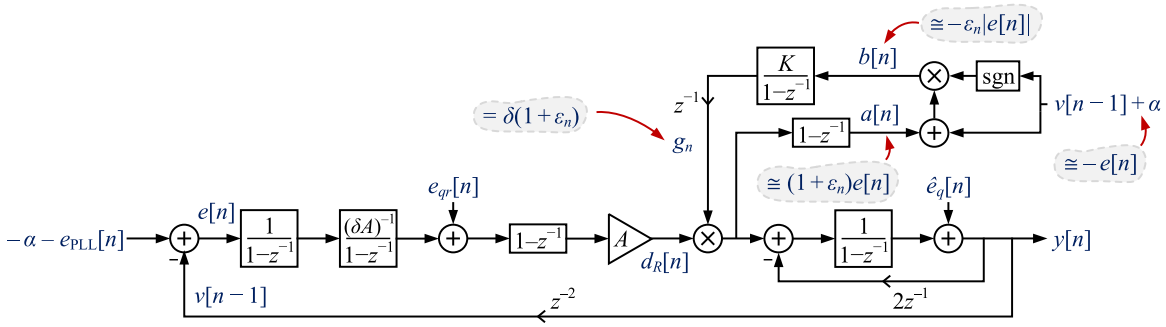

Fig. 7. Rearranged version of the behavioral model shown in Fig. 5(a) modified to accommodate the proposed gain calibration technique.

B. Proposed Digital Gain Calibration Technique

The proposed digital gain calibration technique is a modification of the $\Delta\Sigma$ FDC's RPC, the details of which are shown in Fig. 6, where $\mathrm{sgn}(x) = 1$ if $x \geq 0$ and -1 otherwise. To minimize clutter, Fig. 6 only shows a portion of the RPC. The modifications that implement the gain calibration technique are contained entirely within the dashed contour shown in the figure, and except for these modifications the $\Delta\Sigma$ FDC is identical to that shown in Fig. 2(b).

The gain calibration technique consists of a signed least-mean square (LMS)-like loop with gain K and output g_n, which digitally compensates for forward path gain error caused by $\delta \neq 1$. It is based on the following two results that can be derived from an analysis similar to that presented in [11]. The first result is that $d_R[n]$ in Fig. 2(b) can be multiplied by a constant factor g_n to compensate for non-ideal DMRO frequencies. In the presence of this factor, the transfer function from $\hat{e}_q[n]$ to $p[n]$ is given by

$$\left(1 - g_n\delta^{-1}\right) z^{-2} \frac{\left(1 - z^{-1}\right)}{H_g(z)} \frac{1}{1 + T_g(z)}, \tag{17}$$

where $H_g(z)$ is given by (14) with δ^{-1} replaced by $g_n\delta^{-1}$ and $T_g(z)$ is given by (16) with $H_g(z)$ and $g_n\delta^{-1}$ instead of $H(z)$ and δ^{-1}, respectively. It follows from (17) that $g_n = \delta$ makes the contribution to $p[n]$ from $\hat{e}_q[n]$ equal to zero. The second result is that $g_n(d_R[n] - d_R[n-1])$ equals $-v[n-1] - \alpha$ plus zero-mean error when g_n is equal to its ideal value of δ, i.e., $\delta(d_R[n] - d_R[n-1]) = -v[n-1] - \alpha$ plus zero-mean error.

These observations suggest that, provided it is stable, the gain calibration feedback loop ramps g_n up or down until it reaches the point where the input to the accumulator with gain K is zero-mean noise. Fig. 6 implies that this happens when $g_n(d_R[n] - d_R[n-1]) + v[n-1] + \alpha$ is uncorrelated with $v[n-1] + \alpha$. Therefore, to the extent that the error component in $\delta(d_R[n] - d_R[n-1])$ is uncorrelated with $v[n-1] + \alpha$, the system converges to the ideal value of $g_n = \delta$.

In addition to preventing $\hat{e}_q[n]$ from leaking into the PLL loop, the proposed calibration technique also allows for the use of DMRO topologies with coarse frequency tuning or no tuning at all. This not only simplifies the design and implementation of the DMRO, but also simplifies the system as it renders feedback loops that tune f_{high} and f_{low} as a function of f_{PLL} unnecessary.

The proposed calibration technique somewhat increases the digital complexity of the $\Delta\Sigma$ FDC, but typically does not add significantly to the PLL's overall power or area consumption. For example, in the PLL implementation described in Section V, both $d_R[n]$ and g_n have 10 fractional bits, so 20 fractional bits are required to represent $g_n d_R[n]$. Given that α also has 20 fractional bits, the gain calibration technique negligibly increases the number of fractional bits required to represent the RPC accumulator's input. Therefore, as the calibration technique's digital LMS loop is relatively simple, the f_{ref}-rate digital multiplier prior to the RPC's accumulator represents most of the calibration technique's added complexity.

C. Convergence Analysis

Fig. 7 shows the block diagram of Fig. 5(a) modified to include the gain calibration technique, where ε_n is the error in g_n at sample time n, which is defined as

$$\varepsilon_n = \delta^{-1} g_n - 1. \tag{18}$$

For any fixed value of g_n and neglecting $e_{qr}[n]$, Fig. 7 implies that $a[n]$ is equal to $(1+\varepsilon_n)e[n]$, because the two $1 - z^{-1}$ blocks cancel the two accumulators in the path between $e[n]$ and $a[n]$. The gain calibration loop adds $v[n-1] + \alpha$, which is an estimate of $-e[n]$, to $a[n]$, and multiplies the result by the sign of $v[n-1] + \alpha$ to obtain a measure of ε_n, $b[n]$, which is approximately equal to $-\varepsilon_n |e[n]|$.

More precisely, Fig. 7 and (18) imply that $e[n]$ is given by

$$e[n] = -v[n-1] - \alpha - e_{\mathrm{PLL}}[n], \tag{19}$$

and that $a[n]$ can be written as

$$a[n] = (1 + \varepsilon_n)\, e[n] + (\varepsilon_n - \varepsilon_{n-1}) \sum_{i=0}^{n-1} e[i] + a_e[n], \tag{20}$$

where $a_e[n]$ is the contribution of $e_{qr}[n]$ to $a[n]$. Substituting (19) into (20), adding $v[n-1] + \alpha$ to the result, and then multiplying the resulting expression by $\mathrm{sgn}(v[n-1] + \alpha)$ yields

$$b[n] = -\varepsilon_n\, |v[n-1] + \alpha| + b_e[n], \tag{21}$$

where $b_e[n]$ is error that arises from the error in the estimate of $e[n]$, the contribution of $e_{qr}[n]$, and g_n not being constant.

Fig. 7 together with (18) and (21) further imply that

$$\varepsilon_{n+1} = \left(1 - \delta^{-1} K\, |v[n-1] + \alpha|\right) \varepsilon_n + \delta^{-1} K b_e[n], \tag{22}$$

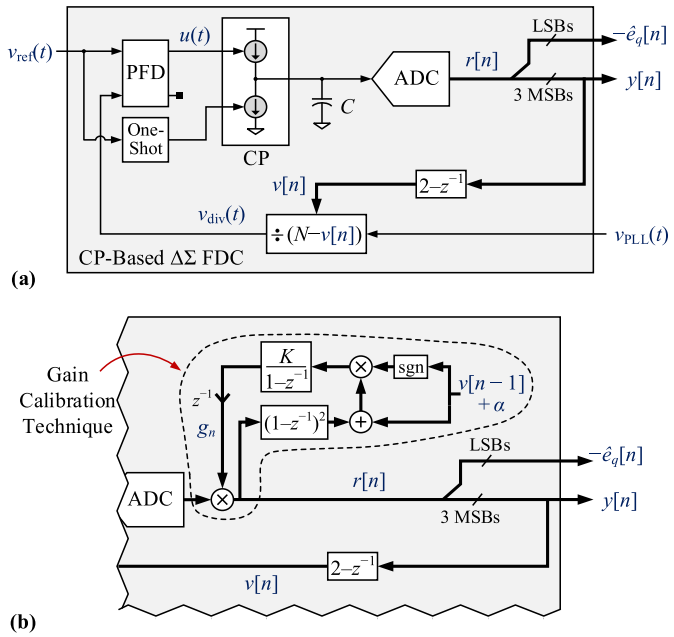

Fig. 8. (a) Simplified block diagram of CP-based ΔΣ FDC, and (b) digital gain calibration technique shown in the context of the CP-based ΔΣ FDC architecture.

from which it follows that

$$\overline{\varepsilon}_{n+1} = \left(1 - \delta^{-1} K \left|v[n-1] + \alpha\right|\right) \overline{\varepsilon}_n + \delta^{-1} K \overline{b_e}[n], \quad (23)$$

where $\overline{\varepsilon_n}$ and $\overline{b_e}[n]$ are the expected values of ε_n and $b_e[n]$, respectively, conditioned to the sequence $v[n-1]$.

When $\delta \neq 1$, the self-dithering property of the ΔΣ FDC is not perfect, so $e_{qr}[n]$ can be correlated with $\text{sgn}(v[n-1]+\alpha)$. Furthermore, it follows from Fig. 1 that

$$p[n] = -e_q[n] + e_q[n-1] + \sum_{i=0}^{n} y[i] + \alpha \quad (24)$$

so Fig. 5(b) and $v[n-1] = y[n-2]$ imply that the term $\psi_{PLL}[n] = \theta_{PLL}(\tau_n) - \theta_{PLL}(\tau_{n-1})$ in $e_{PLL}[n]$, which depends on a low-pass filtered version of $p[n]$, can also be correlated with $\text{sgn}(v[n-1]+\alpha)$. As $b_e[n]$ depends on both $e_{qr}[n]$ and $e_{PLL}[n]$, it follows from these observations that $\overline{b_e}[n]$ in (23) is not zero, so $b_e[n]$ biases the LMS loop and causes g_n to converge to a value that is slightly different than δ. However, numerous simulations run by the authors suggest that the magnitude of this bias is sufficiently small that $\overline{b_e}[n]$ can be neglected in the remainder of the analysis. Hence, (23) reduces to

$$\overline{\varepsilon}_{n+1} = \left(1 - \delta^{-1} K \left|v[n-1] + \alpha\right|\right) \overline{\varepsilon}_n. \quad (25)$$

The recursive application of (25) to itself yields

$$\overline{\varepsilon}_{n+1} = \prod_{i=0}^{n} \left(1 - \delta^{-1} K \left|v[i-1] + \alpha\right|\right) \overline{\varepsilon}_0, \quad (26)$$

which implies that, on average, ε_{n+1} tends to zero provided K is chosen such that

$$\lim_{n\to\infty} \prod_{i=0}^{n} \left(1 - \delta^{-1} K \left|v[i-1] + \alpha\right|\right) = 0. \quad (27)$$

TABLE I
PARAMETERS USED FOR THE SIMULATIONS

Design Parameters		Value	
Reference Source	Frequency, f_{ref}	26 MHz	
	Phase noise (white)	−155 dBc/Hz	
DCO	DCO gain, K_{DCO}	40 kHz	
	Phase noise [1]	−130, −125 and −150 dBc/Hz	
DMRO	Number of stages, N_R	31	
	Frequencies, f_{low}, f_{high}	150 MHz, 3.0 GHz (nominal)	
		225 MHz, 2.5 GHz ($\delta^{-1}=0.8$)	
		142 MHz, 3.3 GHz ($\delta^{-1}=1.1$)	
	Phase noise [1]	−99, −109 and −150 dBc/Hz	
FDC	Fixed count, M	40	
	A	1	
DLF	Loop gain multiplier, K_M	1.5	
	Proportional gain, K_P	2^6	2^5
	Integral gain, K_I	2^{-2}	2^{-4}
	IIR poles, λ_0, λ_1	2^{-1}, 2^0	2^{-2}, 2^{-1}
PLL Settings	Integer multiplier, N	110	
	Fractional multiplier, α	0.001008987426758	
	Output frequency, f_{PLL}	2.86 GHz	
	Loop bandwidth	1 MHz	500 kHz

[1] $1/f^3$, $1/f^2$ and white phase noise components at 1 MHz offset.

As $|v[n-1]+\alpha|$ is bounded and is regularly non-zero, (27) is easy to satisfy in practice.

D. Gain Calibration Technique for CP-Based ΔΣ FDCs

The digital gain calibration technique shown in Fig. 6 can be modified to apply to the CP-based ΔΣ FDC shown in Fig. 8(a) [8], [9], [12]. The modified version of the digital gain calibration technique is shown in Fig. 8(b). Its implementation details are almost identical to those in Fig. 6, except for an extra $1-z^{-1}$ block. In the CP-based ΔΣ FDC, the CP and subsequent analog-to-digital converter (ADC) play the same role as the DMRO in the DMRO-based ΔΣ FDC. The DMRO-based ΔΣ FDC already has a $1-z^{-1}$ block following the DMRO, which is needed as part of the circuitry that makes it possible to read out the DMRO's phase error [10], but this block is not necessary in the CP-based ΔΣ FDC. The additional $1-z^{-1}$ block in Fig. 8(b) compensates for the absence of a $1-z^{-1}$ block at the output of the ADC in the CP-based ΔΣ FDC architecture.

V. SIMULATION RESULTS

This section presents results from bit-exact, event-driven, behavioral C code simulations of the fractional-*N* PLL of Fig. 1 with the proposed ΔΣ FDC and digital gain calibration technique. All digital operations were simulated with fixed-point arithmetic. The PLL's DLF consists of a loop gain multiplier with gain K_M, two single-pole IIR stages with poles at λ_0 and λ_1, and a proportional-integral stage with proportional path gain K_P and integral path gain K_I. Its transfer function is given by

$$L(z) = K_M \left(K_P + \frac{K_I}{1-z^{-1}}\right) \prod_{i=0}^{1} \frac{\lambda_i}{1-(1-\lambda_i)\,z^{-1}}. \quad (28)$$

The parameters used for the simulations are listed in Table I.

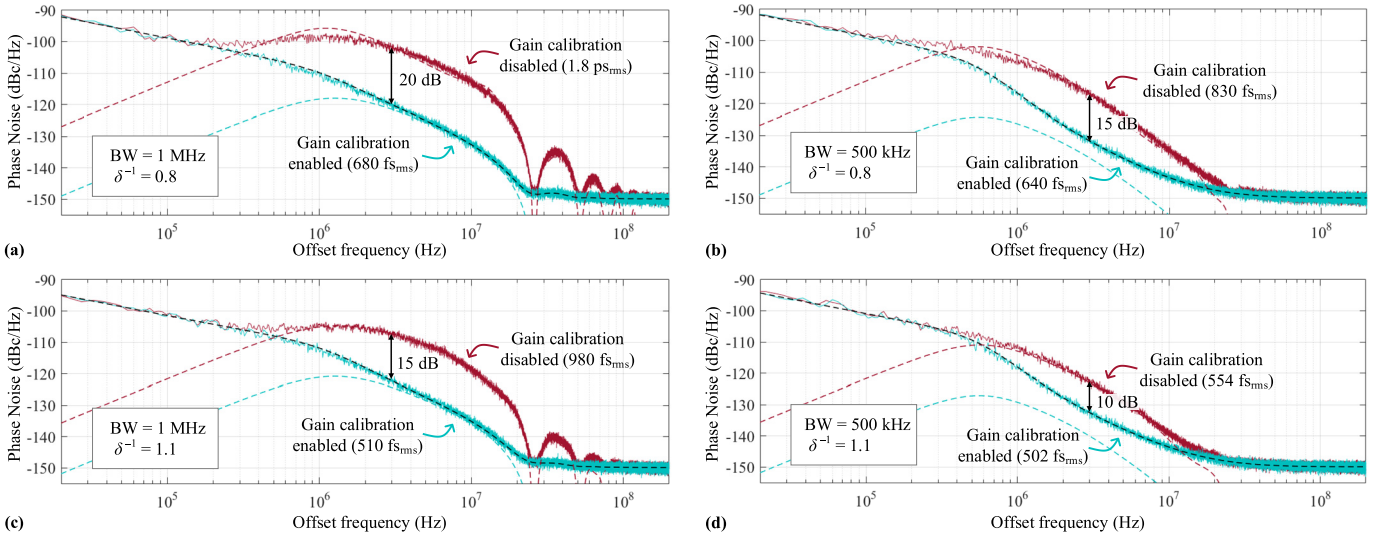

Fig. 9. Simulated PLL phase noise PSD with and without gain calibration enabled for four combinations of PLL bandwidth (BW) and δ^{-1}. The black and colored dashed curves correspond to the theoretical phase noise PSD for $g_n = \delta$ and the combined contribution to the PLL phase noise from $e_{qr}[n]$ and $\hat{e}_q[n]$, respectively.

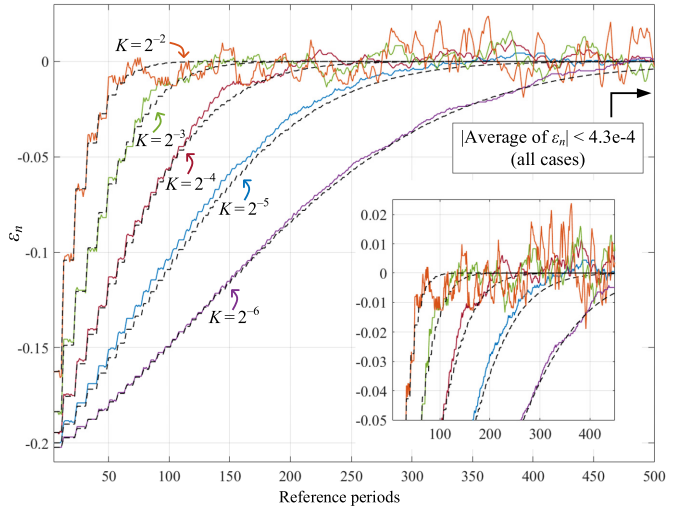

Fig. 10. Sequence ε_n as a function of n for several values of K, where ε_n calculated via (29) is plotted as a dashed curve for each case.

Fig. 9 shows the simulated PLL phase noise PSD with and without gain calibration enabled for four different combinations of PLL bandwidth and $\Delta\Sigma$ FDC forward path gain. For each case it also shows the theoretical PLL phase noise PSD with $g_n = \delta$ as a black dashed curve, and the theoretical combined contribution to the PLL phase noise from $e_{qr}[n]$ and $\hat{e}_q[n]$ as colored dashed curves.[4] As demonstrated in the figure, the higher the PLL bandwidth, the more sensitive the PLL's phase noise is to the $\Delta\Sigma$ FDC quantization error, which becomes more dominant when less filtering is applied to $p[n]$. Consequently, deviations of δ^{-1} from its ideal value of 1 cause a significant degradation of the PLL phase noise PSD for high PLL bandwidth settings.

Given that $N_R = 31$, the power of $\hat{e}_q[n]$ is approximately 36 dB larger than that of $e_{qr}[n]$. Therefore, in the absence of gain correction, it follows from (15) with $A = 1$ that the power of the additional quantization error component seen by the PLL loop is approximately 22 dB and 16 dB higher than that of the $e_{qr}[n]$ component for $\delta^{-1} = 0.8$ and $\delta^{-1} = 1.1$, respectively. This is supported by the simulation results shown in Fig. 9(a) and Fig. 9(c), where the spot phase noise degradation at a 3 MHz offset frequency is approximately 20 dB and 15 dB, respectively.

Fig. 10 shows ε_n versus time for several values of K with a PLL bandwidth of 1 MHz and $\delta = 0.8$.[5] Equation (26) with ε_0 in place of $\overline{\varepsilon}_0$, i.e.,

$$\prod_{i=0}^{n} \Big(1 - \delta^{-1} K \, |v[i-1] + \alpha|\Big)\varepsilon_0, \tag{29}$$

is also plotted (as a dashed curve) for each value of K to provide a comparison baseline and show that the evolution of g_n follows the trend predicted by the analysis in Section IV-C. The simulated PLL phase noise PSD after g_n converged was nearly identical to that shown in Fig. 9(a) with gain calibration enabled. In the $K = 2^{-2}$ case, however, the total integrated jitter increased slightly to 688 fs_{rms} because of the relatively large variance of ε_n. As shown in the figure's inset, ε_n crosses the -0.01 mark for the first time in about 50 reference periods (1.9 μs) and 400 reference periods (15.4 μs) for $K = 2^{-2}$ and $K = 2^{-6}$, respectively, and the absolute value of the mean error after convergence is lower than 0.043% of δ in all cases.

As in most LMS-like algorithms, the choice of K represents a tradeoff between convergence speed and the error variance of g_n [20], [21]. Although it might be possible to derive a

[4]The curves corresponding $e_{qr}[n]$ and $\hat{e}_q[n]$ were generated under the assumption that both sequences are white. However, the sequences are not necessarily white if $\delta \neq 1$, which is why the simulated curves in Fig. 9 deviate somewhat from their respective theoretical predictions, particularly in the $\delta^{-1} = 0.8$ case.

[5]The resolution of the gain calibration technique's accumulator was limited to 1 integer bit and 36 fractional bits, but its output, g_n, was truncated to have only 10 fractional bits to reduce hardware complexity.

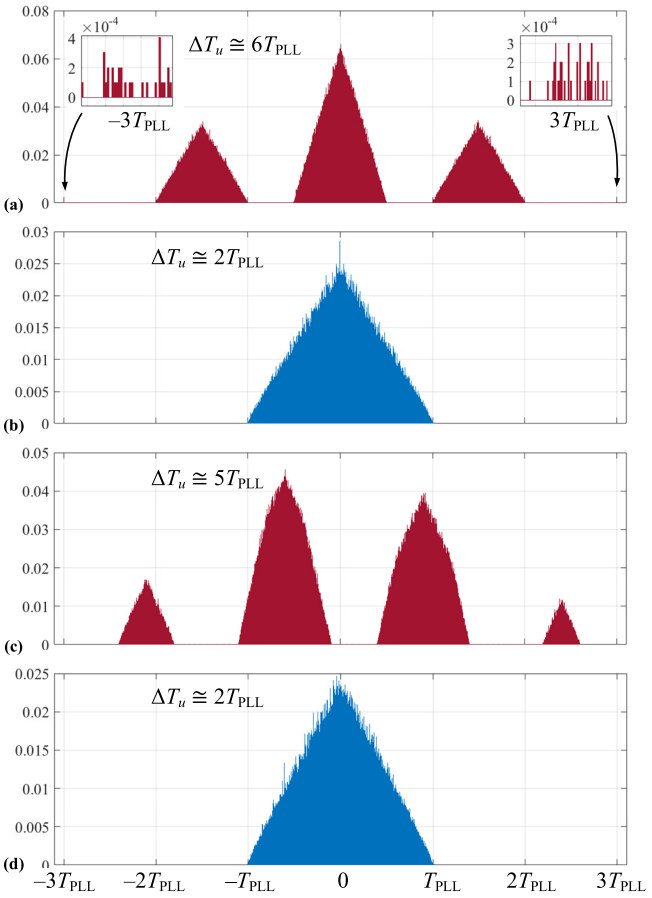

Fig. 11. Normalized histogram of $u(t)$ pulse width minus $T_{\overline{u}}$ calculated via (7) for the original FDC [(a) and (c)] and the proposed FDC [(b) and (d)], where $\alpha = 0.001008987426758$ for (a) and (b) and $\alpha = 0.401008987426758$ for (c) and (d).

closed-form expression that quantifies this tradeoff for the proposed calibration technique, the authors currently choose the value of K based on simulation results.

Fig. 11 shows normalized histograms of $\tau_n - t_n - T_{\overline{u}}$, where $T_{\overline{u}}$ was calculated using (7), for both the original $\Delta\Sigma$ FDC and the proposed $\Delta\Sigma$ FDC. The $u(t)$ pulse widths were measured for over one million reference periods after the gain calibration had converged with $K = 2^{-9}$. The 1 MHz-bandwidth set of parameters with $\delta = 0.8$ was used for the simulations in Fig. 11(a) and Fig. 11(b), whereas the same parameters except for α, which was set to 0.401008987426758, were used for the simulations in Fig. 11(c) and Fig. 11(d).

Although (10) and (12) do not show an explicit dependence of the $u(t)$ pulse-width span on α in either $\Delta\Sigma$ FDC version, it follows from (1) and Fig. 2 that different $\Delta\Sigma$ FDC output levels are exercised for different values of α. Accordingly, different values of α cause $e_q[n]$ to take different values with higher probability than others, which affects the histogram shapes shown in Fig. 11 but not the maximum $u(t)$ pulse-width.

As explained in Section III-B, the span of the $u(t)$ pulse-width in the proposed $\Delta\Sigma$ FDC is approximately three times smaller than that of the $u(t)$ pulse-width in the original $\Delta\Sigma$ FDC, which is supported by the simulation results shown in Fig. 11. As shown in Fig. 11(a), the span of $u(t)$ in the original $\Delta\Sigma$ FDC goes from $-3T_{\text{PLL}}$ to $3T_{\text{PLL}}$, although it reaches the extremes values only rarely. As demonstrated by the results in Fig. 11(c), the span is about $5T_{\text{PLL}}$ for a larger value of α, and the extreme values in this case (i.e., around $-2.4T_{\text{PLL}}$ and $2.6T_{\text{PLL}}$) are reached with higher probability compared to Fig. 11(a). Conversely, as shown in Fig. 11(b) and Fig. 11(d), the proposed architecture's $u(t)$ pulse-width span does not vary significantly with α, and as suggested by (12), it is approximately limited to $2T_{\text{PLL}}$.

VI. Conclusion

This paper presents all-digital enhancements of digital fractional-N PLLs based on $\Delta\Sigma$ FDCs. The enhancements comprise an improved DMRO-based $\Delta\Sigma$ FDC architecture and a digital background gain calibration technique. The former reduces the span of the PFD output pulse-width and significantly relaxes the timing constraints imposed on the $\Delta\Sigma$ FDC's digital portion and divider, which makes the system amenable to simpler divider topologies and higher-frequency reference signals. The latter compensates for non-ideal DMRO frequencies in the digital domain, thereby facilitating the use of simple DMRO topologies with fixed values of f_{high} and f_{low}, and improving the phase noise performance of high-bandwidth PLLs.

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