A 600-MS/s DAC With Over 87-dB SFDR and 77-dB Peak SNDR Enabled by Adaptive Cancellation of Static and Dynamic Mismatch Error

Derui Kong, Kevin Rivas-Rivera, and Ian Galton

***Abstract*— This paper presents a Nyquist-rate current-steering digital-to-analog converter that achieves a peak spurious-free dynamic range better than 87 dB and a peak signal-to-noise-and-distortion ratio better than 77 dB over a 265-MHz signal band. It is enabled by a fully integrated digital calibration technique that measures and cancels both static and dynamic mismatch errors over the first Nyquist band, and various circuit-level techniques that mitigate the effects of jitter and inter-symbol interference.**

***Index Terms*— Calibration, digital-to-analog converter (DAC), dynamic element matching (DEM), inter-symbol interference (ISI), mismatch noise cancellation (MNC).**

I. Introduction

NYQUIST-RATE digital-to-analog converters (DACs) with continuous-time output waveforms are widely used in moderate-to-high-bandwidth applications, such as wireless base stations. Such DACs generate a continuous-time analog output pulse once every clock period. Ideally, the amplitude of each pulse is scaled by the value of the DAC's input sequence during its clock period, but otherwise, the pulses have identical shapes.

Unfortunately, non-ideal circuit behavior causes input-dependent deviations of both the amplitude and shape of each output pulse, which introduces nonlinear error in the DAC's output waveform. The portion of the error from pulse amplitude deviations is called static error, and that from pulse shape deviations is called dynamic error. Both types of error significantly limit DAC performance in practice. In many Nyquist-rate DACs, clock skew and mismatches among nominally identical DAC components are the dominant causes of these errors. Clock skew causes dynamic error and component mismatches cause both static and dynamic error.

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Several previously published DACs incorporate methods to mitigate error from clock skew and component mismatches. These methods include randomization techniques, such as dynamic element matching (DEM) and digital random return-to-zero (DRRZ), dynamic mismatch mapping (DMM), and various mixed-signal calibration techniques [1]–[15]. Randomization techniques cause static error and, in some cases, dynamic error to be wideband noise instead of harmonic distortion. Hence, they improve DAC linearity, but at the expense of significantly reduced signal-to-noise ratio (SNR). DMM is a foreground calibration technique that reorders the usage pattern of nominally identical components to reduce integral nonlinearity (INL). While beneficial, it does not improve differential nonlinearity (DNL) and it tends to be limited by compromises made between improving static and dynamic error. Previously published on-chip mixed-signal calibration techniques have been demonstrated that suppress the static error, but not dynamic error.

A mixed-signal calibration technique called mismatch noise cancellation (MNC) was recently proposed in [16] that adaptively measures and cancels both static and dynamic error from clock skew and component mismatches over the DAC's signal band. This paper presents the first DAC IC implemented with MNC. With MNC enabled, the DAC's measured spurious-free dynamic range (SFDR) is better than 87 dB and its peak signal-to-noise-and-distortion ratio (SNDR) is better than 77 dB over a 265-MHz signal band. With MNC disabled, the SFDR and SNDR drop by more than 24 and 20 dB, respectively. Additional measured results further demonstrate that MNC cancels dynamic error as well as static error, as predicted by theory. As [16] presents a theoretical analysis of the MNC technique, this paper focuses on its practical implementation details and presents several circuit-level techniques incorporated in the DAC to reduce jitter and inter-symbol interference (ISI).

II. Signal Processing Overview

As shown in Fig. 1, the prototype IC consists of a 600-MHz 14-bit main DAC, and an MNC feedback path that measures and cancels the main DAC's signal band error from clock skew and component mismatches. The feedback path consists of a 3-GHz VCO-based ADC, a low-pass decimation filter, a digital error estimator block, and a 600-MHz 9-bit correction DAC.

The sampling theorem implies that no matter what error is introduced by the main DAC, there must exist a correction

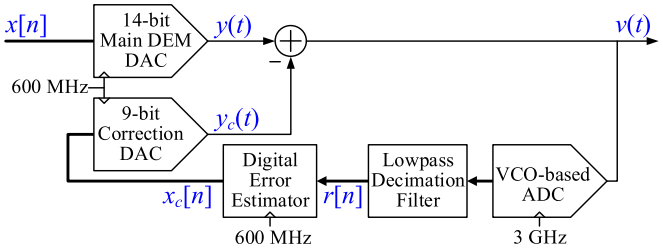

Fig. 1. High-level signal processing block diagram of the prototype IC.

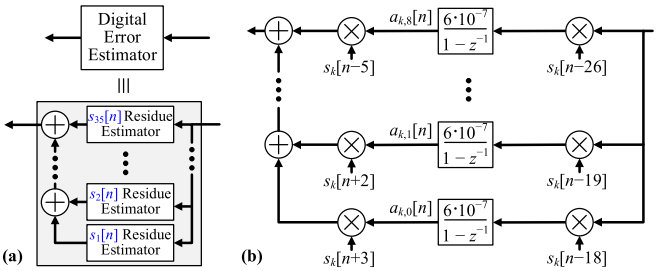

Fig. 2. (a) High-level structure of the digital error estimator. (b) Signal processing details of each $s_k[n]$ error estimator for $k = 1, 2, \ldots, 35$.

DAC input sequence, $x_c[n]$, that would result in a correction DAC output waveform, $y_c(t)$, which would cancel the error over the first Nyquist band up to the accuracy of the correction DAC. The correction DAC's minimum step size must be small enough that error from the quantization of $x_c[n]$ is well below the post-cancellation target noise and distortion floor of the main DAC, and the correction DAC's output range must be large enough to cancel the main DAC's error components. As explained in Section III-B, the correction DAC's resolution of 9 bits and step size equal to a quarter of that of the main DAC are sufficient for this purpose.

The main DAC's static and dynamic output error from clock skew and component mismatches has the form

$$e_{\mathrm{DAC}}(t) = \sum_{k=1}^{35} d_k(t) s_k[n_t] \tag{1}$$

where each $d_k(t)$ is an $f_s = 600$ MHz periodic waveform that depends on the main DAC's clock skew and component mismatches but not on the DAC's input sequence, n_t is the largest integer less than or equal to $f_s t$ at time t, and the $s_k[n]$ sequences are generated explicitly within the DEM encoder so they are known to the system a priori [6], [17]. The $s_k[n]$ sequences each take on values of -1, 0, and 1, and when DEM is enabled, they are zero-mean, white pseudo-random sequences that are uncorrelated with the main DAC's input sequence and each other.

The objective of the MNC feedback loop is to make $y_c(t)$ well-approximate $e_{\mathrm{DAC}}(t)$ over the signal band. To do this, the MNC feedback loop must measure $e_{\mathrm{DAC}}(t)$ over the first Nyquist band, which requires a digitized version of the main DAC's output waveform that has been filtered to include only the first Nyquist band. The oversampling VCO-based ADC and the decimation filter in Fig. 1 perform this operation, so $r[n]$ contains a component equal to the portion of $e_{\mathrm{DAC}}(t)$ restricted to the first Nyquist band that is left over from imperfect MNC cancellation.

Ideally, once the MNC feedback loop converges, $r[n]$ becomes free of $e_{\mathrm{DAC}}(t)$, in which case it is uncorrelated with all of the $s_k[n]$ sequences. Otherwise, $r[n]$ contains a residual component of $e_{\mathrm{DAC}}(t)$ restricted to the first Nyquist band, so it is correlated with at least some of the $s_k[n]$ sequences. Furthermore, the Nyquist-band filtering has an impulse response that is many 600-MHz samples long, so prior to full MNC convergence $r[n]$ is correlated with multiple time-shifted versions of the $s_k[n]$ sequences.

The MNC technique exploits these properties of $r[n]$. As shown in Fig. 2, the digital error estimator block in the MNC feedback loop consists of 35 $s_k[n]$ residue estimators, each of which correlates $r[n]$ with nine shifted versions of one of the $s_k[n]$ sequences. Given that each $s_k[n]$ sequence is restricted to the values of -1, 0, and 1, each correlation is performed by multiplying $r[n]$ by a -1, 0, or 1 during the nth 600-MHz clock cycle. The result is multiplied by a small loop gain constant, $K = 6 \cdot 10^{-7}$, and accumulated. As proven in [16], the feedback loop causes the accumulator outputs to increase or decrease as necessary for $y_c(t)$ to well-approximate $e_{\mathrm{DAC}}(t)$ over the first Nyquist band.

Even though $e_{\mathrm{DAC}}(t)$ is a broadband waveform which depends on the main DAC's input sequence, $x[n]$, the $d_k(t)$ waveforms in (1) are periodic and independent of $x[n]$ [17]. They depend only on component mismatches and clock skew within the main DAC, so they do not change significantly over time. The MNC feedback loop causes the 315 accumulator outputs in the digital error estimator to converge to coefficients which depend only on the $d_k(t)$ waveforms. Thus, like the $d_k(t)$ waveforms, these coefficients depend only on the main DAC's component mismatches and clock skew. As proven in [16], the MNC technique converges to the same coefficients regardless of $x[n]$.

In principle, the MNC technique can perform foreground or background calibration with only minor differences, but in the prototype IC, it was limited to foreground calibration to simplify the project. During foreground calibration, the MNC feedback loop measures 315 coefficients described above. During normal DAC operation, the coefficients that were measured during foreground calibration continue to be used to generate $y_c(t)$, and thereby continue to cancel the error components.

III. Circuit Implementation Details

The IC was implemented in the GlobalFoundries 22-nm FDSOI process. In addition to the blocks shown in Figs. 1 and 2, the IC contains a direct digital synthesizer (DDS), a serial peripheral interface (SPI), a full ESD protection circuitry, and a miscellaneous control and test circuitry. As shown in Fig. 3, an off-chip 1:1 balun converts the IC's differential output signal to a non-differential signal which is used during testing to drive the 50-Ω input of a laboratory signal analyzer.

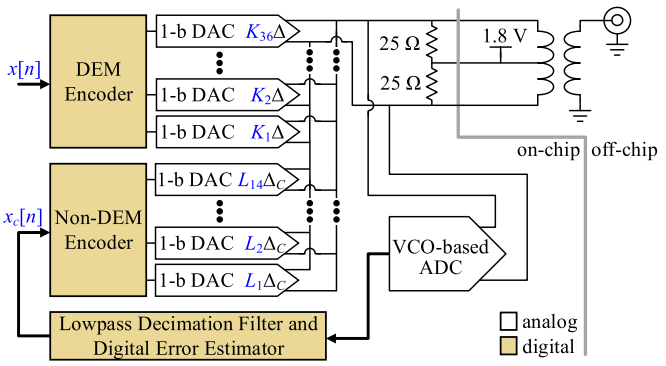

Fig. 3. Circuit-level block diagram of the prototype IC.

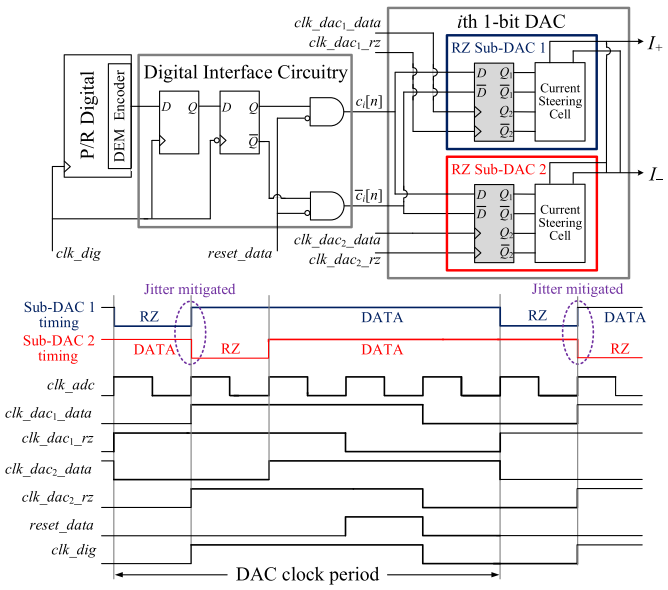

Fig. 4. High-level diagram and timing of the ith 1-bit DAC and digital interface.

A. Main DAC

The 14-bit main DAC consists of the DEM encoder and the subsequent 36 current-steering 1-bit DACs shown in Fig. 3. The DEM encoder has the segmented tree-structure form presented in [5]. It converts the 14-bit $x[n]$ sequence into 36 1-bit sequences, each of which drives a 1-bit DAC with weight K_i. For $i = 1, 2, \ldots, 20$, the values of K_i are 1, 1, 2, 2, 4, 4, $\ldots$, 512, 512, respectively, and for $i = 21, 22, \ldots, 36$, each K_i has a value of 1024. The main DAC's minimum current step averaged over a 600-MHz clock interval, Δ, is 1.56 μA.

Non-return-to-zero (NRZ) 1-bit DACs are a common design choice for current-steering DACs. In the context of the main DAC, an ideal ith NRZ 1-bit DAC would steer $K_i\,\Delta$ amperes of current to either its top output or its bottom output during the nth clock period depending on whether its input bit during that clock period is high or low, respectively. Unfortunately, inevitable asymmetries within any practical NRZ 1-bit DAC in conjunction with parasitic capacitances cause the 1-bit DAC's output waveform to depend nonlinearly on its input bit during at least one prior clock period in addition to that of the current clock period. The resulting ISI causes even DACs that incorporate DEM to introduce harmonic distortion [17].[1]

To circumvent this problem, the IC incorporates return-to-zero (RZ) 1-bit DACs, each of which is reset to a data-independent state every clock period to make its output waveform independent of its input sequence during prior clock periods. In principle, this eliminates ISI provided all analog and digital circuit blocks that make up the 1-bit DACs and that control them are fully reset each period. However, conventional RZ 1-bit DACs are more sensitive to clock jitter than their NRZ counterparts. As explained in the remainder of this section, various new circuit techniques are implemented in the IC to mitigate this issue while ensuring that ISI does not limit performance.

Fig. 4 shows the high-level structure and timing of each 1-bit DAC and its interface to the automatically placed and routed (P/R) digital block. Each 1-bit DAC is implemented as a parallel combination of two current-steering RZ 1-bit sub-DACs to mitigate the effect of clock jitter as explained shortly. The sub-DACs each operate on the same input bit sequence, and their outputs are connected so their output currents add. Each is reset for 20% of the clock period and generates output current for 80% of the clock period.[2] The only difference between the two sub-DACs is that they are reset at different times: sub-DAC 1 is reset during the first 20% of each clock period and sub-DAC 2 is reset during the second 20% of each clock period, as shown in Fig. 4. The 3-GHz ADC clock is used to generate the timing signals necessary to reset the RZ 1-bit sub-DACs. Error from mismatches and clock skew between the sub-DACs are cancelled by the MNC technique so they are not a significant issue in this design.

The average output current magnitude from the ith 1-bit DAC is $I_i = K_i\,\Delta$, so each of the two RZ sub-DACs has an output current magnitude of $0.625I_i$ during its 80% data phase. A single RZ 1-bit DAC with an 80% data phase output current magnitude of $1.25I_i$ or a single NRZ 1-bit DAC with an output current magnitude of I_i are each comparable alternative 1-bit DACs in that they too have average output current magnitudes of I_i. Of these comparable alternatives, the single RZ 1-bit DAC is significantly more sensitive to clock jitter than the single NRZ 1-bit DAC, because the former has two output current transitions at each clock period whereas the latter has at most one output current transition at each clock period and no transition if the input bit remains unchanged.

The timing of the 1-bit DAC in Fig. 4 is such that each rising edge of output current from sub-DAC 1 aligns with a falling edge of output current from sub-DAC 2. The sub-DACs share most of their timing circuitry, so their jitter is highly correlated. Hence, most of the error from clock jitter at the aligned edges cancels when the present and prior 1-bit DAC input bits are equal and add in amplitude otherwise. It follows that the error from jitter introduced by the pairs of aligned edges has the same form as the total error from jitter of the comparable

[1]For example, when the 1-bit DACs are configured to run in the NRZ mode (via a debug feature of the IC), the measured SFDR drops by 10 dB.

[2]The commonly used alternative of interlacing 50% RZ sub-DACs was not used here because of its high current consumptions [18].

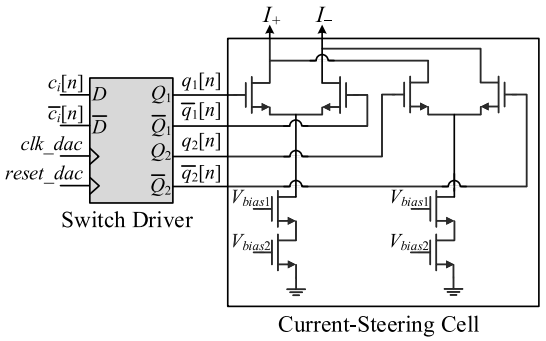

Fig. 5. Circuit diagram of the ith RZ 1-bit sub-DAC.

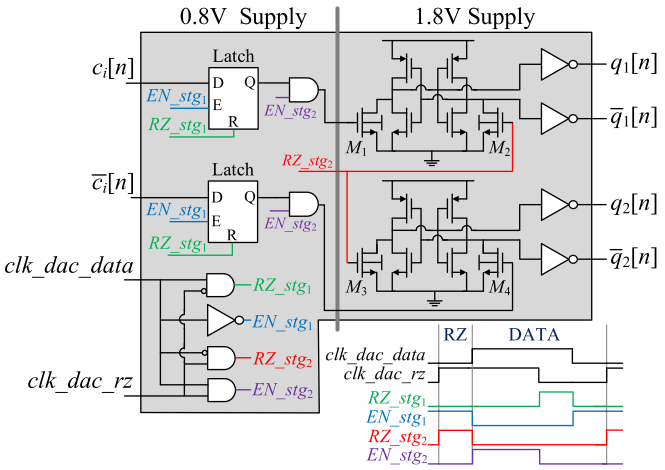

Fig. 6. Circuit diagram of the ith 1-bit DAC's switch driver.

single NRZ 1-bit DAC, but with $|20\log(0.625)| = 4$ dB less power. Each of the non-aligned edges has half the transition magnitude of each edge from the single comparable RZ 1-bit DAC, so the combined error from clock jitter introduced by the two non-aligned sub-DAC edges has the same form as that of the single comparable RZ 1-bit DAC, but with 6-dB less power. Hence, the error from jitter of the 1-bit DAC of Fig. 4 contains a component similar to that from an NRZ 1-bit DAC and a component similar to that from an RZ 1-bit DAC. As the former can be much smaller than the latter for broadband input sequences, it follows that the total error from jitter is up to 6 dB lower than that of the comparable single RZ 1-bit DAC.

As shown in Fig. 5, each sub-DAC's current-steering cell consists of two cascode current sources, each of which is steered to one of the two sub-DAC outputs by a differential pair controlled by the switch driver. During the data phase, the differential pairs steer both currents to the I_+ output if the input bit, $c_i[n]$, is high and to the I_- output if $c_i[n]$ is low. During the RZ phase, they steer the currents to opposite outputs so that the differential output current is zero. In contrast to a conventional RZ 1-bit DAC, which steers a single cascode current source to one of the two outputs during the data phase and to a dummy load during the RZ phase, the common-mode output current does not change during the RZ phase so unwanted large output slewing transients are avoided. Simulations indicate that the largest-weight 1-bit DACs have a minimum output impedance of 30 kΩ across the DAC's signal band, which is sufficient to prevent input code-dependent impedance variations from limiting performance.

The current switches in the 1-bit DAC of Fig. 4 steer a quarter of the current and, hence, have a quarter the size of those in a comparable single RZ 1-bit DAC, but there are four times as many of them. Consequently, the power and area consumed by the 1-bit DAC of Fig. 4 are similar to those of a comparable single RZ 1-bit DAC.

In addition to controlling the current-steering cell as described earlier, the switch driver converts the input sequence's 0.8-V power supply domain to the current-steering cell's 1.8-V power supply domain, and its design ensures data-independent switching current. As shown in Fig. 6, the switch driver circuit consists of separate signal paths for the complementary input bit sequences $c_i[n]$ and $\bar{c}_i[n]$, each of which consists of first and second latch stages that operate from 0.8- and 1.8-V power supplies, respectively. The latches in both stages are briefly reset at each DAC clock period, so the two-path design ensures that the same numbers of positive-going and negative-going logic transitions occur at each DAC clock period regardless of $c_i[n]$. This ensures that the current drawn by the switch driver is data-independent, thereby preventing data-dependent supply modulation which would be a source of ISI and nonlinear distortion.

The interface circuitry shown in Fig. 4 generates retimed complementary versions of the DEM encoder's ith output bit and includes an additional ISI-mitigation technique. It resets the complementary outputs to zero just prior to updating them with their next data values so as to mitigate ISI that would otherwise result from data-dependent coupling from the digital-to-analog supply domains.

As described in [5], the DEM encoder consists of 35 digital switching blocks, each of which is associated with one of the terms in (1). To ensure that the $s_k[n]$ sequences in (1) have the necessary statistical properties, each of the 35 switching blocks is driven by one of the 35 pseudo-random bits that are designed to well-approximate random processes which take on values of 0 and 1 with equal probability, are white, and are uncorrelated with each other and with the main DAC's input sequence. An on-chip 36-bit linear feedback shift register modified as described in [19] generates 144 f_s-rate random bit sequences in parallel, a subset of which are used as the 35 pseudo-random bits. The subset was chosen so as to minimize cross correlations among the 35 sequences as determined by behavioral simulation of the 144-bit random sequence generator.

B. Correction DAC

Behavioral simulations performed during the design phase suggested that the correction DAC's input sequence can be quantized to have the same step size as the main DAC's input sequence without the quantization error degrading overall performance. To provide additional margin, though, the correction

DAC's input sequence is instead quantized to have a step-size equal to a quarter that of the main DAC's input sequence.

Transistor-level simulations were then performed to determine the number of correction DAC bits required to accommodate the maximum expected magnitude of the digital error estimator output, which mainly depends on $e_{\mathrm{DAC}}[n]$. First, Monte Carlo simulations were performed to estimate the standard deviations of the various transistor parameters within the main DAC's 1-bit DACs caused by mismatches. Gaussian-distributed transistor mismatches were then generated with double these standard deviations to provide margin in case of a model error and used for subsequent transistor-level simulations. The simulations consisted of transistor-level 1-bit DACs with the Gaussian-distributed component mismatches manually inserted and with the remaining portion of the system implemented as Verilog-AMS blocks. These simulations indicated that a 9-bit correction DAC is more than sufficient to provide the necessary input range.

Hence, the correction DAC was designed to have 9 bits of resolution and a step size, Δ_C, equal to a quarter that of the main DAC, i.e., 0.39 μA. It consists of the non-DEM encoder and the subsequent 14 current-steering 1-bit DACs shown in Fig. 3. The non-DEM encoder converts the correction DAC's 9-bit digital input sequence into 14 1-bit sequences, each of which drives a 1-bit DAC with weight L_i. For $i = 1$, 2, 3, and 4, the values of L_i are 1, 2, 4, and 8, respectively, for $i = 5$, 6, and 7, each L_i has a value of 16, and for $i = 8, 9, \ldots, 14$, each L_i has a value of 64. The 1-bit DACs are identical to those of the main DAC, except without the bottom sub-DAC shown in Fig. 4.

Results from transistor-level simulations similar to those described above were used to size the correction DAC's transistors large enough that component mismatches and clock skew do not significantly degrade performance. The simulations indicated that the number of the correction DAC's 1-bit DACs and their step sizes are small enough that this could be achieved without applying DEM or calibration to the correction DAC.

C. VCO-Based ADC

It was explained heuristically in [16], but not proven, that the MNC technique is highly insensitive to ADC nonlinearity and noise. An objective of this project is to provide experimental support of this claim. The implemented ADC does not include calibration or special linearization techniques, so it is quite nonlinear: circuit simulations indicate that its second, third, and fourth output harmonics are -26, -47, and -64 dBc, respectively, for a full-scale sinusoidal input. Furthermore, it has only the first-order quantization noise shaping and an oversampling ratio of only 5, so its noise floor is high. Nevertheless, the experimental results presented in Section IV suggest that the ADC's error negligibly affects the MNC coefficients.

The ADC requirements are even further relaxed during foreground calibration, because in this case, the ADC's input range needs only to be a fraction of the main DAC's full-scale output range. Specifically, the main DAC's input during foreground calibration is toggled back and forth between -2389.5Δ and -2388.5Δ. In principle, any other input sequence could have been used, but this choice has the benefit of a very small dynamic range and it ensures rapid MNC loop convergence because it results in $s_k[n]$ sequences with a low percentage of zero values. With this choice, the ADC's differential input range of only 20 mV is sufficient to accommodate the maximum expected error from component mismatches and clock skew.

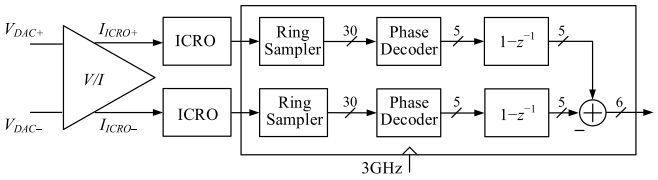

Fig. 7. Block diagram of the VCO-based ADC.

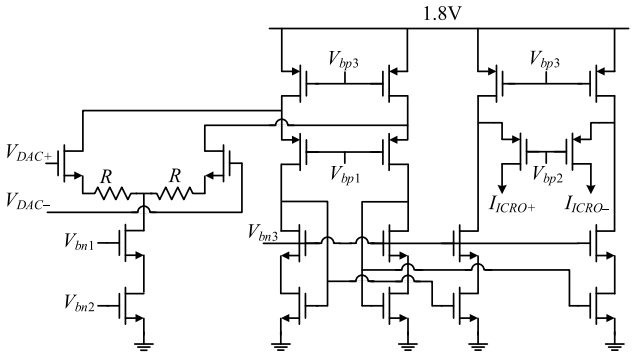

Fig. 8. Circuit diagram of the V/I converter.

A strict requirement, however, is that the digital error estimator input must contain negligible aliased power from outside the DAC's first Nyquist band. This is why an oversampling ADC is required, which is the MNC technique's primary downside. A VCO-based ADC is used in the IC because its inherent low-pass sinc filtering helps suppress the input signal above the DAC's first Nyquist band [20], which made it possible to use the relatively low oversampling ratio of 5. Also its design is particularly simple given that the MNC technique's insensitivity to nonlinearity makes ADC calibration or other linearization techniques unnecessary.

As shown in Fig. 7, the VCO-based ADC includes a differential voltage-to-current (V/I) converter, each output of which is followed by a 15-element pseudo-differential current-controlled ring oscillator (ICRO), a ring sampler, a phase decoder, and a $1–z^{-1}$ digital differentiator block. The high-level structure is similar to that presented in [20], except it consists of one instead of two signal paths, and it does not include dither or digital calibration because of the relaxed linearity and noise requirements.

The V/I converter (Fig. 8) generates currents $I_{\mathrm{ICRO}+}$ and $I_{\mathrm{ICRO}-}$ that drive the ICROs. As in [20], each ICRO consists of two pseudo-differential rings, each made up of 15 current-starved inverters. The V/I converter's input common-mode voltage is that of the IC's output signal, i.e., 1.8 V, and its common-mode output current is 1 mA. The two pMOS

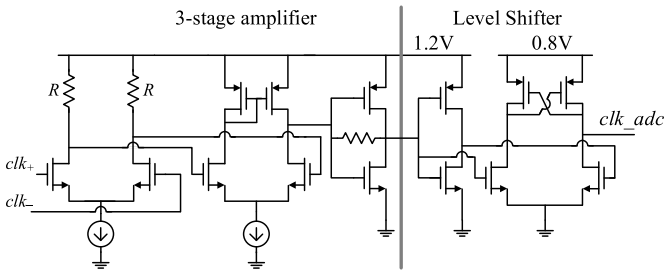

Fig. 9. Simplified diagram of the 3-GHz portion of the clock generator.

cascode bias voltages, V_{bp1} and V_{bp2}, are generated separately to reduce kick-back from the second stage to the first stage, and V_{bp2} is set to the 1.8 V during start-up while the other V/I converter nodes settle to protect the ICRO's thin-oxide devices from start-up transients. The V/I converter's dc gain is programmable but was set to its nominal value of 40 mS during testing. Its −3-dB bandwidth is slightly above the Nyquist frequency of the DAC.

The ring sampler, phase decoder, and $1 - z^{-1}$ block are similar to those described in [20]. They are not implemented as part of the P/R digital block because their data rate is 3 GHz and the P/R digital block is clocked at 600 MHz. The decimation filter is implemented in the P/R digital block, so its input data must have a 600-MHz sample rate. This is achieved by a digital interface circuit close to the ADC, which parallelizes the six 30-Gb/s ADC output lines to thirty 600-Mb/s lines.

D. Clock Generator

The IC is externally clocked by a single 3-GHz differential clock signal, from which the on-chip clock generator derives all the IC's internal clocks. The clock generator consists of the three-stage differential to single-ended amplifier and the 1.2- to 0.8-V level shifter shown in Fig. 9, followed by a clock divider that generates several 600-MHz clock signals, including those shown in Fig. 4. The amplifier operates from a 1.2-V supply and generates a nearly rail-to-rail squared-up version of the 3-GHz clock. The third stage is a transimpedance amplifier which provides a signal-dependent load to the second stage that limits the second-stage's swing sufficiently to prevent its transistors from entering triode operation. The level shifter generates the ADC's 3-GHz clock signal which is also the input to the clock divider.

To achieve the post-cancellation DAC noise performance target, the main DAC's critical 600-MHz clock paths must have rms jitter values of less than 80 fs. The clock generator was designed such that the simulated rms jitter values of these clock paths are below 50 fs to leave margin. The noise performance of the three-stage amplifier is the most critical component of these clock paths. Accordingly, the amplifier dissipates approximately 80% of the clock generator's total power dissipation.

E. P/R Digital Block

The P/R digital block contains the main DAC's DEM encoder, the correction DAC's non-DEM encoder, the low-pass decimation filter, the MNC digital error estimator, the DDS, the SPI, a pseudo-random sequence generator block, and the miscellaneous control and test logic. It consists of approximately 170 000 standard logic cells, occupies an area of 700 μm × 250 μm, and operates from a 0.8-V digital power supply. All registers except those in the SPI are clocked at 600 MHz.

The DDS provides the main DAC's 14-bit input sequence. It is capable of generating one-tone and two-tone test signals with frequencies at arbitrary integer multiples of 600/512 MHz and amplitudes of 0, −6, and −12 dBFS. The DDS internally generates an 18-bit version of the desired sequence and performs dithered requantization to obtain the final 14-bit sequence to suppress spurious tones in the quantization error.

The low-pass decimation filter is implemented as a 33-tap digital poly-phase finite impulse response (FIR) filter [21]. Dithered requantization is subsequently performed to reduce its 16-bit output sequence to a 4-bit sequence prior to the digital error estimator to save area.

F. Mixed-Signal Isolation and Process-Specific Details

The FDSOI process provides good isolation of the IC's transistors from substrate noise. Additionally, various measures were applied to reduce coupling of digital noise in sensitive analog circuitry. The P/R digital block is surrounded by a 2-nF ring of on-chip MOS power supply decoupling capacitors and substrate connections and is separated from the analog circuit blocks by a 250-μm BFMOAT isolation region with reduced substrate doping. All analog transistors reside in triple N-wells, and the analog power supplies are each decoupled with 200-pF on-chip MOS capacitors. On-chip ground planes are used to shield critical clock signals, and the clock generator is placed as far as possible from the P/R digital block. Multiple parallel package bond wires are used to reduce the inductance of critical power supplies.

Several blocks within the IC take advantage of the FDSOI IC technology. The back gates of all 0.8-V pMOS transistors in the P/R digital logic, 1-bit DACs, ADC, and interface circuitry are tied to ground to reduce threshold voltages and increase speed. The back gates of the pull-down nMOS transistors in the second latch stages of the 1-bit DAC switch drivers are tied to 1.8 V to increase pull-down strength.

IV. Measurement Results

Fig. 10 shows an annotated IC die photograph. The die dimensions are 2.5 mm × 2 mm, and the IC's active area is 1.15 mm^2. The IC is packed in a 36-pin QFN package with an exposed paddle to which all the IC's ground pads are down-bonded. The package is mounted to a printed circuit board (PCB) via an Ironwood GHz elastomer QFN socket.

The PCB includes a clock input and DAC output signal conditioning circuitry, low-noise LDO regulators, and a microcontroller for SPI communication. A Rohde & Schwarz SMA100A signal generator was used to provide a single-ended 3-GHz clock signal which was passively bandpass filtered to suppress noise and harmonics prior to the PCB. The clock signal is converted to differential form by a PCB balun, and the

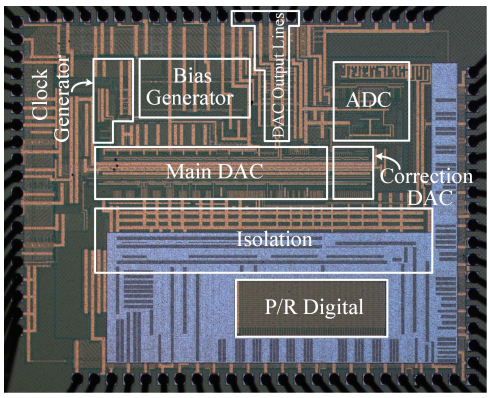

Fig. 10. Die photograph.

outputs of which are ac coupled to 50-Ω impedance-controlled PCB traces. Series 5-Ω resistors between the clock traces and the IC's input clock pins mitigate clock ringing associated with the package bond wire inductance. A PCB balun (Fig. 3) provides a non-differential version of the DAC output, which was measured with a Keysight N9030B PXA signal analyzer.

To fully characterize continuous-time DAC performance, it is necessary to measure both noise and nonlinear distortion over the signal band relative to the signal power. Yet many DAC publications report limited or no noise measurements, and most report measurements of SFDR—the dB power difference between the DAC output's fundamental tone and its largest spurious tone for a full-scale sinusoidal input signal—as the sole means of quantifying nonlinear distortion. Unfortunately, SFDR can be misleading because the number of spurious tones changes with input frequency, and as this number increases, the SFDR tends to decrease even when the total distortion power remains relatively constant. To avoid these limitations, the IC was extensively tested to measure several values of not only SFDR but also SNDR, noise spectral density (NSD), and noise and distortion spectral density (NDSD) as described below.

The signal band was taken to extend from 1 to 265 MHz. The dc to 1-MHz band was excluded because it is suppressed by the output balun, and the upper 35 MHz of the first Nyquist band was excluded because aliasing from the decimation filter's transition band reduces MNC accuracy over this band. This latter exclusion band represents a design tradeoff. It can be reduced by increasing the digital filter's complexity and, therefore, power consumption. Alternatively, the filter complexity can be kept relatively low, e.g., in the current design it is just a 33-tap FIR filter, but the DAC's sample rate can be increased slightly to compensate for the exclusion band. In lieu of other constraints, the best choice, in practice, is that which minimizes power dissipation for a given process.

Each measurement was made with and without DEM enabled during normal DAC operation. The main DAC's error waveform is given by (1) even when DEM is disabled, but in this case, the $s_k[n]$ sequences are nonlinear deterministic functions of $x[n]$. For correct MNC coefficient convergence, the $s_k[n]$ sequences must be uncorrelated with each other and with $x[n]$, so DEM is required during foreground calibration.

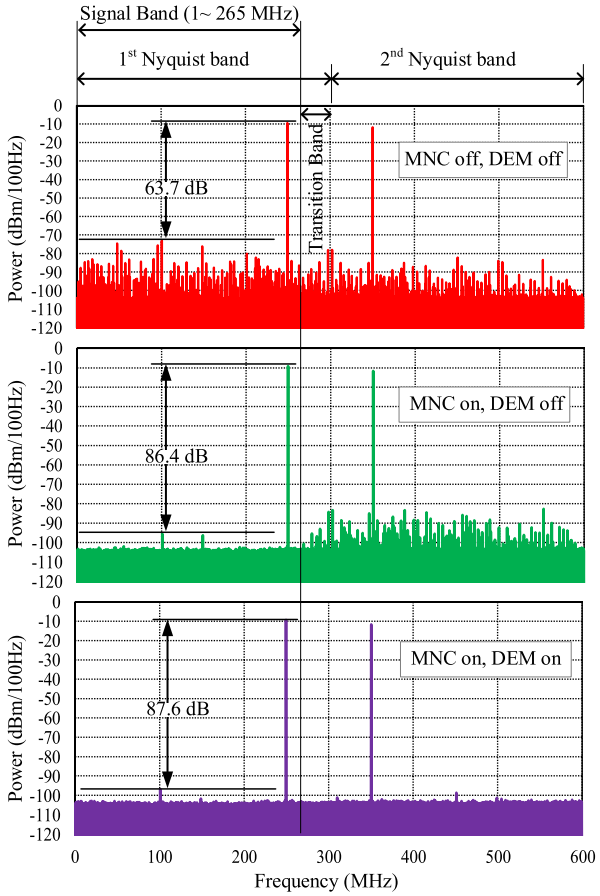

Fig. 11. Measured output spectra for a full-scale 249.6-MHz input signal (the MNC off, DEM on plot is not shown because the signal analyzer's noise floor limits the measurements to the point that it is nearly identical to the MNC on, and DEM on plot).

However, once the coefficients have been measured, DEM is optional; error cancellation works regardless of whether DEM is enabled or disabled. With MNC enabled, DEM offers a tradeoff during normal DAC operation: it slightly increases the signal-band noise floor and overall power dissipation, but it slightly reduces harmonic distortion over the signal band and greatly reduces it outside of the signal band.

Fig. 11 shows representative measured output power spectra over the first two Nyquist bands for a full-scale 249.6-MHz single-tone DAC input sequence. The data were measured with a signal analyzer resolution bandwidth of 100 Hz, exported to files, and plotted via software for improved readability. Without MNC and DEM, the signal-band SFDR is 63.7 dB, with MNC but without DEM, the signal-band SFDR improves to 86.4 dB, and with MNC and DEM, the signal-band SFDR slightly improves further to 87.6 dB. As shown in Fig. 12, these SFDR results are representative of those measured for full-scale single-tone and two-tone input signals throughout the signal band.

The post-cancellation noise floor of the DAC is below that of the signal analyzer, so to measure the DAC's noise floor, it was necessary to use the signal analyzer's internal preamplifier in addition to its noise floor extension feature. To avoid

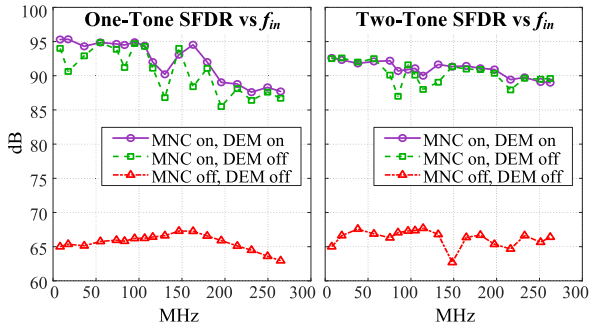

Fig. 12. Measured SFDR versus frequency for one-tone input signals and two-tone input signals separated by 3.52 MHz.

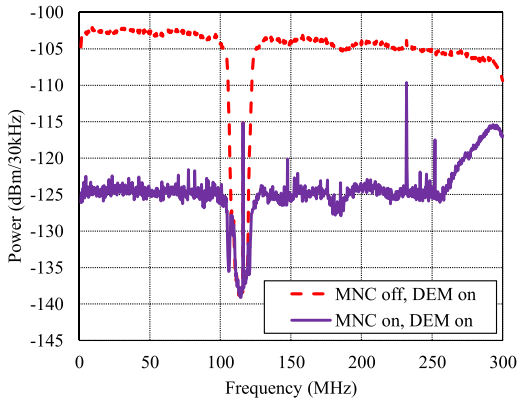

Fig. 13. Measured output noise and distortion spectra.

TABLE I
NSD/NDSD/SNDR MEASURED OVER SIGNAL BAND

	f_{in} (MHz)	NSD (dBc/Hz)		NDSD (dBc/Hz)		SNDR (dB)	
		DEM off	DEM on	DEM off	DEM on	DEM off	DEM on
MNC off	50.4	−164.2	−141.2	−143.9	−141.1	59.7	56.9
	116	−163.3	−140.9	−142.6	−140.7	58.4	56.5
	179.3	−162.4	−139.9	−142.6	−139.8	58.4	55.6
MNC on	50.4	−164.4	−162.4	−162.8	−162.1	78.6	77.9
	116	−163.5	−161.9	−162.1	−161.5	77.9	77.3
	179.3	−162.5	−161.1	−161.0	−160.5	76.8	76.3

TABLE II
NSD/NDSD/SNDR MEASURED OVER THE SECOND NYQUIST BAND

	NSD (dBc/Hz)		NDSD (dBc/Hz)		SNDR (dB)	
	DEM off	DEM on	DEM off	DEM on	DEM off	DEM on
MNC off	−162.5	−145.5	−148.8	−145.5	64.0	60.7
MNC on	−162.6	−148.1	−152.8	−148.0	68.0	63.2

TABLE III
NSD/NDSD/SNDR MEASURED OVER THE THIRD NYQUIST BAND

	NSD (dBc/Hz)		NDSD (dBc/Hz)		SNDR (dB)	
	DEM off	DEM on	DEM off	DEM on	DEM off	DEM on
MNC off	−162.7	−157.5	−158.0	−156.4	73.2	71.6
MNC on	−162.8	−158.0	−158.6	−156.9	73.8	72.1

being limited by the preamplifier's nonlinearity, it was further necessary to use passive notch and low-pass filters prior to the signal analyzer to suppress the signal component of the DAC's output waveform and limit the spectrum to the first Nyquist band.

Fig. 13 shows representative DAC output power spectra measured with the passive filters and preamplification described above for a 116-MHz full-scale sinusoidal input signal. The data were measured with the signal analyzer's resolution bandwidth set to 30 kHz, the number of frequency trace points set to 1001, and the rms average detector enabled. As indicated in the figure, enabling MNC reduced the noise by over 20 dB across the 265-MHz signal band.

Table I presents the values of SNDR, NDSD, and NSD calculated from measured power spectra for full-scale single-tone input signals with the frequencies of 50.4, 116, and 179.3 MHz. The values were calculated from power spectrum plots like those shown in Fig. 13. Each of the three input frequencies was chosen such that the corresponding notch filter did not hide significant spurious tones, and for each measurement, the DAC noise over the notch filter's 30-MHz stopband was estimated by extrapolation. For the SNDR and NDSD measurements, the total noise and distortion was calculated by integrating the measured power spectrum from 1 to 265 MHz and then adding the extrapolated noise over the 30-MHz notch filter stopband. Each NDSD value is this noise and distortion value divided by the integration bandwidth. Each NSD value is equal to the corresponding NDSD value minus the measured power of each non-negligible signal-band spurious tone.

Extensive noise measurements performed by the authors suggest that the DAC's noise floor is nearly independent of the input signal frequency. The slight drop in SNDR with frequency evident in Table I occurs mainly because of the roll-off imposed on the input signal by the 1-bit DAC hold operations. These slight drops with frequency also occur for the NDSD and NSD values in Table I, because the values are specified in units of dBc/Hz.

Although the MNC technique is designed to cancel error primarily over the main DAC's signal band, it typically provides some error cancellation outside of this band too. This is demonstrated by the data in Tables II and III, which show measured NSD, NDSD, and SNDR values over the second and third Nyquist bands with and without MNC for a 116-MHz full-scale sinusoidal input sequence. Notch filters were not available to suppress power outside of the first Nyquist band when measuring the data for Tables II and III, respectively. Therefore, although a notch filter centered at 116 MHz was applied to reduce the power of the signal applied to the signal analyzer, 8 dB of attenuation in conjunction with the preamplifier via the signal analyzer's mechanical attenuator was added to prevent the instrument's nonlinearity from limiting the measurements. This caused the signal analyzer's noise floor to slightly limit the measurements, so it is likely that MNC cancels more error than indicated in Tables II and III.

The reason that MNC provides some error suppression outside of the signal band is that it tends to cancel a significant portion of the static error over all Nyquist bands. A DAC's static error is caused by non-ideal deviations in the amplitudes of its output pulses, so it can be modeled as an input-referred discrete-time error sequence. Hence, each of the DAC's Nyquist bands contains a frequency-shifted replica of the first Nyquist band's static error filtered by the DAC's frequency roll-off. It follows that MNC cancels the static portion of the error from component mismatches over all Nyquist bands to the extent that the correction DAC's pulse shape matches that of the main DAC. In contrast, typical dynamic error bandwidths are much higher than the DAC's signal bandwidth, so the portion of the correction DAC's output that cancels dynamic error over the signal band has the potential to increase error at higher frequencies. Nevertheless, the increase is small because the dynamic error over the DAC's signal band tends to be relatively small and the correction DAC's frequency roll-off attenuates it further outside of the signal band.

The MNC coefficients measured during foreground calibration remain fixed during normal operation. This raises the question of how well MNC works across supply voltage and temperature variations. The analog blocks operate from three supply voltages with nominal values of 0.8, 1.2, and 1.8 V, respectively. After running foreground calibration at these nominal supply values, the performance of the DAC during normal operation with MNC and DEM enabled was measured with the three supply voltages first set to 0.7, 1.1, and 1.7 V, respectively, and then set to 0.9, 1.3, and 1.9 V, respectively. The worst case degradation observed in SNDR, NSD, and NDSD relative to the nominal case was 1 dB. Equipment was not available to perform measurements at different temperatures, but conservative circuit simulations suggest that changing the temperature between −30 °C and 100 °C after foreground calibration at 25 °C would degrade the SNDR by less than 4 dB. If the background version of MNC were implemented in addition to the foreground version, any temperature-dependent degradation would likely be negligible.

Measurements were also performed to assess the IC's ISI mitigation techniques. By enabling and disabling partial-interleaving and the interface and switch driver ISI mitigation techniques for various test conditions, it was determined that the techniques together prevent an SNDR degradation of about 1.7 dB, with the partial interleaving technique contributing roughly half of this benefit. Configuring the 1-bit DACs to operate in NRZ mode with DEM and MNC enabled reduced the measured SFDR by about 10 dB.

The IC includes a test feature that can be enabled to intentionally delay the clock signals that drive just two of the main DAC's 256-weight 1-bit DACs by approximately 25 ps. Letting MNC converge in foreground with this feature disabled and then enabling it during normal DAC operation with a 0-dBFS 116-MHz input signal caused the measured SNDR to degrade from 77.3 to 63.0 dB. Given that enabling the feature only introduces clock skew, this 14.3 dB of degradation must be entirely from dynamic mismatch error. Rerunning foreground calibration with the clock delays in place and applying the same 0-dBFS 116-MHz input signal during normal DAC operation caused the measured SNDR to improve to 76.8 dB. This provides experimental confirmation of the theoretical result presented in [16] that the MNC technique effectively cancels dynamic mismatch error.

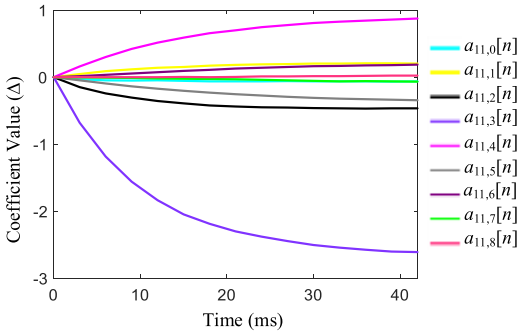

Fig. 14. Representative plot of measured coefficient values versus time.

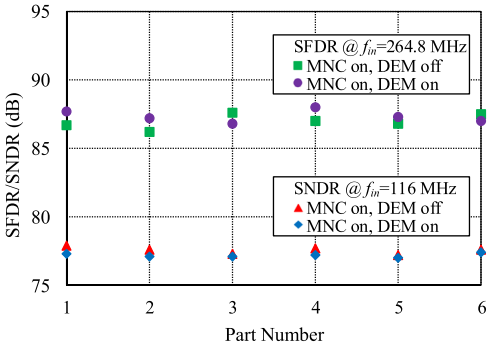

Fig. 15. Measured SFDR and SNDR values across six parts.

Fig. 14 shows a representative subset of the 315 MNC coefficient values versus time measured during foreground calibration. The values were obtained by periodically freezing MNC and reading the coefficients from the $s_{11}[n]$ residue estimator (Fig. 2) via the SPI during foreground calibration. The observed coefficient convergence rate is consistent with that predicted by the analysis presented in [16]. Increasing the MNC loop gain, K, reduces the convergence time at the expense of accuracy. For the measurements reported in this paper, the loop gain was set conservatively small. Additional measurements performed by the authors indicate that increasing K by a factor of 16 reduced the convergence time to 2.5 ms while degrading the SNDR by less than 0.5 dB.

All the measurements presented above were made from a single randomly selected copy of the IC. Fig. 15 shows representative SFDR and SNDR values measured from this and five other randomly selected copies of the IC with MNC enabled. As expected, with MNC enabled, the performance differences among the ICs are small: less than a dB for SNDR and less than 2 dB for SFDR.

Table IV summarizes the measured performance described above along with the available corresponding performance of previously published state-of-the-art DACs. Excluding the DAC presented in [15], the DAC reported in this paper achieves at least 7 dB better SFDR than the other DACs,

TABLE IV
PERFORMANCE TABLE AND COMPARISON TO PRIOR STATE-OF-THE-ART DACS

	This work		[9]	[10]	[7]	[11]	[8]	[15]	[13]	[14]
Process	22nm		65nm	65nm	40nm	130nm	140nm	16nm	20nm	65nm
Resolution (bit)	14		12	12	12	14	14	16	14	16
Sample Rate (MHz)	600		2000	1000	1600	500	200	6000	750	3000[5]
Full Scale (mA)	16[3]		16	16/20	16	16	20	40	2	Not Provided
Supply (V)	0.8/1.2/1.8		1.0/2.5	1.0/2.5	1.2	1.2/2.5	1.0/1.8	1.0/3.0	1.0/1.8	Not Provided
Power (mW)	182 (DEM off), 202 (DEM on)		681	430	40	299	270	350	21.1	800
Mismatch Mitigation	MNC (Fully-Integrated Static and Dynamic Calibration)		DEM/DWA and Off-chip Manual Calibration	DWA and Off-chip Manual Calibration	DEM	DRRZ	DMM	DEM and Static Calibration	R2R and Static Calibration	Static Calibration
Performance	DEM off	DEM on								
Worst SFDR[1] (dB)	85	87	78	78	72	74	79	88[4]	< 65	79
90 dB SFDR corner[2] (MHz)	116	180	< 20	< 20	Not Provided	Not Provided	Not Provided	Not Provided	Not Provided	< 70
NSD (dBc/Hz) @ f_{in} (MHz)	−164.4 @ 50.4 −163.5 @ 116 −162.5 @ 179.3	−162.4 @ 50.4 −161.9 @ 116 −161.1 @ 179.3	−160 @ 1	−162 @ 65	−147.6 @ 15 −139 @ 784	Not Provided	−161 @ 60	−165.5 @ 250	−155 @ 15	Not Provided
SNDR (dB) @ f_{in} (MHz)	78.6 @ 50.4 77.9 @ 116 76.8 @ 179.3	77.9 @ 50.4 77.3 @ 116 76.3 @ 179.3	Not Provided	Not Provided	58.6 @ 15 50 @ 784 (SNR Only)	60 @ 50 55 @ 175	Not Provided	Not Provided	Not Provided	Not Provided

[1] Worst single-tone SFDR reported for $f_{in} \leq 265$ MHz [2] Maximum f_{in} below which single-tone SFDR ≥ 90 dB [3] Includes both sub-DACs in Fig. 4
[4] Only one data point is reported for $f_{in} \leq 265$ MHz [5] Clock frequency used at which SFDR is measured

it achieves at least 12 dB better NSD than the other DACs that incorporate randomization to scramble mismatches (i.e., DEM and DRRZ) without calibration, and it achieves at least 3 dB better NSD than those of the remaining DACs. However, it does not outperform the DAC presented in [15]. As this DAC uses NRZ 1-bit DACs, DEM, and calibration that only addresses static error from component mismatches, its astonishingly good performance suggests that special circuit design and layout techniques not described in [15] must have been utilized to reduce ISI and dynamic mismatch error.

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