Multi-Rate DEM With Mismatch-Noise Cancellation for DCOs in Digital PLLs

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***Abstract*— Mismatches among frequency control elements in digitally-controlled oscillators can be a significant source of phase error in digital phase-locked loops (PLLs). This paper presents a multi-rate dynamic element matching technique and an adaptive mismatch-noise cancellation (MNC) technique that work together to address this problem. The two techniques operate in background during normal PLL operation, and the MNC technique has typical cold start convergence times of a few seconds.**

***Index Terms*— Delta-sigma modulation, digitally-controlled oscillator (DCO), digital calibration, dynamic element matching (DEM), mismatch-noise cancellation (MNC), digital phase-locked loop (PLL), spectral breathing.**

I. Introduction

HIGH-PERFORMANCE phase-locked loops (PLLs) are critical components in modern electronic communication systems. For example, in wireless transceivers they generate radio frequency local oscillator signals for up-conversion and down-conversion of transmitted and received signals, the phase error of which often limits overall transceiver performance.

Most PLLs incorporate either analog filters and voltage-controlled oscillators (VCOs) or digital filters and digitally-controlled oscillators (DCOs). The former are often called *analog PLLs* and the latter are often called *digital PLLs*. To date, analog PLLs have the best phase error performance, but digital PLLs have the lowest circuit area and are more compatible with highly-scaled CMOS IC technology. Thus, reducing phase error in digital PLLs has been the subject of intensive research and development for over a decade [1]–[49].

Nevertheless, frequency control element (FCE) mismatches in DCOs remain a significant source of phase error in high-performance digital PLLs [39]. This problem has only been addressed in prior work via an offline calibration technique that requires several minutes to complete [16], [18]. This paper presents a multi-rate dynamic element matching (DEM) technique and an adaptive mismatch-noise cancellation (MNC) technique that work together to address the problem. Both techniques run in background during normal PLL operation, and the MNC technique typically converges in a few seconds from a cold start.

The paper describes the proposed multi-rate DEM and MNC techniques in detail. Section II provides DCO background information. Section III discusses the effects of FCE mismatches on the DCO frequency. Section IV presents an error model for FCE mismatches. Section V presents the multi-rate DEM technique. Section VI presents the MNC technique. Section VII presents behavioral simulation results that support the analysis of the paper. The proposed techniques are described in the context of an example to simplify the explanations.

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II. Background Information

A DCO is an oscillator whose frequency is controlled by one or more FCEs, each of which is controlled by a 1-bit digital sequence. For instance, each FCE in an LC-based DCO contributes to the DCO's tank a capacitance that takes on one of two values depending on the state of the FCE's input bit. Changing the FCE's input bit increases or decreases the DCO frequency by a fixed frequency step.

The instantaneous frequency of a DCO is given by a fixed offset frequency plus $f_{\text{tune}}(t)$, where

$$f_{\text{tune}}(t) = \sum_{i=1}^{N_{\text{FCE}}} f_i(t), \tag{1}$$

N_{FCE} is the number of FCEs in the DCO, and $f_i(t)$ is the contribution of the ith FCE to the DCO frequency. Ideally,

$$f_i(t) = (b_i[m_t] - 1/2)\,\Delta_i, \tag{2}$$

where $b_i[m]$ is the FCE's input bit value (either 0 or 1) over the mth clock interval, $m_t = \lfloor f_{\text{FCE}} t \rfloor$, f_{FCE} is the clock-rate of the input bit, and Δ_i is the FCE's frequency step size.[1]

The DCO's input sequence, $d[n]$, represents the ideal value of $f_{\text{tune}}(t)$ over the nth clock interval. For example, suppose $d[n]$ is represented as a 16-bit two's complement code where the least significant bit (LSB) represents a DCO frequency step of Δ (e.g., $\Delta = 100$ Hz). Then

$$d[n] = \left(-2^{15} d_{15}[n] + \sum_{i=0}^{14} 2^i d_i[n]\right)\Delta, \tag{3}$$

where $d_i[n]$, for each $i = 0, 1, \ldots, 15$, is the value of the ith bit of the code (either 0 or 1) over the nth clock interval.

[1] By definition, m_t is the largest integer less than or equal to $f_{\text{FCE}} t$ at time t, so it is a continuous-time waveform. Hence, $b_i[m_t]$ is a continuous-time waveform even though $b_i[m]$ is a discrete-time sequence.

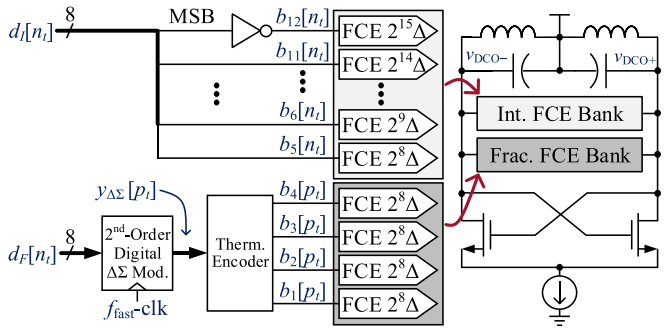

Fig. 1. Conventional frequency control technique for an LC-based DCO.

Ideally, $f_{\text{tune}}(t) = d[n_t]$, where $n_t = \lfloor f_{\text{in}} t \rfloor$ and f_{in} is the clock-rate of the DCO input. Equations (1)-(3) with $f_{\text{FCE}} = f_{\text{in}}$ imply that this can be achieved with a bank of 16 FCEs, where the ith FCE's frequency step size is $\Delta_i = 2^{i-1}\Delta$, $b_i[n] = d_{i-1}[n]$ for $i = 1, 2, \ldots, 15$, and $b_{16}[n] = 1 - d_{15}[n]$.

Unfortunately, in PLL applications that require low phase noise, such as local oscillator synthesis for cellular telephone transceivers, DCOs with minimum frequency steps of tens of Hz are required, but most existing FCEs have minimum frequency steps of tens of kHz or more [50], [51]. A common solution to this problem is described below for an example case in which $f_{\text{tune}}(t)$ needs to be controlled in steps of Δ, yet the smallest realizable FCE frequency step size is $\Delta_{\min} = 2^8\Delta$. In this case, the eight LSBs of $d[n]$ are said to represent the *fractional part* of $d[n]$ because they cause DCO frequency steps that are fractions of $\Delta_{\min}$, and the eight most significant bits (MSBs) of $d[n]$ are said to represent the *integer part* of $d[n]$ because they cause DCO frequency steps that are multiples of $\Delta_{\min}$.

The idea is to have two FCE banks: an *integer FCE bank* controlled by the integer part of $d[n]$, and a *fractional FCE bank* controlled by the output of an oversampling digital $\Delta\Sigma$ modulator driven by the fractional part of $d[n]$ [2]. The $\Delta\Sigma$ modulator's highpass-shaped quantization noise is lowpass filtered by the DCO, so provided the oversampling rate is sufficiently high, it negligibly contributes to the DCO's phase error.

Fig. 1 shows a specific example in the context of an LC-based DCO, where $p_t = \lfloor f_{\text{fast}} t \rfloor$, $f_{\text{fast}} \gg f_{\text{in}}$, and $d_I[n_t]$ and $d_F[n_t]$ are the integer and fractional parts of $d[n_t]$, respectively. The f_{fast}-clk signal is such that p_t changes synchronously with n_t, so that n_t can be written as a function of p_t, i.e.,

$$n_t = g(p_t). \tag{4}$$

In this example $g(p_t) = \lfloor (f_{\text{in}}/f_{\text{fast}})\, p_t \rfloor$, where $f_{\text{fast}}/f_{\text{in}}$ is an integer much greater than 1.

It follows from (3) that $d[n_t] = d_I[n_t] + d_F[n_t]$, where

$$d_I[n_t] = \left(-2^{15} d_{15}[n_t] + \sum_{i=8}^{14} 2^i d_i[n_t] \right) \Delta \tag{5}$$

and

$$d_F[n_t] = \Delta \sum_{i=0}^{7} 2^i d_i[n_t]. \tag{6}$$

As shown in Fig. 1, $d_F[n_t]$ is sampled at a rate of f_{fast} by a second-order digital $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator's output is a four-level sequence quantized to multiples of $\Delta_{\min}$ and can be written as

$$y_{\Delta\Sigma}[p_t] = d_F[n_t] + e_{\Delta\Sigma}[p_t], \tag{7}$$

where $e_{\Delta\Sigma}[p_t]$ is second-order highpass-shaped quantization noise plus any dither used within the $\Delta\Sigma$ modulator. A thermometer encoder maps $y_{\Delta\Sigma}[p_t]$ to a 4-bit thermometer code which drives a bank of four FCEs, each with a frequency step of $\Delta_{\min}$. It follows from (1), (2) and (7) that the contribution of the fractional FCE bank to the DCO frequency, $f_F(t)$, is

$$f_F(t) = \sum_{i=1}^{4} f_i(t) = d_F[n_t] + e_{\Delta\Sigma}[p_t]. \tag{8}$$

The integer FCE bank is directly driven by $d_I[n_t]$. Specifically, the ith FCE, for $i = 5, 6, \ldots, 11$, has input $b_i[n_t] = d_{i+3}[n_t]$ and frequency step size $\Delta_i = 2^{i+3}\Delta$, and the 12^{th} FCE has input $b_{12}[n_t] = 1 - d_{15}[n_t]$ and frequency step size $\Delta_{12} = 2^{15}\Delta$. It follows from (1), (2) and (5) that the contribution of the integer FCE bank to the DCO frequency, $f_I(t)$, is

$$f_I(t) = \sum_{i=5}^{12} f_i(t) = d_I[n_t], \tag{9}$$

where a constant additive term has been omitted.

The contribution of the two FCE banks to the DCO frequency is $f_{\text{tune}}(t) = f_I(t) + f_F(t)$, so (8) and (9) imply that

$$f_{\text{tune}}(t) = d[n_t] + e_{\Delta\Sigma}[p_t]. \tag{10}$$

Accordingly, $e_{\Delta\Sigma}[p_t]$ causes DCO frequency error. The DCO's phase error is the integral of its frequency error, so as mentioned above, a lowpass-filtered version of $e_{\Delta\Sigma}[p_t]$ appears as a component of the DCO's phase error. Given that $e_{\Delta\Sigma}[p_t]$ has a highpass-shaped spectrum that peaks at $f_{\text{fast}}/2$, its contribution to the DCO's phase error can be made negligible relative to other sources of phase error if f_{fast} is large enough [2], [11], [50].

III. Effects of FCE Mismatches

The FCEs in the previous example are ideal. Unfortunately, non-ideal circuit behavior causes $f_i(t)$ to deviate from (2). For example, suppose for now that $f_i(t)$ is modeled as ideal except for a static gain error given by α_i, i.e.,

$$f_i(t) = (b_i[m_t] - 1/2)\, \alpha_i \Delta_i. \tag{11}$$

Ideally, $\alpha_i = 1$ for $i = 1, 2, \ldots, N_{\text{FCE}}$, but inevitable component mismatches introduced during fabrication cause α_i to deviate from 1.

Repeating the analysis for the example in Fig. 1 with (11) in place of (2) gives

$$f_{\text{tune}}(t) = \alpha_F\, f_{\text{tune-ideal}}(t) + e_F(t) + e_I(t) + (\alpha_I - \alpha_F)\, d_I[n_t], \tag{12}$$

where $f_{\text{tune-ideal}}(t)$ is given by the right side of (10), α_F and α_I are the averages of α_i for $i = 1, 2, 3, 4$ and $i = 5, 6, \ldots, 12$, respectively,

$$e_F(t) = \sum_{i=1}^{4} (\alpha_i - \alpha_F)\,(b_i[p_t] - 1/2)\,\Delta_{\min} \tag{13}$$

and

$$e_I(t) = \sum_{i=5}^{12} (\alpha_i - \alpha_I)\,(b_i[n_t] - 1/2)\,\Delta_i. \tag{14}$$

Hence, the FCE static gain errors introduce a gain factor, α_F, and three additive error terms to $f_{\text{tune}}(t)$. The α_F gain factor does not significantly degrade performance in typical PLLs. In contrast, as explained next, the three additive error terms in (12) tend to cause spurious tones and increase phase error in PLLs because they are nonlinear functions of $d[n_t]$.

The individual bits of $d[n]$, i.e., $d_i[n]$, for each $i = 0, 1, \ldots, 15$, each depend on $d[n]$ but are restricted to values of 0 and 1. Hence, each $d_i[n]$ is a nonlinear function of $d[n]$. Nevertheless, they can be combined as in (3) to yield $d[n]$, which implies that multiplying $d_0[n]$, $d_1[n]$, …, $d_{14}[n]$, and $d_{15}[n]$ by 2^0, 2^1, …, 2^{14}, and -2^{15}, respectively, and adding the results causes the nonlinear components from the individual bits to cancel each other. Any deviation from a set of scale factors proportional to those mentioned above prevents full cancellation of the nonlinear components. It can be verified from (5), (13) and (14) that $e_F(t)$, $e_I(t)$, and $(\alpha_I - \alpha_F)d_I[n_t]$ are each a function of a subset of the individual bits of $d[n_t]$, so they are nonlinear functions of $d[n_t]$.

A partial solution to this problem is to replace the thermometer encoder in Fig. 1 with a mismatch-shaping DEM encoder [52]. Doing so would cause $e_F(t)$ to be replaced by highpass-shaped noise that is free of nonlinear distortion and is uncorrelated with $d[n_t]$, so it would be suppressed by the DCO like the $\Delta\Sigma$ quantization noise. Similarly, the integer FCE bank could be modified to accommodate a mismatch-shaping DEM encoder clocked at a rate of f_{in}, which would cause $e_I(t)$ to be replaced by shaped noise that is free of nonlinear distortion and is uncorrelated with $d[n_t]$. However, $f_{\text{in}} \ll f_{\text{fast}}$, so less of the shaped noise would be suppressed by the DCO. Unfortunately, DEM as described above would not help prevent the last term in (12) from introducing nonlinear distortion because $d_I[n_t]$ is a non-linear function of $d[n_t]$.

As demonstrated in [39], the last two terms in (12) increase the phase error in a PLL unless $d_I[n_t]$ remains constant once the PLL is locked. In most published digital PLLs $d[n]$ varies by much less than $\Delta_{\min}$ when the PLL is locked, and measured results are usually presented for PLL frequencies at which $d_I[n_t]$ does not change during the measurement interval. This renders the last two terms in (12) constant, so they do not contribute phase error. Unfortunately, this is not a viable option in practice because DCO center frequency drift caused by flicker noise, voltage and temperature variations, and pulling from external interference cause $d[n_t]$ to vary by far more than $\Delta_{\min}$ over time. For instance, measurement results indicate that the frequency of the DCO presented in [39] varies by about -200 kHz/°C, which corresponds to $\sim 7\Delta_{\min}$ per degree Celsius. In practice, this causes the digital PLL's phase noise to increase drastically from time to time as $d[n_t]$ slowly drifts past integer multiples of $\Delta_{\min}$. This issue is sometimes called "spectral breathing" because the phase noise spectrum, as viewed on laboratory measurement equipment, appears to swell up every now and then as if it is taking deep breaths. During these "breaths" the PLL's performance is extremely degraded. Furthermore, when the PLL is used to generate phase or frequency modulated signals, such as a GFSK signal for a Bluetooth transmitter, $d[n_t]$ typically varies by more than $\Delta_{\min}$, so there are no periods between "breaths" during which the phase noise performance is good.

To address this problem, a single bank of FCEs driven by a $\Delta\Sigma$ modulator and a mismatch-shaping DEM encoder could be used, where the $\Delta\Sigma$ modulator oversamples $d[n_t]$ instead of just $d_F[n_t]$. The DEM encoder would cause any mismatches among the FCEs to contribute shaped noise instead of nonlinear distortion, and the oversampling would ensure that most of the noise is suppressed by the DCO. Unfortunately, high oversampling ratios would be required in practice, which makes this solution impractical because of the associated high power consumption.

In the remainder of the paper, a new multi-rate DEM technique and an MNC technique that work together within a PLL to solve the problems that arise from FCE mismatches are presented. As in Fig. 1, two FCE banks are used. Both FCE banks are driven by a multi-rate DEM encoder, which ensures that the error arising from FCE mismatches is free of nonlinear distortion. In addition, the multi-rate DEM encoder avoids high power consumption because most of its digital logic is clocked at a rate of f_{in} instead of f_{fast}.[2] Much of the additive error is not oversampled, so instead of relying on the DCO to suppress it, the MNC technique adaptively measures the error and cancels it in real time.

IV. FCE Mismatch Model

FCEs with $\Delta_i > \Delta_{\min}$ are usually built by connecting nominally identical minimum-weight FCEs in parallel. Static mismatches among these FCEs are sources of error, but other non-idealities such as the non-instantaneous frequency transitions of realizable FCEs are also sources of error. Hence, a more comprehensive model than (11) for $f_i(t)$ is

$$f_i(t) = (b_i[m_t] - 1/2)\,\Delta_i + e_i(t), \tag{15}$$

where $e_i(t)$ is error that models both the static mismatch and the non-ideal frequency transitions of the ith FCE. FCEs are designed such that frequency transitions caused by input bit changes settle within a clock period, so $e_i(t)$ only depends on $b_i[m_t - 1]$ and $b_i[m_t]$. This can be modeled as

$$e_i(t) = \begin{cases} e_{11i}, & \text{if } b_i[m_t - 1] = 1,\ b_i[m_t] = 1, \\ e_{01i}(t), & \text{if } b_i[m_t - 1] = 0,\ b_i[m_t] = 1, \\ e_{00i}, & \text{if } b_i[m_t - 1] = 0,\ b_i[m_t] = 0, \\ e_{10i}(t), & \text{if } b_i[m_t - 1] = 1,\ b_i[m_t] = 0, \end{cases} \tag{16}$$

where e_{11i}, $e_{01i}(t)$, e_{00i}, and $e_{10i}(t)$ represent the error over each clock interval corresponding to the four

[2] Although the hardware of the proposed techniques is different from that of the solution in which $d[n_t]$ is oversampled and a DEM encoder clocked at a high rate is used to control the FCEs, a pessimistic power consumption analysis suggests that the proposed techniques are at least five times more power-efficient.

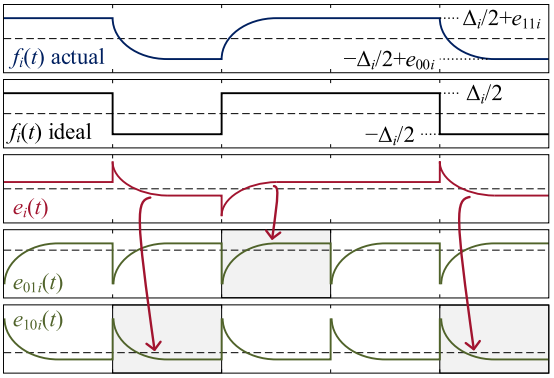

Fig. 2. Example waveforms related to (15) and (16) for an FCE input bit sequence of 1, 0, 1, 1, 0.

different possibilities of the FCE's current and prior input bit values [53].[3]

Fig. 2 shows example waveforms associated with (15) and (16). A consequence of the frequency transitions settling within a clock period is that when an FCE's input bit does not change between clock periods, neither does its contribution to the DCO frequency, so e_{00i} and e_{11i} are constant. In contrast, $e_{01i}(t)$ and $e_{10i}(t)$ are not constant because they represent deviations from the FCE's ideal instantaneous frequency transitions when its input bit changes. As shown in Fig. 2, the shape of each of these frequency transitions depends only on whether the corresponding FCE input changed from 0 to 1 or 1 to 0, and both $e_{01i}(t)$ and $e_{10i}(t)$ are $1/f_{\text{FCE}}$-periodic.

Experimental results suggest, at least for the LC-based DCOs presented in [36] and [39], that the frequency transition introduced by each FCE when its input bit changes from 0 to 1 and that when the input bit changes from 1 to 0 are antisymmetric to a high degree of accuracy, i.e., $e_{11i} - e_{01i}(t) = -[e_{00i} - e_{10i}(t)]$. Therefore, substituting (16) into (15), applying this observation, collecting terms and omitting constant additive terms yields

$$f_i(t) = (b_i[m_t] - 1/2)\,\alpha_i(t)\Delta_i + (b_i[m_t - 1] - 1/2)\,\gamma_i(t), \tag{17}$$

where

$$\alpha_i(t) = 1 + (e_{01i}(t) - e_{00i})/\Delta_i \text{ and } \gamma_i(t) = e_{11i} - e_{01i}(t). \tag{18}$$

Given that $\alpha_i(t)$ and $\gamma_i(t)$ are functions of $e_{01i}(t)$ and $e_{10i}(t)$, which are $1/f_{\text{FCE}}$-periodic, they are also $1/f_{\text{FCE}}$-periodic.

V. Multi-Rate DEM

A. Starting Point: Single-Rate Segmented DEM

Suppose the DCO's input sequence is given by (3), and for now suppose that $\Delta\Sigma$ quantization is not necessary because FCEs with small-enough step sizes are available,

[3]The FCE model given by (15) and (16) is analogous to that of a non-return-to-zero (NRZ) 1-bit DAC. To prevent $e_i(t)$ from depending on $b_i[m_t - 1]$, return-to-zero (RZ) FCEs could be implemented by setting the FCEs to a signal-independent state for a fraction of each clock period, but this is not practical for PLLs because it would periodically slew the DCO frequency and thereby introduce excessive phase noise.

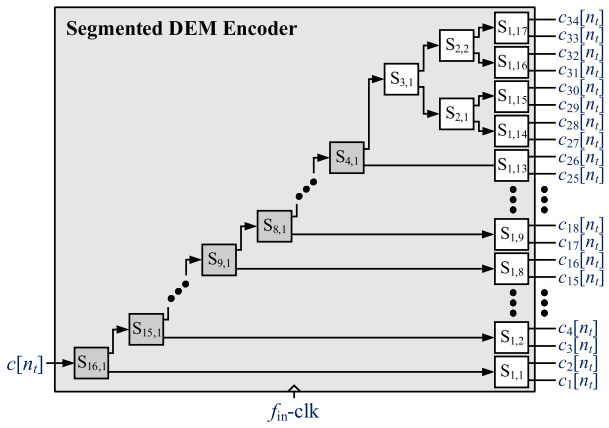

Fig. 3. Segmented DEM encoder example.

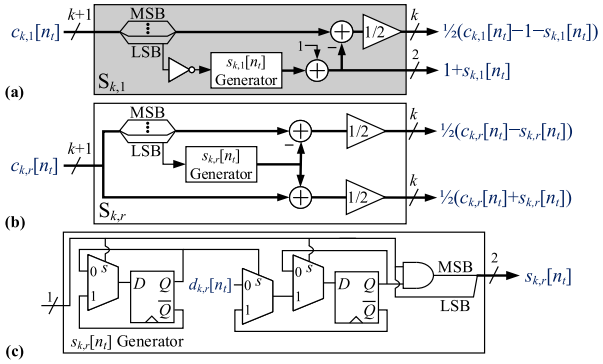

Fig. 4. (a) Segmenting switching block, (b) non-segmenting switching block, and (c) switching sequence generator.

i.e., $\Delta_{\min} = \Delta$. Even in this case, FCE mismatches are a problem because they cause nonlinear distortion. A conventional single-rate segmented DEM encoder can be used to prevent this problem. For example, the mismatch-shaping segmented DEM encoder shown in Fig. 3 can be used with 34 FCEs [54]. The ith FCE has input $b_i[n_t] = c_i[n_t]$ and frequency step size $\Delta_i = K_i\Delta$, where

$$K_{2i-1} = K_{2i} = 2^{i-1} \quad \text{for} \quad i = 1,\ 2,\ \ldots,\ 13 \quad \text{and}$$
$$K_i = 2^{13} \quad \text{for} \quad i = 27,\ 28,\ \ldots,\ 34. \tag{19}$$

The DEM encoder's input sequence, $c[n_t]$, is obtained from the DCO input sequence as

$$c[n_t] = d[n_t]/\Delta + 2^{15} + 2^{13} - 1 \tag{20}$$

for reasons explained in [54].

As shown in Fig. 3, the DEM encoder consists of 33 digital switching blocks (SBs), labeled $S_{k,r}$ for $k = 1, 2, \ldots, 16$, and $r = 1, 2, \ldots, 17$, configured in a tree structure. The 13 shaded SBs are called segmenting SBs, whereas the other 20 SBs are called non-segmenting SBs. The functional details of the SBs are shown in Fig. 4. The top and bottom outputs of each segmenting SB are $\frac{1}{2}(c_{k,1}[n_t] - 1 - s_{k,1}[n_t])$ and $1 + s_{k,1}[n_t]$, respectively, where $c_{k,1}[n_t]$ is the SB input sequence, and $s_{k,1}[n_t]$, called a switching sequence, is 0 when $c_{k,1}[n_t]$ is odd and ± 1 otherwise. Similarly, the top and bottom outputs of each non-segmenting SB are $\frac{1}{2}(c_{k,r}[n_t] - s_{k,r}[n_t])$

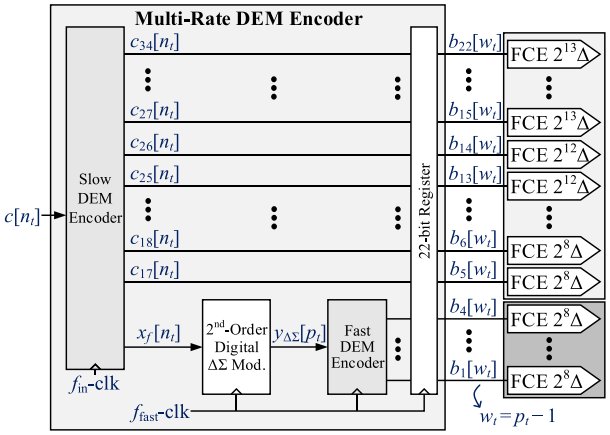

Fig. 5. Multi-rate DEM encoder example.

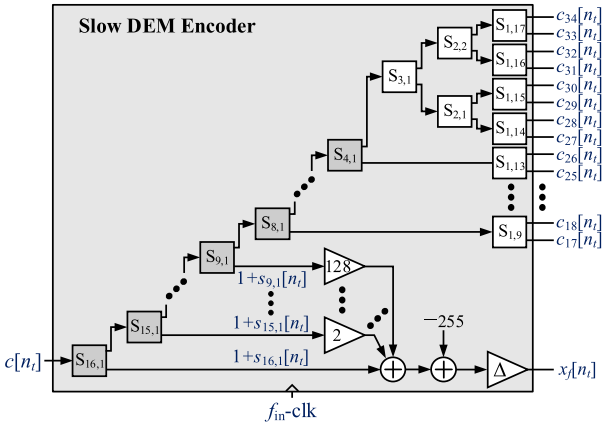

Fig. 6. Slow DEM encoder example.

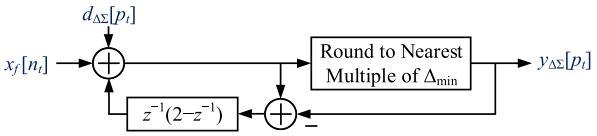

Fig. 7. Details of the second-order digital ΔΣ modulator.

and ½($c_{k,r}[n_t] + s_{k,r}[n_t]$), respectively, where $c_{k,r}[n_t]$ is the SB input sequence and $s_{k,r}[n_t]$ is 0 when $c_{k,r}[n_t]$ is even and ±1 otherwise.

Regardless of the SB type, each switching sequence is zero-mean and has a first-order highpass-shaped power spectral density (PSD) that peaks at $f_{\text{in}}/2$. It is generated in two's complement format by the logic shown in Fig. 4(c), wherein $d_{k,r}[n_t]$ is generated within each SB and is well-modeled as a two-level white random sequence that takes on values of 0 and 1 with equal probability and is independent of the $d_{k,r}[n_t]$ sequences in the other SBs.

B. Extension to Multi-Rate Segmented DEM

Now suppose that the smallest practical FCE frequency step size is $\Delta_{\min} = 2^8\Delta$. As the lower 16 FCEs in the example above all have frequency step sizes smaller than $\Delta_{\min}$, the bottom 16 outputs of the DEM encoder can no longer drive FCEs directly. The multi-rate DEM architecture shown in Fig. 5 addresses this situation, where the bottom 4 FCEs make up the fractional FCE bank, the top 18 FCEs make up the integer FCE bank, and $w_t = p_t - 1$ is a T_{fast}-delayed version of p_t, where $T_{\text{fast}} = 1/f_{\text{fast}}$. As in Fig. 1, $n_t = g(p_t)$ changes synchronously with p_t.

The block labeled slow DEM encoder in Fig. 5 is a modified version of the DEM encoder in Fig. 3. Its outputs $c_{17}[n_t]$, $c_{18}[n_t]$, …, $c_{34}[n_t]$ are identical to those in Fig. 3, and instead of outputs $c_1[n_t]$, $c_2[n_t]$, …, $c_{16}[n_t]$ it has an output, $x_f[n_t]$, given by

$$x_f[n_t] = \Delta \sum_{i=1}^{16} K_i \, (c_i[n_t] - 1/2). \tag{21}$$

Each $c_i[n_t]$ takes on values of 0 and 1, so (19) and (21) imply that $|x_f[n_t]| \le 255\Delta$ and $x_f[n_t]$ is restricted to multiples of Δ.

The slow DEM encoder could be implemented from the DEM encoder of Fig. 3 directly by combining $c_1[n_t]$, $c_2[n_t]$, …, $c_{16}[n_t]$ as in (21), but the structure of Fig. 6 is used instead because is simpler. As implied by Fig. 4(b), the sum of the outputs of each non-segmenting SB is equal to the SB's input, so it follows from (21), Fig. 3 and Fig. 4(a) that $x_f[n_t]$ can be computed directly from the bottom outputs of $S_{16,1}$, $S_{15,1}$, …, $S_{9,1}$ as

$$x_f[n_t] = \Delta \sum_{k=9}^{16} 2^{16-k} s_{k,1}[n_t]. \tag{22}$$

Hence, as shown in Fig. 6, $S_{1,1}$, $S_{1,2}$, …, $S_{1,8}$ are not necessary in the slow DEM encoder.

The Δ scale factor shown in Fig. 6 is not an actual multiplier; it just denotes that the subsequent digital logic should interpret the LSB of $x_f[n_t]$ to represent a DCO frequency step size of Δ.

As shown in Fig. 5, $x_f[n_t]$ is sampled at a rate of f_{fast} by a second-order digital ΔΣ modulator whose functional diagram is shown in Fig. 7. The dither sequence, $d_{\Delta\Sigma}[p_t]$, is generated such that it can be well-modeled as a two-level white random sequence that is independent of $d[n_t]$ and $x_f[n_t]$ and takes on values of 0 and Δ with equal probability. It ensures that the ΔΣ modulator's quantization noise is asymptotically independent of $x_f[n_t]$ and $d_{\Delta\Sigma}[p_t]$, and has a PSD equal to that of the output of a filter with transfer function $(1 - z^{-1})^2$ driven by white noise with a variance of $\Delta_{\min}^2/12$ [55]. The ΔΣ modulator output is quantized to values in the set $\{-2\Delta_{\min}, -\Delta_{\min}, 0, \Delta_{\min}, 2\Delta_{\min}\}$ and is given by

$$y_{\Delta\Sigma}[p_t] = x_f[n_t] + e_{\Delta\Sigma}[p_t], \tag{23}$$

where $e_{\Delta\Sigma}[p_t]$ is second-order highpass-shaped quantization noise plus $d_{\Delta\Sigma}[p_t]$.

The block in Fig. 5 labeled fast DEM encoder is a conventional mismatch-shaping non-segmented DEM encoder with a clock rate of f_{fast}. It is implemented as a tree of non-segmenting SBs, and it maps $y_{\Delta\Sigma}[p_t]$ to four 1-bit sequences, each of which drives an FCE with a frequency step size of $\Delta_{\min}$ [56], [57].

Each $b_i[w_t]$ in Fig. 5, for $i = 1, 2, 3, 4$, is clocked at a rate of f_{fast} and toggles rapidly enough such that the FCE frequency transitions from the fractional FCE bank introduce high-frequency error components to the DCO's phase error. Such components are lowpass filtered by the DCO, so they are not a problem in practice provided f_{fast} is large enough. Consequently, the frequency transitions of the FCEs from the fractional FCE bank are modeled as ideal, so that $f_i(t)$ is given by (11) for $i = 1, 2, 3, 4$.

It follows from the results presented in [53] and (11) that

$$f_F(t) = \alpha_F y_{\Delta\Sigma}[w_t] + e_F(t), \tag{24}$$

where α_F is the average of α_i for $i = 1, 2, 3, 4$ and $e_F(t)$ is a function of the errors introduced by the fractional FCE bank and the switching sequences from the fast DEM encoder. The fast DEM encoder ensures that $e_F(t)$ is free of nonlinear distortion, uncorrelated with $y_{\Delta\Sigma}[w_t]$, and has a first-order highpass-shaped PSD that peaks at $f_{\text{fast}}/2$, so this term is not a problem in practice provided f_{fast} is large enough. Thus, substituting (23) into (24) and neglecting $e_F(t)$ gives

$$f_F(t) = \alpha_F x_f[g(w_t)] + \alpha_F e_{\Delta\Sigma}[w_t]. \tag{25}$$

As shown in Fig. 5, the $c_{17}[n_t]$, $c_{18}[n_t]$, …, $c_{34}[n_t]$ outputs of the slow DEM encoder drive the same FCEs as those of the DEM encoder of Fig. 3. As shown in Appendix A, this implies that $f_I(t)$ is given by

$$f_I(t) = \alpha_I(t) d[g(w_t)] + \gamma_I(t) d[g(w_t - 1)] + e_I(t), \tag{26}$$

where

$$e_I(t) = \Delta \sum_{k,r} \left\{ \alpha_{k,r}(t) s_{k,r}[g(w_t)] + \gamma_{k,r}(t) s_{k,r}[g(w_t - 1)] \right\}, \tag{27}$$

$\alpha_I(t)$, $\gamma_I(t)$, $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ are T_{fast}-periodic waveforms that depend on the errors introduced by the integer FCE bank, and the summation indices indicate the summation over all k and r values corresponding to the SBs within the slow DEM encoder.

The contribution to the DCO frequency from both FCE banks is $f_{\text{tune}}(t) = f_I(t) + f_F(t)$, so (25) and (26) imply that

$$f_{\text{tune}}(t) = \alpha_I(t) d[g(w_t)] + \gamma_I(t) d[g(w_t - 1)] + \alpha_F e_{\Delta\Sigma}[w_t] + e_M(t), \tag{28}$$

where

$$e_M(t) = e_I(t) + \alpha_F x_f[g(w_t)] \tag{29}$$

is called *FCE mismatch error*. As shown below, $e_M(t)$ is a linear combination of the switching sequences from the slow DEM encoder whose coefficients depend on the errors introduced by both FCE banks.

The $\gamma_I(t) d[g(w_t - 1)]$ term in (28) is proportional to a T_{fast}-delayed version of $d[g(w_t)]$, so it represents a linear filtering operation. It follows from the expressions for $\alpha_I(t)$ and $\gamma_I(t)$ in Appendix A that this term tends to be much smaller than the desired signal component, $\alpha_I(t) d[g(w_t)]$, so it is not a problem in practice. The $\alpha_F e_{\Delta\Sigma}[w_t]$ term is proportional to $\Delta\Sigma$ quantization noise plus dither so it is free of nonlinear distortion, is uncorrelated with the other terms in (28), and has a highpass-shaped PSD. The $e_M(t)$ term also has these properties because it is a linear combination of the switching sequences from the slow DEM encoder. The PSD of $\alpha_F e_{\Delta\Sigma}[w_t]$ peaks at $f_{\text{fast}}/2$, whereas the PSD of $e_M(t)$ peaks at $f_{\text{in}}/2$. Hence, f_{fast} can be increased to make the DCO phase error introduced by $\alpha_F e_{\Delta\Sigma}[w_t]$ negligible, but this would not reduce the DCO phase error contribution from $e_M(t)$. Therefore, $e_M(t)$ is the only problematic term in (28).

Substituting (22) and (27) into (29) yields

$$e_M(t) = \Delta \sum_{k,r} \left\{ \delta_{k,r} s_{k,r}[g(w_t)] + \gamma_{k,r}(t) \left(s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)] \right) \right\}, \tag{30}$$

where

$$\delta_{k,r} = \begin{cases} \alpha_{k,r}(t) + \gamma_{k,r}(t) + \alpha_F 2^{16-k}, & \text{if } k \geq 9,\ r = 1, \\ \alpha_{k,r}(t) + \gamma_{k,r}(t), & \text{otherwise,} \end{cases} \tag{31}$$

is constant for each k and r, even though neither $\alpha_{k,r}(t)$ nor $\gamma_{k,r}(t)$ are constant. As can be verified by substituting (18) into the expressions for $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ in Appendix A, the non-constant terms in each $\alpha_{k,r}(t)$ are equal in magnitude but opposite in sign to the corresponding terms in $\gamma_{k,r}(t)$, so $\alpha_{k,r}(t) + \gamma_{k,r}(t)$, and hence $\delta_{k,r}$, are constant. Therefore, the terms proportional to $\delta_{k,r}$ in (30) represent the DCO frequency error contribution from FCE static gain errors, whereas the terms proportional to $\gamma_{k,r}(t)$ in (30) represent the DCO frequency error contribution from non-ideal FCE frequency transitions.

VI. Adaptive FCE Mismatch Noise Cancellation

The purpose of the MNC technique is to cancel most of the DCO phase error that would otherwise be caused by $e_M(t)$. To do this, the sequence

$$e_{\text{MNC}}[p_t] = \Delta \sum_{k,r} \left\{ a_{k,r} s_{k,r}[n_t] + b_{k,r} \left(s_{k,r}[g(w_t)] - s_{k,r}[n_t] \right) \right\}, \tag{32}$$

where $a_{k,r}$ and $b_{k,r}$ are called the MNC coefficients, is injected into the fractional path of the multi-rate DEM encoder. The ideal MNC coefficient values, i.e., the values of $a_{k,r}$ and $b_{k,r}$ for which the DCO phase error contribution of $e_M(t)$ is minimized, are estimated with a least-mean-square (LMS)-like algorithm.

In the following, it is explained how $e_{\text{MNC}}[p_t]$ affects the DCO's phase error, how the FCE mismatch error is measured, and how the MNC coefficients are adaptively computed from the FCE mismatch error measurement.

A. MNC Sequence Application

Fig. 8 shows the fractional path of the multi-rate DEM encoder shown in Fig. 5 modified to accommodate MNC. The $e_{\text{MNC}}[p_t]$ sequence is subtracted from $x_f[n_t]$ prior to the $\Delta\Sigma$ modulator, and the output range of the $\Delta\Sigma$ modulator, the range of the fast DEM encoder, and the number of FCEs driven by the fast DEM encoder are all four times those of the original system to accommodate the resulting dynamic range

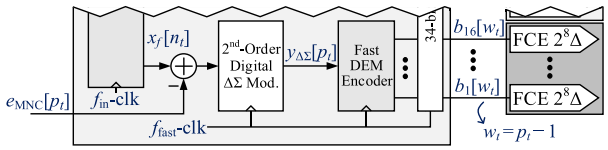

Fig. 8. Fractional path of the example multi-rate DEM encoder shown in Fig. 5 modified to accommodate $e_{\mathrm{MNC}}[p_t]$.

increase. Thus, $f_F(t)$ is still given by (24), but now $y_{\Delta\Sigma}[p_t]$ is given by the right side of (23) minus $e_{\mathrm{MNC}}[p_t]$. Despite having the same qualitative properties as before, α_F and $e_F(t)$ in (24) are slightly different in the modified system because of the additional FCEs.

An analysis almost identical to that presented in Section V shows that $f_{\mathrm{tune}}(t)$ is now given by

$$f_{\mathrm{tune}}(t) = \alpha_I(t)d[g(w_t)] + \gamma_I(t)d[g(w_t-1)] + \alpha_F e_{\Delta\Sigma}[w_t] + e_R(t), \quad (33)$$

where

$$e_R(t) = e_M(t) - \alpha_F e_{\mathrm{MNC}}[w_t] \quad (34)$$

is the *residual* FCE mismatch error, i.e., what is left of $e_M(t)$ when $e_{\mathrm{MNC}}[p_t]$ is applied. It follows from (30), (32) and (34) that

$$e_R(t) = \Delta \sum_{k,r} \left\{ \delta_{k,r\text{-res}} s_{k,r}[g(w_t)] + \gamma_{k,r\text{-res}}(t) \left(s_{k,r}[g(w_t-1)] - s_{k,r}[g(w_t)] \right) \right\}, \quad (35)$$

where $\delta_{k,r\text{-res}}$ and $\gamma_{k,r\text{-res}}(t)$ are defined as

$$\delta_{k,r\text{-res}} = \delta_{k,r} - \alpha_F a_{k,r} \quad \text{and} \quad \gamma_{k,r\text{-res}}(t) = \gamma_{k,r}(t) - \alpha_F b_{k,r}, \quad (36)$$

respectively.

Given that $\delta_{k,r}$ is constant, there exists an $a_{k,r}$ that causes $\delta_{k,r\text{-res}} = 0$. In contrast, there is no $b_{k,r}$ that causes $\gamma_{k,r\text{-res}}(t)$ to vanish completely, because $\gamma_{k,r}(t)$ is not constant. However, $\gamma_{k,r}(t)$ is T_{fast}-periodic so there exists a $b_{k,r}$ that makes the DC component of $\gamma_{k,r\text{-res}}(t)$ zero, such that $\gamma_{k,r\text{-res}}(t)$ is a linear combination of sinusoids with frequencies that are non-zero multiples of f_{fast} [58]. Therefore, it follows from (36) that if

$$a_{k,r} = \frac{\delta_{k,r}}{\alpha_F} \quad \text{and} \quad b_{k,r} = \frac{1}{\alpha_F T_{\mathrm{fast}}} \int_0^{T_{\mathrm{fast}}} \gamma_{k,r}(\tau)d\tau, \quad (37)$$

for each k and r, then

$$\delta_{k,r\text{-res}} = 0 \text{ and } \int_0^{T_{\mathrm{fast}}} \gamma_{k,r\text{-res}}(\tau)d\tau = 0. \quad (38)$$

In the absence of FCE static mismatches, $a_{k,r} = 0$, and if the FCE frequency transitions are ideal, $b_{k,r} = 0$.

Phase error is the integral of frequency error, so the DCO phase error introduced by $e_R(t)$ is given by

$$\theta_R(t) = \int_0^t e_R(\tau)d\tau. \quad (39)$$

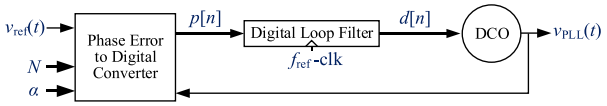

Fig. 9. General form of a digital fractional-N PLL.

If (38) is satisfied, then (35) and (39) imply that

$$\theta_R(t) = \Delta \sum_{k,r} \left(s_{k,r}[g(w_t-1)] - s_{k,r}[g(w_t)] \right) \times \int_0^{t-p_t T_{\mathrm{fast}}} \gamma_{k,r\text{-res}}(u)du, \quad (40)$$

where $t - p_t T_{\mathrm{fast}} = t - \lfloor f_{\mathrm{fast}} t \rfloor T_{\mathrm{fast}} < T_{\mathrm{fast}}$. The term within the parenthesis in (40) equals zero when $g(w_t) - g(w_t - 1) = 0$ and $s_{k,r}[g(w_t)-1] - s_{k,r}[g(w_t)]$ otherwise. Given that $g(w_t) - g(w_t - 1)$ can only take on values from the set {0,1}, then

$$s_{k,r}[g(w_t-1)] - s_{k,r}[g(w_t)] = (g(w_t) - g(w_t-1)) \left(s_{k,r}[g(w_t)-1] - s_{k,r}[g(w_t)] \right). \quad (41)$$

Furthermore, $g(w_t)$ is a T_{fast}-delayed version of n_t, which increases by one unit every $T_{\mathrm{in}} = 1/f_{\mathrm{in}}$, so $g(w_t) - g(w_t - 1)$ is T_{in}-periodic and is given by

$$g(w_t) - g(w_t-1) = \sum_{k=-\infty}^{\infty} r\,(t - kT_{\mathrm{in}}), \quad (42)$$

where $r(t) = 1$ for $t \in [T_{\mathrm{fast}}, 2T_{\mathrm{fast}})$ and 0 otherwise. It follows from (42) that the Fourier expansion of $g(w_t) - g(w_t - 1)$ is

$$\frac{f_{\mathrm{in}}}{f_{\mathrm{fast}}} + \sum_{m=1}^{\infty} \frac{2}{m\pi} \sin\left(m\pi \frac{f_{\mathrm{in}}}{f_{\mathrm{fast}}}\right) \cos\left(2\pi m f_{\mathrm{in}} \left[t - \frac{3}{2}T_{\mathrm{fast}}\right]\right). \quad (43)$$

Thus, if the conditions shown in (38) are satisfied, (40), (41) and (43) imply that $\theta_R(t)$ would be given by second-order shaped noise multiplied by a T_{in}-periodic waveform and a DC-free T_{fast}-periodic waveform. Consequently, $e_R(t)$ would introduce components with frequencies around $f_{n,m} = nf_{\mathrm{fast}} \pm mf_{\mathrm{in}}$ to the DCO's phase error, where $n = 1, 2, 3, \ldots$ and $m = 0, 1, 2, \ldots$. It follows from (43) that the power of the components around frequencies $f_{n,m}$ with m near multiples of $f_{\mathrm{fast}}/f_{\mathrm{in}}$ is very low. Therefore, $\theta_R(t)$ would not be a problem if f_{fast} is large enough because $e_R(t)$ would only introduce high-frequency components to the DCO's phase error that would be lowpass filtered by the DCO. Simulation results also suggest that $\theta_R(t)$ is not a problem provided the conditions shown in (38) are satisfied and f_{fast} is large enough.

B. FCE Mismatch Error Measurement

The ideal MNC coefficient values are estimated as part of the feedback loop in a digital fractional-N PLL that incorporates the DCO. This is done during the PLL's normal operation by adaptively adjusting $a_{k,r}$ and $b_{k,r}$ such that the conditions shown in (38) are satisfied for each k and r, thereby minimizing $e_R(t)$.

The purpose of a fractional-N PLL is to generate a periodic output signal, $v_{\mathrm{PLL}}(t)$, with frequency $f_{\mathrm{PLL}} = (N + \alpha) f_{\mathrm{ref}}$,

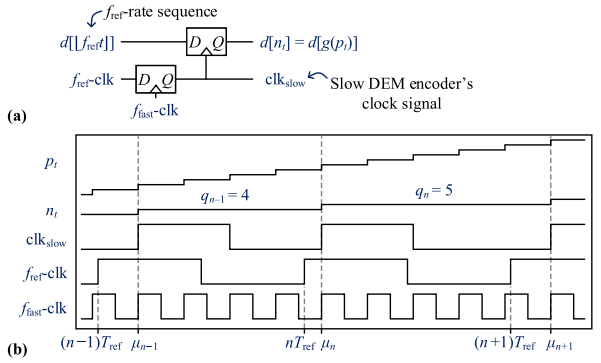

Fig. 10. (a) Synchronization circuit used at DCO input, and (b) illustration of the clock signals within the DCO, p_t, and $n_t = g(p_t)$ for $f_{\text{fast}} = 4.5 f_{\text{ref}}$.

where N is a positive integer, α is a fractional value and f_{ref} is the frequency of a reference oscillator waveform, $v_{\text{ref}}(t)$. The general form of a digital fractional-N PLL without MNC is shown in Fig. 9. It consists of a phase-error-to-digital converter (PEDC), a lowpass digital loop filter (DLF), and a DCO. The PEDC's output is an f_{ref}-rate digital sequence of the form

$$p[n] = -\theta_{\text{PLL}}[n] + e_p[n], \tag{44}$$

where $\theta_{\text{PLL}}[n]$ is an estimate of the PLL's phase error and $e_p[n]$ is additive error that includes quantization error from the PEDC's digitization process as well as error from circuit noise and other non-ideal circuit behavior in both the PEDC and reference oscillator.

Suppose the DCO contains the multi-rate DEM structure shown in Fig. 5 modified as shown in Fig. 8 with $f_{\text{in}} = f_{\text{ref}}$. Typically, f_{fast}-clk is a divided-down version of $v_{\text{PLL}}(t)$. Given that $f_{\text{PLL}} = (N + \alpha) f_{\text{ref}}$, f_{ref} and f_{fast} are incommensurate frequencies when $\alpha \neq 0$, so it is not possible for n_t to change synchronously with $p_t = \lfloor f_{\text{fast}} t \rfloor$ if $n_t = \lfloor f_{\text{ref}} t \rfloor$. Therefore, as shown in Fig. 10, in practice the DCO input is synchronized to f_{fast}-clk so (4) is satisfied, i.e., so n_t only changes at times μ_n, which are multiples of T_{fast}, instead of times nT_{ref}, where $T_{\text{ref}} = 1/f_{\text{ref}}$ is the reference period. It is common practice in digital PLLs to synchronize the DLF output to the clock signal of the fractional path, so this is not a special requirement of the proposed system. A circuit to avoid metastability issues is also needed as part of the synchronization circuit shown in Fig. 10(a), but it has been omitted for simplicity [59].

A key requirement of a PLL is to suppress low-frequency DCO error, which is achieved by subjecting additive frequency error introduced by the DCO to a highpass filter that has at least one zero at DC. In the following, the impulse response of this filter is denoted as $h[n]$, and its running sum, i.e., $h[0] + h[1] + \ldots + h[n]$, is denoted as $l[n]$.

As shown in Appendix B, $p[n]$ can be written as

$$p[n] = p_{\text{ideal}}[n] + p_R[n], \tag{45}$$

where $p_{\text{ideal}}[n]$ represents the contribution to $p[n]$ of all noise sources except FCE mismatches and $p_R[n]$ is the contribution to $p[n]$ from $e_R(t)$. Specifically, $p_R[n]$ is given by

$$p_R[n] = \Delta\alpha_F T_{\text{fast}} \sum_{i=0}^{n-1} \sum_{k,r} \left\{ y_{k,r\text{-}a}[i] + y_{k,r\text{-}b}[i] \right\} l[n-1-i], \tag{46}$$

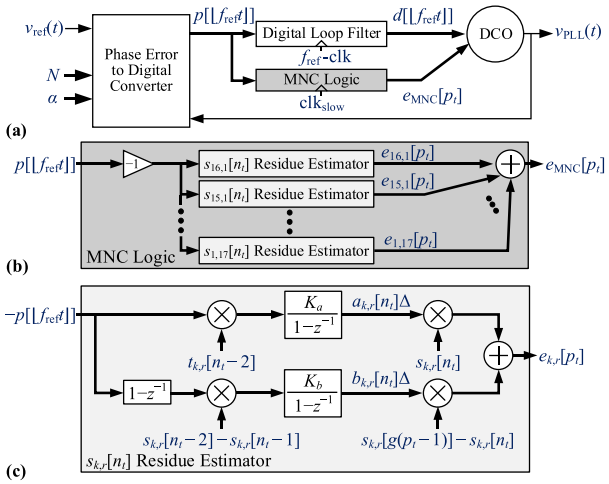

Fig. 11. (a) Digital fractional-N PLL with multi-rate DEM and MNC, (b) details of the MNC logic, and (c) details of each switching sequence residue estimator.

where $y_{k,r\text{-}a}[i] + y_{k,r\text{-}b}[i]$ is proportional to the PLL's frequency error introduced by the $s_{k,r}[n]$ sequences. As explained in Appendix B, if $a_{k,r}$ and $b_{k,r}$ in (32) are replaced by $a_{k,r}[n_t]$ and $b_{k,r}[n_t]$, respectively, then

$$y_{k,r\text{-}a}[i] = (q_{i-1} - 3)\, s_{k,r}[i-1] a_{k,r\text{-error}}[i-1] + 3 s_{k,r}[i] a_{k,r\text{-error}}[i] \tag{47}$$

and

$$y_{k,r\text{-}b}[i] = \left(s_{k,r}[i-1] - s_{k,r}[i] \right) b_{k,r\text{-error}}[i], \tag{48}$$

where q_{i-1} is the number of T_{fast} periods between times μ_{i-1} and μ_i, and

$$\begin{aligned} a_{k,r\text{-error}}[n] &= a_{k,r}[n] - a_{k,r} \quad \text{and} \\ b_{k,r\text{-error}}[n] &= b_{k,r}[n] - b_{k,r} \end{aligned} \tag{49}$$

are the MNC coefficient errors at sample time n.

The term proportional to $s_{k,r}[i]$ in (47) arises because the time at which the PEDC samples the PLL's phase error, which is given by $\mu_n + 4T_{\text{fast}}$ in the design example, is not equal to the time at which the integer FCE bank's inputs are updated, i.e., $\mu_n + T_{\text{fast}}$. Accordingly, the integer FCE bank's inputs are updated three T_{fast} before the PLL's phase error is sampled, which causes $y_{k,r\text{-}a}[i]$ to depend on $s_{k,r}[i-1]$ and also on $s_{k,r}[i]$.

As implied by (45)-(48), the PEDC's output has information regarding the MNC coefficient errors. The MNC coefficient estimation process described next is based on this result and on the properties of the switching sequences.

C. MNC Coefficients Estimation

A digital fractional-N PLL with the multi-rate DEM encoder and MNC technique is shown in Fig. 11(a). The details of the MNC logic are shown in Fig. 11(b) and Fig. 11(c), wherein

$$t_{k,r}[n] = \sum_{i=0}^{n} s_{k,r}[i] \tag{50}$$

is the running sum of $s_{k,r}[n]$, and K_a and K_b are called the MNC gains. The MNC logic block consists of an adder and 25 $s_{k,r}[n_t]$ residue estimators.

It follows from Fig. 4 that each $s_{k,r}[n]$ sequence is a concatenation of sequences of the form 1, 0, …, 0, –1, 0, …, 0 or –1, 0, …, 0, 1, 0, …, 0, where each 0 is present only when the input of the $s_{k,r}[n]$ generator is zero [52]. Thus, $|s_{k,r}[n]| \leq 1, |t_{k,r}[n]| \leq 1$ and $|s_{k,r}[n] - s_{k,r}[n-1]| \leq 2$ for all n, so the multipliers in Fig. 11(c) are simple in terms of hardware.

The $s_{k,r}[n_t]$ residue estimators are responsible for the computation of the MNC coefficients. At each sample time, the MNC coefficient errors are measured and $a_{k,r}[n_t]$ and $b_{k,r}[n_t]$ are updated such that they approach the values shown in (37). The measurement of the MNC coefficient errors is based on the statistical properties of the switching sequences [60].

As explained in [57] and can be verified from Fig. 4, although each $s_{k,r}[n]$ sequence depends on the input of its corresponding SB, when it is non-zero, its sign depends on $d_{k,r}[n]$. Given that the $d_{k,r}[n]$ sequences are independent of the $d_{k,r}[n]$ sequences in the other SBs, this provides enough randomization for the $s_{k,r}[n]$ sequences to be uncorrelated with each other. Furthermore, as the $d_{k,r}[n]$ sequences are also independent of all electronic device noise sources in the PLL, each $s_{k,r}[n]$ sequence is uncorrelated with all such sources as well, and it is also uncorrelated with the PEDC's quantization noise in PLLs where such noise source is uncorrelated with the PLL's phase error [29], [39]. Hence, in such cases, the $s_{k,r}[n]$ sequences are uncorrelated with all PLL noise except the terms in $p[n]$ arising from $e_R(t)$, i.e., $p_R[n]$.

As explained above, the $y_{k,r\text{-}a}[i]$ and $y_{k,r\text{-}b}[i]$ terms in $p[n]$ depend on the MNC coefficient errors, and such terms are proportional to functions of the $s_{k,r}[n]$ sequences. Specifically, it can be seen from (45)-(48) that $p[n]$ has information about an accumulated version of

$$(q_{n-2} - 3)\, s_{k,r}[n-2] a_{k,r\text{-error}}[n-2], \tag{51}$$

and that $p[n] - p[n-1]$ has information about

$$\big(s_{k,r}[n-2] - s_{k,r}[n-1]\big)\, b_{k,r\text{-error}}[n-1]. \tag{52}$$

Therefore, it follows that the accumulator inputs in Fig. 11(c), i.e., $-p[n]t_{k,r}[n-2]$ and $(p[n-1]-p[n])(s_{k,r}[n-2]-s_{k,r}[n-1])$, when non-zero, are noisy estimates of $a_{k,r\text{-error}}[n]$ and $b_{k,r\text{-error}}[n]$, respectively, so they can be used to adaptively compute the ideal MNC coefficients. In practice, the top and bottom branches within each $s_{k,r}[n_t]$ residue estimator interfere with each other in a way that makes the accumulator inputs have information about both MNC coefficient errors. However, extensive simulations run by the authors suggest that the MNC coefficient values converge to their ideal values regardless of such interferences provided the MNC gains are set properly.

It would also be possible to correlate $p[n-1] - p[n]$ by $s_{k,r}[n-2]$ to get an estimate of $a_{k,r\text{-error}}[n]$. However, as $a_{k,r}[n]$ is only updated when the accumulator input is non-zero, correlating $p[n-1] - p[n]$ against $s_{k,r}[n-2]$ instead of $-p[n]$ against $t_{k,r}[n-2]$ would significantly decrease the convergence speed of $a_{k,r}[n]$ because normally $s_{k,r}[n-2]$ is zero more often than $t_{k,r}[n-2]$. Although correlating $-p[n]$ against $t_{k,r}[n-2]$ effectively increases the error variance of $a_{k,r}[n]$, as explained next, this problem can be mitigated by reducing K_a.

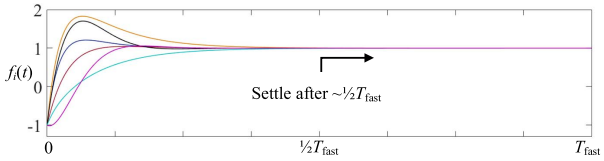

Fig. 12. Example frequency transitions normalized to $\Delta_i/2$ versus time over $T_{\text{fast}} = 8T_{\text{PLL}}$ for six different FCEs.

As is common in most LMS-like algorithms, the choice of K_a and K_b represents a tradeoff. The larger the MNC gains, the faster the convergence, but the larger the error variance of $a_{k,r}[n]$ and $b_{k,r}[n]$. Also, as the $s_{k,r}[n_t]$ residue estimators comprise two LMS-like loops in parallel that interfere with each other, K_a and K_b each affect the convergence time and error variance of both $a_{k,r}[n]$ and $b_{k,r}[n]$. Although it might be possible to develop closed-form expressions that quantify these tradeoffs, the authors currently use simulations to assist the design process and to choose the values of K_a and K_b.

VII. Simulation Results

The multi-rate DEM and the MNC techniques were tested in an event-driven behavioral simulation of a modified version of the $\Delta\Sigma$ frequency-to-digital converter based fractional-N PLL presented in [39] and [40]. As explained in [38], $p[n]$ is given by (44) where $e_p[n]$ is first-order shaped quantization noise that is uncorrelated with the PLL's phase error plus error from both the PEDC and reference oscillator.

The DLF consists of two single-pole IIR stages and a proportional-integral stage. Its transfer function is

$$L(z) = K_M \left(K_P + \frac{K_I}{1-z^{-1}}\right) \prod_{i=0}^{1} \frac{\lambda_i}{1-(1-\lambda_i)\,z^{-1}}, \tag{53}$$

where K_M, K_P, K_I, λ_0 and λ_1 are constant loop filter parameters. The DCO consists of an LC oscillator core with a power-of-two-weighted coarse capacitor bank, an integer FCE bank and a fractional FCE bank. The latter two are driven by the multi-rate DEM encoder shown in Fig. 5 and modified as shown in Fig. 8 with $f_{\text{fast}} = f_{\text{PLL}}/8$ and $\Delta_{\min} = 40$ kHz (i.e., $\Delta = 156.25$ Hz).

The static gain error of the ith FCE was modeled as an additive zero-mean Gaussian random variable with a standard deviation of 5% of Δ_i divided by the square root of $\Delta_i/\Delta_{\min}$, which is consistent with measurement results obtained by the authors from the PLL IC presented in [36]. The FCE frequency transitions were modeled as second-order transients that settle within one T_{fast} period. The parameters of these transients, such as the damping factor and the natural frequency, are modelled as random variables with means and standard deviations determined from transistor-level simulation results. Fig. 12 shows example frequency transients used in the simulation.

The simulated noise parameters of the DCO and the reference oscillator, as well as the PEDC internal parameters, are the same as those used in [38]. Specifically, $f_{\text{ref}} = 26$ MHz,

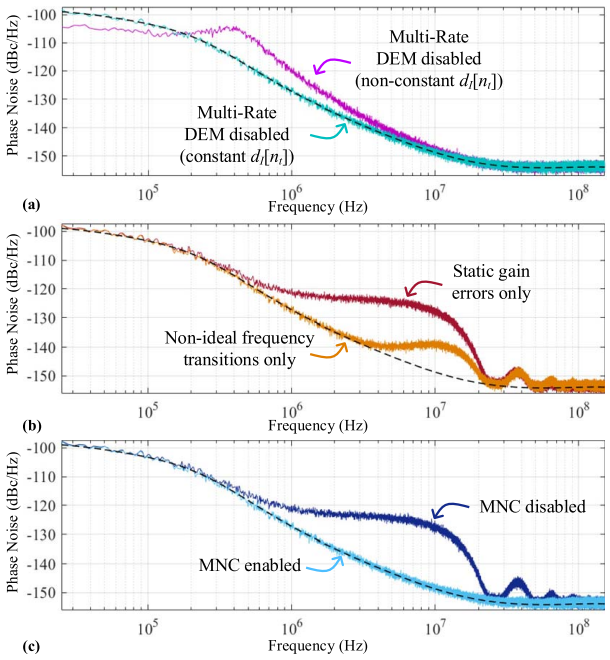

Fig. 13. Simulated PLL phase noise PSD versus frequency with (a) static gain errors and non-ideal frequency transitions enabled and the multi-rate DEM technique disabled, (b) static gain errors and non-ideal frequency transitions enabled separately and the multi-rate DEM technique enabled, and (c) both sources of error enabled, the multi-rate DEM technique enabled and the MNC technique disabled and enabled.

$N = 134$ and $\alpha = 0.0003846153$, so that $f_{\text{PLL}} = 3.484$ GHz and $f_{\text{fast}} = 435.5$ MHz. The DLF parameters used were $K_M = 1.25$, $K_P = 2^4$, $K_I = 2^{-4}$, $\lambda_0 = 2^{-3}$ and $\lambda_1 = 2^{-2}$, and the MNC gains were set to $K_a = 2^{-3}$ and $K_b = 2^{-5}$. The simulated PLL has a bandwidth of 206 kHz and a phase margin of 63 degrees.

Fig. 13(a) shows the simulated PLL phase noise PSD with the multi-rate DEM technique disabled, i.e., with the flip-flops in both the slow and fast DEM encoders frozen. The two curves in Fig. 13(a) were obtained from two different simulations: one in which $d_I[n_t]$ is constant and another one in which $d_I[n_t]$ changes frequently. As mentioned in Section III, although the DCO input sequence does not vary significantly in the short term once the PLL is locked, its moving average drifts over time such that $d_I[n_t]$ eventually begins to change frequently, at which point it degrades the PLL's phase noise as shown in Fig. 13(a). Once the multi-rate DEM technique is enabled, whether or not $d_I[n_t]$ changes has no significant effect on the DCO's frequency, so spectral breathing no longer occurs.

Fig. 13(b) shows the simulated PLL phase noise PSD with the multi-rate DEM technique enabled for two cases: one case with just static gain errors, and the other case with just non-ideal frequency transitions. Fig. 13(c) shows the simulated PLL phase noise PSD considering both sources of error with the multi-rate DEM technique enabled and with the MNC technique disabled and enabled. The theoretical PLL phase noise PSD for ideal FCEs, which was computed using the linearized model presented in [38], is also plotted as the dashed curves in Fig. 13 to provide a comparison baseline.

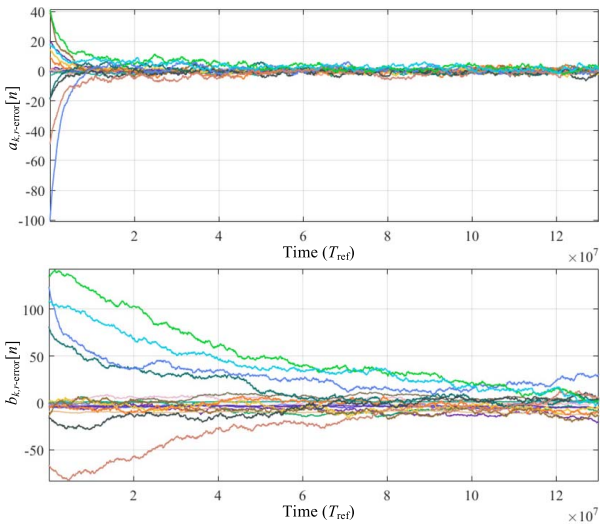

Fig. 14. MNC coefficient error evolution over time for $K_a = 2^{-3}$ and $K_b = 2^{-5}$.

As shown in Fig. 13(c), when the MNC technique is enabled the resulting phase noise PSD matches the theoretically-predicted phase noise PSD for ideal FCEs after $13 \cdot 10^7$ reference periods (5 seconds) from a cold start. This implies a phase noise improvement of more than 20 dB at an offset frequency around 10 MHz. As the FCE mismatches are mostly determined by circuit component mismatches, they are not expected to change significantly over time. Hence, once obtained, the MNC coefficients can be stored in memory and used subsequently by the PLL, thereby avoiding future convergence time delays.

Fig. 14 shows the evolution of the MNC coefficient errors over time from the simulation used to generate the curves in Fig. 13(c). As shown in Fig. 14, some $b_{k,r}[n]$ coefficients initially move away from their ideal values. As explained above, this happens because the top and bottom branches of each $s_{k,r}[n_t]$ residue estimator interfere with each other so that the error estimate at the input of each accumulator is biased by the MNC coefficient error of the opposite branch. As suggested by Fig. 14, if the MNC gains are set properly, this is not a problem in practice because this effect becomes less significant as either one or both MNC coefficients approach their ideal values.[4]

It follows from (47) and (48) that the terms proportional to $a_{k,r\text{-error}}[n]$ in $p[n]$ are $q_n - 3$ times larger than those proportional to $b_{k,r\text{-error}}[n]$ (e.g., $q_n \cong 16$ in the design example), so for $K_a = K_b$, the error variance of each $b_{k,r}[n]$ is expected to be larger than that of $a_{k,r}[n]$. Therefore, in order to make the error variance of the $b_{k,r}[n]$ coefficients comparable to that of the $a_{k,r}[n]$ coefficients, K_b has to be smaller than K_a. As shown in Fig. 14, this causes the $b_{k,r}[n]$ coefficients to converge to their ideal values at a slower rate than the $a_{k,r}[n]$ coefficients, so the convergence speed of the MNC technique is limited by K_b. Nonetheless, it follows from Fig. 14 that the $a_{k,r}[n]$ coefficients get close to their ideal values in less than 10^7 reference periods ($\sim$0.4 seconds).

[4]Furthermore, extensive simulations run by the authors in which $p[n]$ was subjected to pessimistic nonlinearities suggest that the convergence of the MNC coefficients is barely affected by nonlinearities in the PEDC.

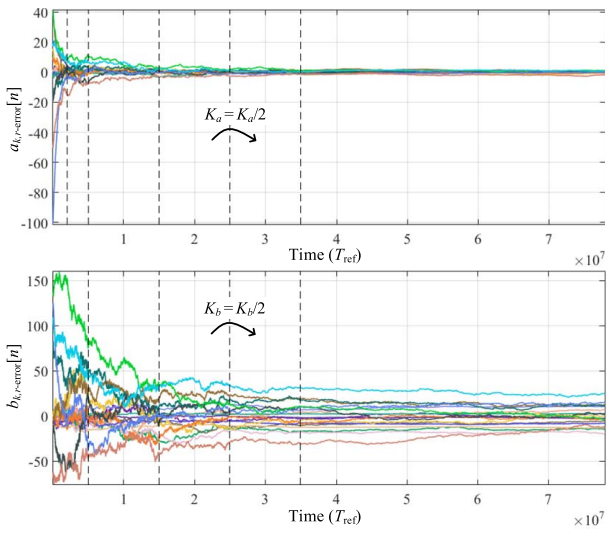

Fig. 15. MNC coefficient error evolution over time for MNC gains that change over time. Initially $K_a = 2^{-1}$ and $K_b = 2^{-2}$, and after $3.5 \cdot 10^7$ reference periods $K_a = 2^{-6}$ and $K_b = 2^{-6}$.

Hence, as the most significant sources of phase noise are the FCE static gain errors, the MNC technique allows for a considerable phase noise improvement in less than half a second.

To reduce the cold-start convergence time of the MNC technique, large MNC gains can be used initially and decreased over time [61]. Fig. 15 shows the evolution of the MNC coefficient errors over time for $7.8 \cdot 10^7$ reference periods (3 seconds) for an example case in which K_a and K_b are initially set to 2^{-1} and 2^{-2}, respectively, and then divided by two at the times indicated by the vertical dashed lines. In this case, the MNC coefficients reach the final values shown in Fig. 14 in roughly 3 seconds, and the $a_{k,r}[n]$ coefficients get close to their ideal values in less than $2 \cdot 10^6$ reference periods (~0.08 seconds), which is five times faster than in Fig. 14.

Appendix A

It follows from Fig. 5 and (17) that

$$f_I(t) = \sum_{i=5}^{22} \left[(b_i[w_t] - 1/2)\, \alpha_i(t)\, \Delta_i + (b_i[w_t - 1] - 1/2)\, \gamma_i(t) \right]. \quad (54)$$

Expressions for each $b_i[w_t] = c_{i+12}[g(w_t)]$ in terms of $d[g(w_t)]$ and the switching sequences can be found by tracing through the tree of Fig. 6 and applying (20) and the expressions shown in Fig. 4(a) and Fig. 4(b). This leads to

$$c_i[g(w_t)] - 1/2 = m_i d[g(w_t)]/\Delta + \sum_{k,r} \kappa_{k,r,i} s_{k,r}[g(w_t)], \quad (55)$$

where

$$m_i = 0 \quad \text{for } 17 \le i \le 26 \quad \text{and } m_i = 2^{-16} \quad \text{for } 27 \le i \le 34, \quad (56)$$

and each $\kappa_{k,r,i}$ is one of 0, $-1/2$, $1/2$, -2^{-k} or 2^{-k}. Combining (4), (19) and (54)-(56) yields (26) and (27), where $\alpha_I(t)$ and $\gamma_I(t)$ are the averages of $\alpha_i(t)$ and $(2^{-13}/\Delta)\gamma_i(t)$ for $i = 15$, 16, …, 22, respectively,

$$\alpha_{k,r}(t) = \sum_{i=5}^{22} \alpha_i(t) K_{i+12} \kappa_{k,r,i+12} \quad \text{and}$$
$$\gamma_{k,r}(t) = \sum_{i=5}^{22} \frac{\gamma_i(t)}{\Delta} \kappa_{k,r,i+12}. \quad (57)$$

Each $\alpha_I(t)$, $\gamma_I(t)$, $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ is T_{fast}-periodic, because it is a linear combination of $\alpha_i(t)$ and $\gamma_i(t)$, which are T_{fast}-periodic.

Appendix B

The phase error of the digital PLL shown in Fig. 9 is given by

$$\theta_{\text{PLL}}(t) = \int_0^t \psi_{\text{PLL}}(u)du, \quad (58)$$

where $\psi_{\text{PLL}}(t)$ is the PLL's frequency error at time t. The $\theta_{\text{PLL}}[n]$ term in (44) is a sampled version of $\theta_{\text{PLL}}(t)$ given by

$$\theta_{\text{PLL}}[n] = \theta_{\text{PLL}}(\tau_n), \quad (59)$$

where $\tau_n = nT_{\text{ref}} + \lambda_n$ and λ_n is a small implementation-dependent deviation of τ_n from its ideal value. It follows from (44), (58) and (59) that

$$p[n] = p[0] - T_{\text{ref}} \sum_{i=1}^{n} \psi_{\text{PLL}}[i] + e_p[n], \quad (60)$$

where

$$\psi_{\text{PLL}}[i] = \frac{1}{T_{\text{ref}}} \int_{\tau_{i-1}}^{\tau_i} \psi_{\text{PLL}}(u)du \quad (61)$$

is the PLL's average frequency error over the time interval $[\tau_{i-1}, \tau_i]$ and $p[0]$ is the initial value of $p[n]$. Fig. 9 and (61) imply that $e_R(t)$ causes a term in $\psi_{\text{PLL}}[i]$ given by

$$\{e_R * h\}[i] = \sum_{j=0}^{\infty} h[j] e_R[i - j], \quad (62)$$

where

$$e_R[i] = \frac{1}{T_{\text{ref}}} \int_{\tau_{i-1}}^{\tau_i} e_R(u)du \quad (63)$$

and $h[j]$ is the impulse response of the highpass filtering operation imposed by the PLL on the DCO's additive frequency error as described in Section VI-B.

In the design example of this paper $\lambda_n = 4.2T_{\text{fast}} + 1/8 T_{\text{fast}} v[n]$, where $v[n]$ is an integer-valued sequence restricted to the set {–6, –5, …, 5, 6}, so $\tau_n = nT_{\text{ref}} + 4.2T_{\text{fast}} + 1/8 T_{\text{fast}} v[n]$. As the magnitude of $1/8 T_{\text{fast}} v[n]$ is at most $3/4 T_{\text{fast}}$, its effect is negligible. Furthermore, for the sake of simplicity, τ_n is assumed to be given by

$$\tau_n = \mu_n + 4T_{\text{fast}}, \quad (64)$$

where μ_n, as shown in Fig. 10(b), is a multiple of T_{fast}. Given that $0 < \mu_n - nT_{\text{ref}} \le T_{\text{fast}}$ for all n and that T_{fast} is a

small fraction of T_{ref}, this approximation does not significantly affect the following results. Substituting (36) with $a_{k,r}$ and $b_{k,r}$ replaced by $a_{k,r}[g(w_t)]$ and $b_{k,r}[g(w_t)]$, respectively, into (35), and the result of this operation and (64) into (63) yields

$$\begin{aligned} e_R[i] &= \frac{\Delta}{T_{\text{ref}}} \sum_{k,r} \int_{\mu_{i-1}+4T_{\text{fast}}}^{\mu_i+4T_{\text{fast}}} \Big\{ \big(\delta_{k,r} - \alpha_F a_{k,r}[g(w_t)]\big)\, s_{k,r}[g(w_t)] \\ &\quad + \big(\gamma_{k,r}(t) - \alpha_F b_{k,r}[g(w_t)]\big) \\ &\quad \times \big(s_{k,r}[g(w_t-1)] - s_{k,r}[g(w_t)]\big)\Big\}\, dt. \end{aligned} \tag{65}$$

Given that $t \in [\mu_n, \mu_{n+1})$ implies $g(p_t) = n-1$, it follows that $g(w_t) = i-2$ for $t \in [\mu_{i-1} + 4T_{\text{fast}},\ \mu_i + T_{\text{fast}})$ and $g(w_t) = i-1$ for $t \in [\mu_i + T_{\text{fast}},\ \mu_i + 4T_{\text{fast}})$, so (65) can be written as

$$e_R[i] = -\Delta \frac{\alpha_F T_{\text{fast}}}{T_{\text{ref}}} \sum_{k,r} \big\{ y_{k,r\text{-}a}[i-1] + y_{k,r\text{-}b}[i-1] \big\}, \tag{66}$$

where $y_{k,r\text{-}a}[i]$ and $y_{k,r\text{-}b}[i]$ are given by (47) and (48), respectively, and it has been assumed that $q_i = (\mu_{i+1} - \mu_i)/T_{\text{fast}}$ is greater than 3 for all i (e.g., $q_i \cong 16$ in the design example). Substituting (66) into (62) and the result into (60), rearranging terms and considering that $s_{k,r}[n] = 0$ for $n < 0$ gives (45) and (46).

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