Comments and Corrections

Errata for "A TDC-Free Mostly-Digital FDC-PLL Frequency Synthesizer With a 2.8–3.5 GHz DCO"

Several errors were made by IEEE during the typesetting process of [1] through no fault of the authors. Although the authors made IEEE aware of these errors prior to publication of [1], an oversight by IEEE prevented three of the errors from being corrected. The errors corrupted the Equations (1), Fig. 11, and Table I in [1], corrected versions of which are as follows:

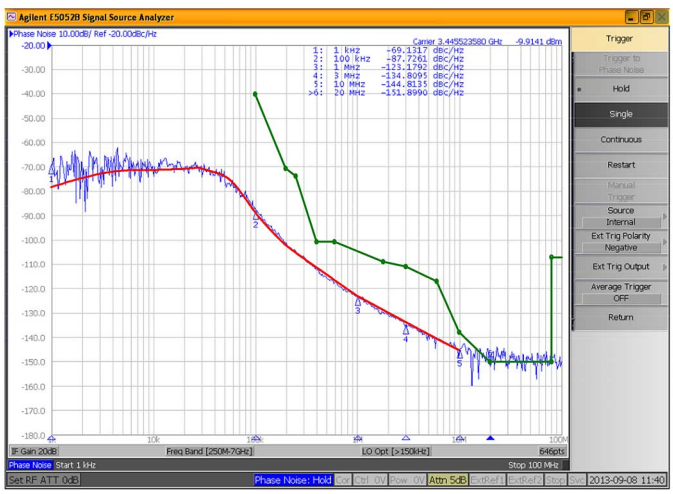

Fig. 11. Representative measured FDC-PLL phase noise spectrum, the corresponding phase noise spectrum predicted by the theoretical results, and the GSM phase noise mask.

$$L_{PI}(z) = K_P + K_I \frac{1}{1-z^{-1}}, \quad L_{LPF}(z) = \prod_{i=0}^{3} \frac{\lambda_i}{1-(1-\lambda_i)z^{-1}} \quad (1)$$

TABLE I
SUPPLY VOLTAGES AND MEASURED CURRENT CONSUMPTION OF THE VARIOUS FDC-PLL CIRCUIT BLOCKS

Circuit	Supply Voltage	Current
Digitally Controlled Oscillator	1.0 V	9.84 mA
Fine-Bank FCE Flip Flops	1.0 V	0.13 mA
DLC, DCO input encoder and ΔΣ modulator	1.0 V	2.04 mA
Charge Pump, PFD, and ADC	1.2 V	1.85 mA
Divider	1.0 V	0.36 mA
Bias Generator	1.2 V	0.96 mA
Crystal Oscillator Buffer	1.2 V	0.65 mA
Divider Buffer and Output Buffer	1.0 V	4.41 mA

REFERENCES

[1] C. Venerus and I. Galton, "A TDC-free mostly-digital FDC-PLL frequency synthesizer with a 2.8–3.5 GHz DCO," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 450–463, Feb. 2015.

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