Adaptive Cancellation of Static and Dynamic Mismatch Error in Continuous-Time DACs

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***Abstract*— Inadvertent but inevitable mismatches among nominally identical unit element 1-bit digital-to-analog converters (DACs) within a multi-bit Nyquist-rate DAC cause both static and dynamic error in the DAC's continuous-time output waveform. Prior calibration techniques are able to suppress static mismatch error, but have had limited success in suppressing dynamic mismatch error. This paper presents a digital calibration technique that adaptively measures and cancels both static and dynamic mismatch error over the DAC's first Nyquist band. The technique is capable of either foreground or background operation, and is relatively insensitive to non-ideal circuit behavior. The paper presents a rigorous mathematical analysis of the technique, and demonstrates the results of the paper with both behavioral and transistor-level circuit simulations.**

***Index Terms*— Digital-to-analog converter, dynamic element matching, mismatch error cancellation.**

I. Introduction

HIGH-RESOLUTION Nyquist-rate DACs with continuous-time output signals are required in critical applications such as wireless transmitters. Each such digital-to-analog converter (DAC) interpolates a discrete-time input sequence to create a continuous-time output signal, so it can be viewed as a device that generates an analog output pulse for each input code. Ideally, the output pulse during the nth clock interval is scaled by the nth input code value, and except for this scale factor all the pulses have the same shape.

Such DACs generally consist of several nominally identical *unit element 1-bit DACs* in parallel. Unfortunately, inadvertent but inevitable fabrication mismatches among the unit element 1-bit DACs often limit performance. The mismatches cause non-ideal deviations of both the scale factor and shape of each overall DAC output pulse. Error in the overall DAC's output waveform from mismatch-induced pulse scale factor deviations is called *static mismatch error* and that from mismatch-induced pulse shape deviations is called *dynamic mismatch error*. Both types of error can significantly limit performance in practice.

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Of course, there are many other types of non-ideal circuit behavior that contribute error in addition to static mismatch error and dynamic mismatch error. For example, if any of the unit element 1-bit DAC output waveforms depend on prior DAC input values in addition to the current DAC input value, a type of dynamic error called inter-symbol interference (ISI) is introduced. Nevertheless, these other types of error can be mitigated to a large extent by known circuit and system-level techniques. The same is true of static mismatch error. In contrast, prior techniques have been less successful in mitigating dynamic mismatch error.

Dynamic element matching (DEM) and digital calibration have been applied to address this problem in prior work, but with mixed results. DEM has been shown to prevent both static and dynamic mismatch error from causing nonlinear distortion, but it does so at the expense of degrading signal-to-noise ratio (SNR) [1]–[4]. Digital calibration techniques have been demonstrated that reduce static mismatch error, but prior calibration techniques do not significantly reduce dynamic mismatch error [5]–[11].

The difficulty arises from a fundamental property of continuous-time output DACs. Each DAC output pulse has a bandwidth that far exceeds the DAC's signal bandwidth, because the pulse's duration is limited to one clock interval. Hence, any technique to cancel dynamic mismatch error must either have a bandwidth that is much wider than the DAC's signal bandwidth, or must somehow perform frequency selective cancellation over a particular band of interest such as the first Nyquist band. The situation is different in systems that only use sampled versions of DAC output signals, such as switched-capacitor delta-sigma ADCs and pipelined ADCs, and well-known techniques have been developed to cancel or otherwise suppress the effects of component mismatches in such cases [12]–[14]. Unfortunately, these techniques are not applicable to DACs with continuous-time output signals that are not resampled such as in wireless transmitters.

This paper proposes a mismatch noise cancellation (MNC) technique that addresses this problem. The MNC technique consists of a feedback path around a main DEM DAC. The feedback path adaptively measures and cancels both static and dynamic mismatch error within the DEM DAC's first Nyquist band. The feedback path consists of an ADC, digital signal processing logic, and a correction DAC. As demonstrated in the paper, the performance requirements of the ADC and correction DAC are modest compared to the overall system performance.

The feedback path forms an estimate of the Nyquist-band portion of the main DEM DAC's static and dynamic mismatch

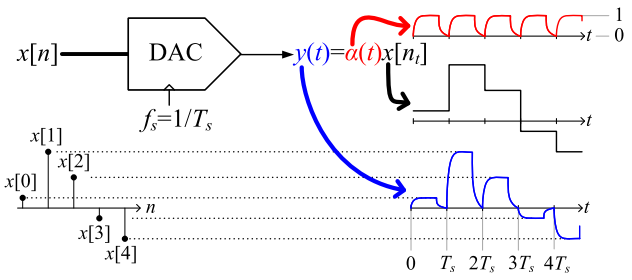

Fig. 1. Desired DAC behavior.

error by driving the correction DAC with the sum of the outputs of multiple digital filters driven by different pseudo-random digital sequences. The pseudo-random sequences are generated explicitly within the main DAC's DEM logic so they are known a priori, but the filter coefficients depend on the component mismatches, so they must be estimated by the MNC technique. The feedback path correlates a digitized version of the overall system's analog output waveform by time-shifted versions of each pseudo-random sequence and uses the results to adaptively estimate the filter coefficients. Thus, the feedback path implements several feedback loops that operate in parallel.

The MNC technique functions regardless of the DAC's input sequence, so it can be used in both foreground and background calibration modes. The convergence rate can be maximized in foreground mode, though, so foreground mode can be used to minimize the initial convergence time and background mode can be used to adaptively track out temperature variation effects.

The paper describes the proposed MNC technique in detail, presents a rigorous mathematical convergence-rate analysis, and presents simulation results. Section II presents DEM DAC background information. Section III describes the MNC technique and its analysis in detail. Section IV presents behavioral and transistor-level simulation results that support the theoretical findings of the paper.

II. Background Information

A. Ideal Behavior of a Practical DAC

As illustrated in Fig. 1, a DAC converts a discrete-time digital sequence, $x[n]$, with a sample-rate of f_s, into a continuous-time analog waveform, $y(t)$. The ideal output of a practical DAC is

$$y(t) = \alpha(t)x[n_t] \quad \text{where } n_t = \lfloor f_s t \rfloor, \tag{1}$$

and $\alpha(t)$ is a periodic *pulse shaping waveform* with period $1/f_s$.[1] It can be verified that the continuous-time Fourier transform of $y(t)$ is

$$Y(j\omega) = X\left(e^{j\omega T_s}\right) A_p(j\omega) \tag{2}$$

[1]By definition, n_t is the largest integer less than or equal to $f_s t$ at time t, so it is a continuous-time waveform. Hence, $x[n_t]$ is a continuous-time waveform even though $x[n]$ is a discrete-time sequence.

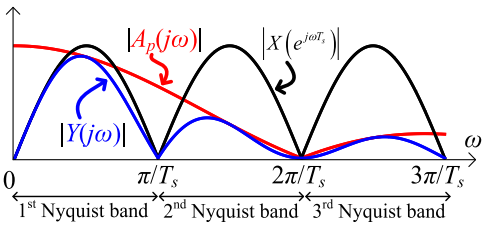

Fig. 2. Example DAC spectra.

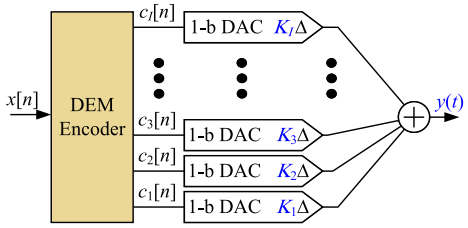

Fig. 3. General form of a DEM DAC.

where $X(e^{j\omega})$ is the discrete-time Fourier transform of $x[n]$, $A_p(j\omega)$ is the continuous-time Fourier transform of

$$\alpha_p(t) = \begin{cases} \alpha(t) & \text{if } 0 \le t \le T_s, \\ 0, & \text{otherwise,} \end{cases} \tag{3}$$

and $T_s = 1/f_s$ is the sample period of the DAC [15].

Example spectra are shown in Fig. 2. The periodicity of the discrete-time Fourier transform gives rise to multiple *Nyquist bands*, three of which are shown in the figure.[2] A practical DAC is designed to faithfully represent its input sequence over a single Nyquist band, most commonly the first Nyquist band. Strictly speaking, this would require that $A_p(j\omega)$ have a magnitude of unity and a constant group delay over the desired Nyquist band, which is not easy to achieve with practical circuits. However, a digital filter can be inserted between $x[n]$ and the DAC's input to compensate for deviations of $A_p(j\omega)$ from unity magnitude and constant group delay over the desired Nyquist band. Therefore, moderate deviations of $A_p(j\omega)$ from unity magnitude and constant group delay over the desired Nyquist band are not problematic in practice.

B. Dynamic Element Matching

Fig. 3 shows the general form of a DEM DAC for an input sequence which takes on values in the range $\{-1/2\ L\Delta,\ \Delta - 1/2\ L\Delta, 2\Delta - 1/2\ L\Delta, \ldots, L\Delta - 1/2\ L\Delta\}$, where L is the number of input levels minus one and Δ is the DAC's minimum input step-size [3]. The DEM DAC consists of an all-digital DEM encoder followed by I 1-bit DACs, the outputs of which are summed to form $y(t)$. The output of the ith 1-bit DAC has the form

$$y_i(t) = \left(c_i[n_t] - \tfrac{1}{2}\right) K_i \Delta + e_i(t) \tag{4}$$

where the 1-bit DAC's f_s-rate input bit sequence, $c_i[n]$, takes on values of 1 and 0, K_i is a constant called the 1-bit DAC's weight, and $e_i(t)$ represents all deviations from pure two-level

[2]The kth Nyquist band for $k = 1, 2, \ldots$, is defined as the set of frequencies that satisfy $\pi\ (k-1) f_s < |\omega| < \pi k f_s$.

behavior including effects such as intentional pulse-shaping and unintentional error from non-ideal analog circuit behavior.

By design, each K_i is an integer, $K_1 = 1$, and $K_{i-1} \leq K_i \leq K_1 + K_2 + \cdots + K_{i-1} + 1$ for $i = 2, 3, \ldots, I$ [16]. In practice, 1-bit DAC weights of $K_i > 1$ are implemented by combining multiple unit element 1-bit DACs in parallel. Thus, the ith 1-bit DAC consists of K_i unit element 1-bit DACs in parallel.

The DEM encoder maps each input sample, $x[n]$, to I output bits, $c_i[n]$, for $i = 1, 2, \ldots, I$, under the constraint

$$x[n] = \sum_{i=1}^{I} K_i \left(c_i[n] - \frac{1}{2} \right) \Delta . \tag{5}$$

This constraint is sufficient to ensure that the DEM DAC satisfies (1) with $\alpha(t) = 1$ if $e_i(t) = 0$ for every 1-bit DAC and that the number of input levels, L, is $K_1 + K_2 + \cdots + K_I$ [16].

In practice, $e_i(t)$ in (4) is often well-modeled as

$$e_i(t) = \begin{cases} e_{11i}(t), & \text{if } c_i[n_t - 1] = 1, \quad c_i[n_t] = 1, \\ e_{01i}(t), & \text{if } c_i[n_t - 1] = 0, \quad c_i[n_t] = 1, \\ e_{00i}(t), & \text{if } c_i[n_t - 1] = 0, \quad c_i[n_t] = 0, \\ e_{10i}(t), & \text{if } c_i[n_t - 1] = 1, \quad c_i[n_t] = 0, \end{cases} \tag{6}$$

where $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$, are T_s-periodic waveforms corresponding to the four different possibilities of the current and previous 1-bit DAC input bit values [15]. During any given T_s clock period, $e_i(t)$ is equal to exactly one of the $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ waveforms, so $e_i(t)$ is non-periodic and signal-dependent in general.

In DEM DACs, the 1-bit DAC weights by design are such that for most values of $x[n]$ there are multiple distinct sets of DEM encoder output bit values that satisfy (5). During each T_s clock period, the DEM encoder sets its output bits to one of these sets chosen as a function of a pseudo-random variable and, when spectral shaping of the DEM DAC error is required, also as a function of past input samples. This causes

$$y(t) = \alpha(t) x[n_t] + \beta(t) + e_{DAC}(t) \tag{7}$$

where $\alpha(t)$ and $\beta(t)$ are T_s-periodic functions of $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ that are independent of the type of DEM used, and $e_{DAC}(t)$ is an error waveform, called DAC noise, that depends on the type of DEM used, $x[n]$, and $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ [15]. The first term on the right side of (7) corresponds to the ideal DAC behavior given by (1). The $\beta(t)$ term is T_s-periodic so it consists only of tones at multiples of f_s. As these tones do not fall within any Nyquist band of the DAC output and do not depend on the DAC input, they do not cause significant problems in most DAC applications. Hence, $e_{DAC}(t)$ is the only significant undesirable component of the DAC output.

It can be shown that (6) implies that $e_{DAC}(t)$ contains two types of error in general, one that depends only on the current DEM DAC input sample, and one that depends on both the prior and current DEM DAC input samples [15]. The first type of error is caused by mismatches among the nominally identical unit element 1-bit DACs, so it is the sum of all static mismatch error and dynamic mismatch error, and is called mismatch noise. The second type of error results from non-ideal memory effects *within* each unit element 1-bit DAC that cause $e_i(t)$ to depend not only on $c_i[n_t]$ but also on $c_i[n_t - 1]$. Hence, this latter type of error is ISI error.

DEM causes the mismatch noise to be a pseudo-random noise waveform that is free of nonlinear distortion, and in some cases spectrally shaped so as to minimize the noise within a desired frequency band. DEM causes much of the ISI error to be a pseudo-random waveform too, but even with DEM the ISI error contains a second-order distortion component. If DEM were not used (i.e., if the encoder were to choose only one of the possible sets of output bits for each given input value), (7) would still hold, but $e_{DAC}(t)$ would be a deterministic high-order nonlinear function of $x[n]$.

III. Mismatch Noise Cancellation Technique

A. Problem Statement

DEM DACs achieve high linearity by effectively converting much of what would otherwise be nonlinear distortion into pseudo-random noise. While often preferable to nonlinear distortion, the noise is nevertheless a problem in wideband analog signal generation applications.

In the absence of ISI, if all of the unit element 1-bit DACs were perfectly matched and clocked at exactly the same time, then $e_{DAC}(t)$ would be zero. In this case, the $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ waveforms would differ from 1-bit DAC to 1-bit DAC only by the ideal 1-bit DAC scale factors, K_i. However, mismatches among the unit element 1-bit DACs including relative skew among their clock signals inevitably result from random errors introduced during fabrication as well as from systematic circuit design and layout constraints. Some of these errors change the scale factors of the $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ waveforms thereby giving rise to static mismatch error in the DAC's output waveform. Others change the relative shapes of the $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ waveforms across the 1-bit DACs thereby giving rise to dynamic mismatch error in the DAC's output waveform. As examples, in current steering 1-bit DACs, threshold voltage mismatches among the current source transistors contribute static mismatch error whereas capacitance mismatches and clock skew contribute dynamic mismatch error.

The objective of the proposed MNC technique is to adaptively measure and cancel the entire mismatch noise component of $e_{DAC}(t)$ over the first Nyquist band, which includes both static and dynamic mismatch error. The MNC technique cancels only a portion of the ISI error component of $e_{DAC}(t)$, so it should be applied to DEM DACs in which ISI error is not the dominant type of error. This requires that the rise and fall transients of each unit element 1-bit DAC are sufficiently well matched or else that return-to-zero (RZ) 1-bit DACs are used. RZ 1-bit DACs reset their outputs to a fixed value (usually zero) at the end of each T_s clock period. This causes $e_{00i}(t) = e_{10i}(t)$ and $e_{11i}(t) = e_{01i}(t)$ in (6), so ISI is avoided because $e_i(t)$ does not depend on past values of $c_i[n]$.

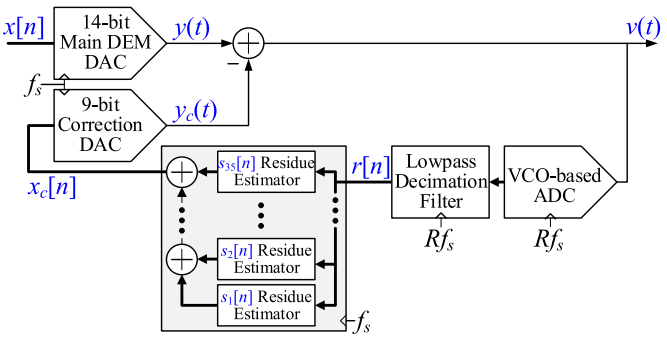

Fig. 4. Proposed MNC technique applied to a main DEM DAC.

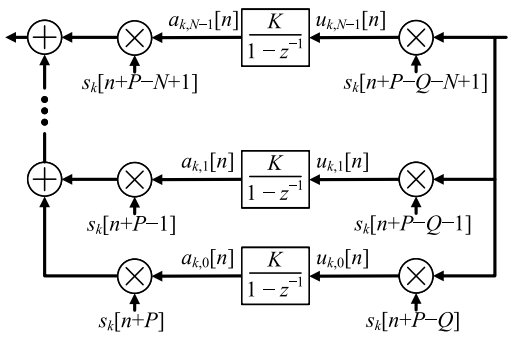

Fig. 5. Details of each $s_k[n]$ residue estimator.

B. Proposed Solution

The MNC technique is explained below in the context of a design example that targets an effective number of bits (ENOB) of 13.5 over a 200 MHz first Nyquist band. The purpose of presenting the MNC technique in the context of the design example is to simplify the explanation, but the technique is not restricted to the specific design example details.

Fig. 4 shows a high-level block diagram of the design example system. It consists of a main DAC and a feedback path. The feedback path consists of a VCO-based oversampling ADC of the type described in [17] with an oversampling ratio of $R = 5$, a digital lowpass decimation filter, a bank of digital residue error estimators, and a correction DAC. The details of each block and the overall system's theory of operation are described in the remainder of this section and in Section IV, respectively.

The main DAC is a 14-bit DEM DAC with a DEM encoder of the type described in [3], 36 current-steering RZ 1-bit DACs, and a clock rate of $f_s = 400$ MHz. As shown in [16], it converts the input sequence, $x[n]$, into an analog waveform, $y(t)$, given by (7) with

$$e_{DAC}(t) = \sum_{k=1}^{35} d_k(t) s_k[n_t] \tag{8}$$

where each $d_k(t)$ is a T_s-periodic linear combination of the 36 sets of $e_{00i}(t)$, $e_{01i}(t)$, $e_{10i}(t)$, and $e_{11i}(t)$ waveforms, and the $s_k[n]$ sequences for $k = 1, 2, \ldots, 35$ are white random sequences that are uncorrelated with $x[n]$, uncorrelated with each other, zero-mean, and restricted to values of -1, 0, and 1. The DEM encoder randomly chooses the sign of $s_k[n]$ independently for all k and n, so all non-zero values of $s_k[n]$ are zero-mean, independent random variables. As the $d_k(t)$ waveforms are functions of component mismatches, they are not known a priori. In contrast, the $s_k[n]$ sequences are generated explicitly within the DEM encoder, so they are known to the system a priori.

Like the main DAC, the correction DAC is based on current-steering 1-bit DACs, and both DACs have differential outputs. The differencing operation in Fig. 4 is implemented at the circuit level by simply connecting the negative and positive outputs of the correction DAC to the positive and negative outputs, respectively, of the main DAC.

Although not shown explicitly in Fig. 4, the output of the bank of error residue estimators is re-quantized to have the same minimum step-size as the correction DAC. This step-size must be small enough that both the quantization error and any additional error introduced by the correction DAC have negligible effects on the performance of the overall system. It was found that a step-size equal to a quarter of that of the main DAC is more than sufficient to meet this objective. The maximum swing of the main DAC's output, $y(t)$, is much greater than that of $e_{DAC}(t)$ in practice, so the maximum swing of the correction DAC need only be a fraction of that of the main DAC. This makes it practical for the correction DAC's resolution to be modest despite its reduced minimum step-size relative to that of the main DAC. Accordingly, in this design example the correction DAC has a resolution of 9-bits and does not incorporate DEM.

The VCO-based ADC and lowpass decimation filter are designed such that the f_s sample-rate output of the decimation filter is equivalent to a digitized version of just the first Nyquist band of the overall output, $v(t)$. Although the design example system has a 200 MHz Nyquist band and an ADC oversampling ratio of $R = 5$, simulation results suggest that fairly high ADC noise and nonlinear distortion can be tolerated. In particular, they indicate that the noise and nonlinear distortion introduced by the VCO-based ADC prototype in [17] would negligibly affect the performance of the feedback loop even without the digital linearization described in [17]. They also indicate that the high input impedance of the ADC would negligibly load the outputs of the DACs.

The $s_k[n]$ residue estimators in Fig. 4 for $k = 1, 2, \ldots, 35$ are digital blocks that together generate the correction DAC's input sequence. Each $s_k[n]$ residue estimator is responsible for adaptively generating an output sequence that contributes a component in the correction DAC's output equal to the portion of the kth term in (8) over the first Nyquist band.

The details of the $s_k[n]$ residue estimator for each k are shown in Fig. 5, wherein N, P, Q, and K have values of 9, 3, 15, and $6 \cdot 10^{-5}$, respectively, for the example system. As described in more detail shortly, N represents a tradeoff between cancellation accuracy and digital complexity, P and Q are chosen according to the delay and impulse response spread, respectively, of the MNC feedback path, and K represents a tradeoff between MNC convergence speed and accuracy.

The $s_k[n]$ residue estimator consists of Nf_s-rate channels, the inputs of which are the decimation filter output sequence, $r[n]$, and the outputs of which are summed to form the $s_k[n]$ residue estimator's output. The mth channel multiplies the decimation filter output by a time-shifted version of the $s_k[n]$ sequence, accumulates the result to generate a sequence $a_{k,m}[n]$, and multiplies $a_{k,m}[n]$ by another time-shifted version of the $s_k[n]$ sequence. As described above, the $s_k[n]$ sequences are restricted to values of -1, 0, and 1 which greatly simplifies the multipliers, and they are known to the system because they are calculated explicitly within the main DAC's DEM encoder. P-sample advanced versions of the $s_k[n]$ sequences are required, but this is not an issue provided $x[n]$ is known P samples in advance.

It can be seen from Fig. 5 that the output of the $s_k[n]$ residue estimator can be written as

$$\sum_{m=0}^{N-1} h_k[m]s_k[n+P-m]. \tag{9}$$

where $h_k[m] = a_{k,m}[n]$ for $m = 0, 1, \ldots, N-1$. It follows that the output of the $s_k[n]$ residue estimator is equivalent to the output of an N-tap FIR filter with input $s_k[n+P]$ and impulse response $h_k[m]$. The filter is not time-invariant because the impulse response evolves over time, n. As proven in Section IV, the feedback system causes the impulse response to adaptively converge such that the correction DAC's output contains a component equal to the portion of the kth term in (8) over the first Nyquist band. Therefore, the bank of $s_k[n]$ residue estimators in Fig. 4 can be viewed as the bank of adaptive FIR filters shown in Fig. 6, where $H_k(z)$ denotes the z-transform of $h_k[m]$.

C. Mismatch Noise Cancellation Principle

Even though the correction DAC does not incorporate DEM, its output has the same form as (7), i.e.,

$$y_c(t) = \alpha_c(t)x_c[n_t] + \beta_c(t) + e_{DAC\text{-}c}(t) \tag{10}$$

where the subscript c is used to distinguish the various terms from their main DAC counterparts, except $e_{DAC\text{-}c}(t)$ is harmonic distortion rather than noise [18]. Analysis as well as transistor-level simulations with realistic mismatches indicate that the correction DAC's minimum step-size is sufficiently small relative to that of the main DAC that $e_{DAC\text{-}c}(t)$ is negligible relative to $e_{DAC}(t)$. Hence, $e_{DAC\text{-}c}(t)$ is neglected in the analysis below. The $\beta_c(t)$ term is also neglected, because it does not have any components within the first Nyquist band, so it does not interfere with the cancelation process.

Therefore, by the same reasoning that led to (2), the continuous-time Fourier transform of the correction DAC output over the first Nyquist band is well-approximated as

$$Y_c\left(j\omega\right) = X_c\left(e^{j\omega T_s}\right) A_{p\text{-}c}\left(j\omega\right) \tag{11}$$

where $X_c(e^{j\omega})$ is the discrete-time Fourier transform of $x_c[n]$ and $A_{p\text{-}c}(j\omega)$ is the continuous-time Fourier transform of the right side of (3) with $\alpha(t)$ replaced by $\alpha_c(t)$. Also by the same reasoning that led to (2), the continuous-time Fourier transform of (8) is

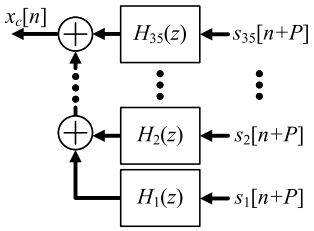

Fig. 6. Equivalent behavior of the $s_k[n]$ residue estimator bank.

$$E_{DAC}\left(j\omega\right) = \sum_{k=1}^{35} S_k\left(e^{j\omega T_s}\right) D_{p\text{-}k}\left(j\omega\right) \tag{12}$$

where $S_k(e^{j\omega})$ is the discrete-time Fourier transform of $s_k[n]$ and $D_{p\text{-}k}(j\omega)$ is the continuous-time Fourier transform of the right side of (3) with $\alpha(t)$ replaced by $d_k(t)$. To cancel $e_{DAC}(t)$ over the first Nyquist band it is necessary for (11) and (12) to equal each other for all $|\omega| < \pi f_s$. It follows from (11), (12), and Fig. 6 that this is achieved if

$$H_k(e^{j\omega}) = e^{-j\omega P}\frac{D_{p\text{-}k}(j\omega)}{A_{p\text{-}c}(j\omega)} \quad \text{for } |\omega| \le \pi f_s \tag{13}$$

The inverse discrete-time Fourier transform of the right side of (13) is the ideal $H_k(z)$ filter impulse response and it is both infinite-length and two-sided, yet the actual $H_k(z)$ filters only have impulse responses that are nonzero for $n = 0, 1, \ldots, N-1$. Consequently, it is not possible to satisfy (13) perfectly. However, (13) represents a stable system, so the ideal impulse response converges to 0 as $n \to \pm\infty$. It follows from (13) that P is just a delay term, so increasing P simply shifts the ideal impulse response to the right. Consequently, P can be chosen large enough that the terms of the ideal impulse response are negligible for $n < 0$. Similarly, N can be chosen large enough that the terms of the ideal impulse response are negligible for $n \ge N$. So choosing N and P ensures that the error incurred by using length-N $H_k(z)$ filters to approximate (13) is negligible. As demonstrated in Section IV, $N = 9$ and $P = 3$ are sufficient to achieve more than 2.5 bits of both static mismatch error and dynamic mismatch error cancellation in the design example system.

It remains to show that the feedback causes $a_{k,m}[n]$ for $m = 0, 1, \ldots, N-1$ and $k = 1, 2, \ldots, 35$ to converge to values that cause (13) to be well approximated. A rigorous analysis that proves this result is presented next.

D. Convergence Analysis

The decimation filter's output can be written as $r[n] = r_{ideal}[n] + r_e[n] + r_c[n]$, where $r_{ideal}[n]$ is the decimation filter output sequence that would have occurred in the absence of both $e_{DAC}(t)$ and the correction DAC feedback loop, $r_e[n]$ is the additional error caused by $e_{DAC}(t)$ that would have occurred in the absence of the correction DAC feedback loop, and $r_c[n]$ is the additional component introduced by the correction DAC feedback loop. Therefore, the objective of the correction DAC feedback loop is to adjust the $a_{k,m}[n]$ values such that $r_c[n] = -r_e[n]$ for all n.

Each term in the summation on the right side of (8) has the form of (1) with $d_k(t)$ playing the role of $\alpha(t)$ and $s_k[n_t]$ playing the role of $x[n_t]$. Consequently, each term can be viewed as being contributed by a separate ideal DAC with input sequence $s_k[n]$ and pulse shaping function $d_k(t)$. It follows that the relationship between $s_k[n]$ and its contribution to $r_e[n]$ must be that of a causal linear time-invariant (LTI) discrete time system. Denoting the impulse response of this LTI system by $b_k[n]$, it follows that

$$r_e[n] = \sum_{k=1}^{35} b_k[n] * s_k[n] = \sum_{k=1}^{35} \sum_{i=0}^{\infty} b_k[i] s_k[n-i]. \quad (14)$$

To the extent that nonlinearity and aliasing from the ADC can be neglected, similar reasoning implies that the relationship between $x_c[n]$ and $r_c[n]$ must also be that of a causal discrete-time LTI system. Hence,

$$r_c[n] = x_c[n] * (-h_c[n]) \quad (15)$$

where $-h_c[n]$ is the LTI system's impulse response (the -1 factor in this definition of $h_c[n]$ simplifies notation in the subsequent analysis). Furthermore, $h_c[n] = 0$ for all $n < 0$ for causality and also for $n = 0$ to prevent the feedback loop from being delay-free.

These observations and the signal processing operations shown in Fig. 4 and Fig. 5 imply that the input to and the output of the mth accumulator in the $s_k[n]$ residue estimator can be written as

$$u_{k,m}[n] = s_k[n-m+P-Q] \left(r_{ideal}[n] + r_e[n] - \sum_{l=1}^{35} \sum_{i=-\infty}^{n-1} \sum_{j=0}^{N-1} h_c[n-i] a_{l,j}[i] s_l[i+P-j] \right), \quad (16)$$

and

$$a_{k,m}[n] = a_{k,m}[n-1] + K u_{k,m}[n], \quad (17)$$

respectively. It follows that $u_{k,m}[n] = 0$ at each value of n for which $s_k[n-m+P-Q] = 0$, so $a_{k,m}[n]$ only changes at values of n for which $s_k[n-m+P-Q] \neq 0$. Given that the only non-zero values of $s_k[n]$ are 1 and -1, this implies that $a_{k,m}[n]$ only changes at values of n for which $s_k^2[n-m+P-Q] = 1$.

Given that the convergence rate of each $a_{k,m}[n]$ sequence depends on the particular pattern of zeros and ones taken on by $s_k^2[n]$ for all n, the expected values of $u_{k,m}[n]$ and $a_{k,m}[n]$ conditioned on this pattern of zeros and ones are of interest. In the following, these conditional expectations are denoted as $\bar{u}_{k,m}[n]$ and $\bar{a}_{k,m}[n]$, respectively. As described above, all non-zero values of $s_k[n]$ are independent zero-mean random variables that take on values of 1 and -1. Furthermore, (16) and (17) imply that $a_{l,j}[n]$ does not depend on $s_k[n']$ for any $n' \geq n + P$. These properties with (14) and (16) imply that

$$\bar{u}_{k,m}[n] = s_k^2[n-m+P-Q] \left(b_k[m-P+Q] - \sum_{l=1}^{35} \sum_{i=n-m-Q}^{n-1} \sum_{j=0}^{N-1} h_c[n-i] E_{l,i,j}[n] \right) \quad (18)$$

where $E_{l,i,j}[n]$ is the mean of $a_{l,j}[i] s_l[i+P-j] s_k[n-m+P-Q]$ conditioned on the pattern of zeros and ones taken on by $s_k^2[n]$ for all n.

By definition, $E_{l,i,j}[n] = \bar{a}_{k,j}[n-m-Q+j] s_k^2[n-m+P-Q]$ when $l = k$ and $i - j = n - m - Q$. Given that K is very small (e.g., $K = 6 \cdot 10^{-5}$ in the design example) it follows from (17) that $a_{l,j}[i]$ is only very weakly correlated with $s_k[n-m+P-Q]$ for all other values of l, i, and j in the triple sum of (18). Hence, any of these terms that are non-zero are very close to zero because all non-zero values of $s_k[n-m+P-Q]$ are independent, zero-mean random variables. Consequently, (18) can be well approximated as

$$\bar{u}_{k,m}[n] = s_k^2[n-m+P-Q] \left(b_k[m-P+Q] - \sum_{j=0}^{N-1} h_c[Q+m-j] \bar{a}_{k,j}[n-m-Q+j] \right) \quad (19)$$

The expectation operator is linear, so (17) implies

$$\bar{a}_{k,m}[n] = \bar{a}_{k,m}[n-1] + K \bar{u}_{k,m}[n]. \quad (20)$$

The set of difference equations given by (20) with $\bar{u}_{k,m}[n]$ given by (19) for $m = 0, 1, \ldots, N-1$ specifies the evolution of the expectation of the coefficients of the kth FIR filter in Fig. 6. However, these difference equations present two analysis complications because of the s_k^2 term in (19). One complication is that the difference equations, while linear, are not time-invariant because the s_k^2 terms are zero for some values of n. The other complication is that the s_k^2 terms across the different equations are not zero for the same values of n.

The latter complication can be solved by replacing n with $n + m$ in each of the difference equations, because, as can be verified from (19), the s_k^2 terms in the expressions for $\bar{u}_{k,m}[n+m]$ are identical for all $m = 0, 1, \ldots, N-1$. The N equations obtained by substituting (19) into (20) for every $m = 0, 1, \ldots, N-1$ and replacing every occurrence of n by $n + m$ can be written in matrix form as

$$\mathbf{a}_k[n] = \mathbf{a}_k[n-1] - \begin{cases} \mathbf{0} & \text{if } s_k[n+P-Q] = 0, \\ K\mathbf{H_c}\mathbf{a}_k[n-Q] - K\mathbf{b}_k, & \text{otherwise,} \end{cases} \quad (21)$$

where

$$\mathbf{a}_k[n] = \begin{bmatrix} \bar{a}_{k,0}[n] \\ \bar{a}_{k,1}[n+1] \\ \vdots \\ \bar{a}_{k,N-1}[n+N-1] \end{bmatrix}, \quad \mathbf{b}_k = \begin{bmatrix} b_k[Q-P] \\ b_k[Q-P+1] \\ \vdots \\ b_k[Q-P+N-1] \end{bmatrix}, \quad (22)$$

and

$$\mathbf{H_c} = \begin{bmatrix} h_c[Q] & h_c[Q-1] & \cdots & h_c[Q-N+1] \\ h_c[Q+1] & h_c[Q] & \cdots & h_c[Q-N+2] \\ \vdots & \vdots & \ddots & \vdots \\ h_c[Q+N-1] & h_c[Q+N-2] & \cdots & h_c[Q] \end{bmatrix}. \quad (23)$$

This is an N-dimensional, Qth-order, time-varying matrix difference equation. It converges if and only if $\mathbf{a}_k[n] \to \mathbf{a}'_k$ as $n \to \infty$ where $\mathbf{a}'_k$ is the constant steady-state solution of (21). Furthermore, if the system converges it follows from taking the limit of (21) as $n \to \infty$ that

$$\mathbf{H_c}\mathbf{a}'_k = \mathbf{b}_k. \quad (24)$$

Defining $\mathbf{z}_k[n] = \mathbf{a}_k[n] - \mathbf{a}'_k$, (21) and (24) imply that

$$\mathbf{z}_k[n] = \begin{cases} \mathbf{z}_k[n-1], & \text{if } s_k[n+P-Q] = 0, \\ \mathbf{z}_k[n-1] - K\mathbf{H_c}\mathbf{z}_k[n-Q], & \text{otherwise,} \end{cases} \quad (25)$$

and the system converges if and only if $\mathbf{z}_k[n] \to \mathbf{0}$ as $n \to \infty$.

If $s_k[n]$ were never zero, then (25) would be a time-invariant as well as linear matrix difference equation. In this case (25) could be rewritten as a QN-dimensional, first-order matrix equation and shown to converge provided the eigenvalues of its system matrix all have magnitude less than one. Unfortunately, $s_k[n] = 0$ for some values of n as described above, which complicates the analysis. A new analysis is presented in the remainder of the section that addresses this problem. The analysis shows that the system parameters can be chosen such that $\mathbf{z}_k[n] \to \mathbf{0}$ as $n \to \infty$ and provides a measure of the convergence rate.

The analysis makes use of the following standard matrix theory definitions and results [19]. For any N-dimensional vector $\mathbf{v} = [v_j]$ and $N \times N$ matrix $\mathbf{A} = [a_{j,k}]$, the *max norm* of $\mathbf{v}$ and the maximum absolute row sum norm of $\mathbf{A}$ are defined as

$$\|\mathbf{v}\| = \max_{1 \le m \le N} |v_m| \text{ and } \|\mathbf{A}\|_1 = \max_{1 \le m \le N} \sum_{n=1}^{N} |a_{m,n}|, \quad (26)$$

respectively, and these definitions imply that

$$\|\mathbf{A}\mathbf{v}\| \le \|\mathbf{A}\|_1 \|\mathbf{v}\|. \quad (27)$$

For any two vectors $\mathbf{v}$ and $\mathbf{w}$ of equal dimension

$$\|\mathbf{v}\| - \|\mathbf{w}\| \le \|\mathbf{v} + \mathbf{w}\| \le \|\mathbf{v}\| + \|\mathbf{w}\|. \quad (28)$$

The following system-related definitions are used by the theorems presented below:

$$r = \frac{1}{h_c[Q]} \sum_{m \ne Q} |h_c[m]|, \quad (29)$$

and

$$g = \frac{\left\|\mathbf{H_c}^2\right\|_1 \left[1 - (1 - 2h_c[Q]K)^{Q-1}\right]}{2h_c^2[Q](1-r)(1-2h_c[Q]K)^{2Q-2}}. \quad (30)$$

The following theorem shows that $\mathbf{z}_k[n] \to \mathbf{0}$ as $n \to \infty$ for the case where the system is started at time $n = 0$ with all registers initialized to zero. It does so by showing that $||\mathbf{z}_k[n]|| \to 0$ as $n \to \infty$. From the definition of $\mathbf{z}_k[n]$, this initial condition implies that $\mathbf{z}_k[n] = -\mathbf{a}'_k$, for all $n < 0$

Theorem 1: If $0 \le r < 1$, $0 < g < 1$, and $\mathbf{z}_k[n] = -\mathbf{a}'_k$ for all $-Q \le n < 0$, then

$$\|\mathbf{z}_k[J_m]\| \le \left\|\mathbf{a}'_k\right\| (1 - K(1-r)(1-g)h_c[Q])^m \quad (31)$$

for all $m \ge 1$, where J_m is the mth largest non-negative integer n for which $s_k[n+P-Q] \ne 0$.

□

As implied by (25), $\mathbf{z}_k[n] = \mathbf{z}_k[n-1]$ when $n \ne J_m$ for any $m = 1, 2, \ldots$, so the theorem implies that $\mathbf{z}_k[n] \to \mathbf{0}$ at least exponentially with the number of times that $s_k[n+P-Q] \ne 0$ over n provided the theorem's hypothesis is satisfied.

As explained below, the conditions placed on $h_c[n]$ and K by the theorem's hypothesis are easy to meet in a practical design, and the dependence of the convergence on how frequently $s_k[n+P-Q]$ is non-zero does not present a problem in practice.

The theorem also gives insight into the choice of Q. The requirement that $0 \le r < 1$ implies that $h_c[Q]$ must be positive and that it must be the maximum value of the impulse response.

Proof of Theorem 1: If $\mathbf{a}'_k = 0$ then (25) implies that $\mathbf{z}_k[n] = \mathbf{0}$ for all $n \ge 0$, so Theorem 1 holds for this case. The remainder of the proof considers the case of $\mathbf{a}'_k \ne 0$.

The proof uses mathematical induction. The *inductive step*, which is proven shortly, is: for any $m = 1, 2, 3, \ldots$, if

$$\frac{\|\mathbf{z}_k[i]\|}{\|\mathbf{z}_k[i-1]\|} \ge 1 - 2h_c[Q]K, \quad (32)$$

for all $-Q+1 \le i < J_m$,[3] then the conditions of the theorem's hypothesis are sufficient to ensure that (32) holds for $i = J_m$ and

$$\frac{\|\mathbf{z}_k[J_m]\|}{\|\mathbf{z}_k[J_m-1]\|} \le 1 - K(1-r)(1-g)h_c[Q]. \quad (33)$$

The induction *base step*, i.e., that (32) holds for $-Q+1 \le i < J_1$, follows directly from (25), the max norm definition in (26), and the condition that $\mathbf{z}_k[n] = -\mathbf{a}'_k$ for all $-Q \le n < 0$. Therefore, given that $\mathbf{z}_k[n] = \mathbf{z}_k[n-1]$ when $n \ge 0$ and $n \ne J_m$ for any $m = 1, 2, \ldots$, provided the inductive step is true, it follows from induction that (32) and (33) hold for all integers $m \ge 1$. Furthermore, recursively applying (33) when $n = J_m$ and $\mathbf{z}_k[n] = \mathbf{z}_k[n-1]$ when $n \ne J_m$ with $\mathbf{z}_k[J_1 - 1] = -\mathbf{a}'_k$ yields (31).

Hence, it remains to show that the inductive step is true. This is done in the remainder of the proof.

For any $m = 1, 2, 3, \ldots$, let $n = J_m$ (to simplify the notation). Then (25) reduces to

$$\mathbf{z}_k[n] = \mathbf{z}_k[n-1] - K\mathbf{H_c}\mathbf{z}_k[n-Q] \quad (34)$$

[3]By limiting the amount that $||\mathbf{z}_k[i]||$ can decrease over each iteration, (32) prevents the possibility of convergence with ringing, which is necessary for (31) to hold.

which can be rewritten as

$$\mathbf{z}_k[n] = \mathbf{z}_k[n-1] - K\mathbf{H_c}\mathbf{z}_k[n-1] - K\mathbf{H_c}\left(\mathbf{z}_k[n-Q] - \mathbf{z}_k[n-1]\right) \quad (35)$$

and further rewritten as

$$\mathbf{z}_k[n] = \left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{z}_k[n-1] - \sum_{m=1}^{Q-1} K\mathbf{H_c}\left(\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]\right). \quad (36)$$

where $\mathbf{I}$ is the $N \times N$ identity matrix. Taking the L_1 norm of (36) and applying (28) multiple times yields

$$\|\mathbf{z}_k[n]\| \le \|\left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{z}_k[n-1]\| + \sum_{m=1}^{Q-1} \|K\mathbf{H_c}\left(\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]\right)\| \quad (37)$$

and

$$\|\mathbf{z}_k[n]\| \ge \|\left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{z}_k[n-1]\| - \sum_{m=1}^{Q-1} \|K\mathbf{H_c}\left(\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]\right)\|. \quad (38)$$

Let $\mathbf{v}$ be any real N-dimensional column vector. Then

$$\|\left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{v}\| = \|(1 - h_c[Q]K)\,\mathbf{v} + K\left(h_c[Q]\mathbf{I} - \mathbf{H_c}\right)\mathbf{v}\|. \quad (39)$$

Applying (27) with $\mathbf{A} = h_c[Q]\mathbf{I} - \mathbf{H_c}$ and (28) to (39) gives

$$\|(\mathbf{I} - K\mathbf{H_c})\mathbf{v}\| \le (1 - h_c[Q]K)\|\mathbf{v}\| + K\|h_c[Q]\mathbf{I} - \mathbf{H_c}\|_1\|\mathbf{v}\| \quad (40)$$

and

$$\|(\mathbf{I} - K\mathbf{H_c})\mathbf{v}\| \ge (1 - h_c[Q]K)\|\mathbf{v}\| - K\|h_c[Q]\mathbf{I} - \mathbf{H_c}\|_1\|\mathbf{v}\|. \quad (41)$$

The requirement that $0 \le r < 1$ and (29) imply that $h_c[Q]$ is positive. This, (23), (26), and (29) imply that $||h_c[Q]\mathbf{I} - \mathbf{H_c}||_1 \le h_c[Q]r$, so (40) and (41) imply

$$\|\left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{v}\| \le \left(1 - h_c[Q]\,K\,(1-r)\right)\|\mathbf{v}\| \quad (42)$$

and

$$\|\left(\mathbf{I} - K\mathbf{H_c}\right)\mathbf{v}\| \ge \left(1 - h_c[Q]\,K\,(1+r)\right)\|\mathbf{v}\|. \quad (43)$$

Substituting $\mathbf{v} = \mathbf{z}_k[n-1]$ into (42) and (43), and the results into (37) and (38) yields

$$\|\mathbf{z}_k[n]\| \le \left(1 - h_c[Q]\,K\,(1-r)\right)\|\mathbf{z}_k[n-1]\| + \sum_{m=1}^{Q-1} \|K\mathbf{H_c}\left(\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]\right)\| \quad (44)$$

and

$$\|\mathbf{z}_k[n]\| \ge \left(1 - h_c[Q]\,K\,(1+r)\right)\|\mathbf{z}_k[n-1]\| - \sum_{m=1}^{Q-1} \|K\mathbf{H_c}\left(\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]\right)\| \quad (45)$$

Equation (25) for $n \ge 0$ and the condition $\mathbf{z}_k[n] = -\mathbf{a}'_k$ for $-Q \le n < 0$ imply that each $\mathbf{z}_k[n-m-1] - \mathbf{z}_k[n-m]$ in (44) and (45) is either $K\mathbf{H_c}\mathbf{z}_k[n-m-Q]$ or $\mathbf{0}$. Consequently,

$$\|\mathbf{z}_k[n]\| \le \left(1 - h_c[Q]\,K\,(1-r)\right)\|\mathbf{z}_k[n-1]\| + \sum_{m=1}^{\min\{Q-1,n\}} \left\|K^2\mathbf{H_c}^2\mathbf{z}_k[n-m-Q]\right\| \quad (46)$$

and

$$\|\mathbf{z}_k[n]\| \ge \left(1 - h_c[Q]\,K\,(1+r)\right)\|\mathbf{z}_k[n-1]\| - \sum_{m=1}^{\min\{Q-1,n\}} \left\|K^2\mathbf{H_c}^2\mathbf{z}_k[n-m-Q]\right\|. \quad (47)$$

Applying (27) with $\mathbf{A} = K^2\mathbf{H_c}^2$ to (46) and (47) yields

$$\|\mathbf{z}_k[n]\| \le \left(1 - h_c[Q]\,K\,(1-r)\right)\|\mathbf{z}_k[n-1]\| + K^2\left\|\mathbf{H_c}^2\right\|_1 \sum_{m=1}^{\min\{Q-1,n\}} \|\mathbf{z}_k[n-m-Q]\| \quad (48)$$

and

$$\|\mathbf{z}_k[n]\| \ge \left(1 - h_c[Q]\,K\,(1+r)\right)\|\mathbf{z}_k[n-1]\| - K^2\left\|\mathbf{H_c}^2\right\|_1 \sum_{m=1}^{\min\{Q-1,n\}} \|\mathbf{z}_k[n-m-Q]\|. \quad (49)$$

Recursively applying (32) to itself for $i = 2, 3, 4, \ldots n+Q$, yields

$$\|\mathbf{z}_k[n-i]\| \le \|\mathbf{z}_k[n-1]\|\left(1 - 2h_c[Q]\,K\right)^{-i+1}. \quad (50)$$

Hence,

$$\sum_{m=1}^{\min\{Q-1,n\}} \|\mathbf{z}_k[n-m-Q]\| \le \|\mathbf{z}_k[n-1]\| \times \sum_{m=1}^{Q-1}\left(1 - 2h_c[Q]\,K\right)^{-m-Q+1}. \quad (51)$$

The right side of (51) can be expanded via the geometric series formula as

$$\frac{1 - \left(1 - 2h_c[Q]\,K\right)^{Q-1}}{2h_c[Q]\,K\left(1 - 2h_c[Q]\,K\right)^{2Q-2}}. \quad (52)$$

Substituting (52) into (51) and the result into (48) and (49) yields

$$\frac{\|\mathbf{z}_k[n]\|}{\|\mathbf{z}_k[n-1]\|} \le 1 - h_c[Q]\,K\,(1-r) + K\left\|\mathbf{H_c}^2\right\|_1 \frac{1 - \left(1 - 2h_c[Q]\,K\right)^{Q-1}}{2h_c[Q]\left(1 - 2h_c[Q]\,K\right)^{2Q-2}} \quad (53)$$

and

$$\frac{\|\mathbf{z}_k[n]\|}{\|\mathbf{z}_k[n-1]\|} \ge 1 - h_c[Q]\,K\,(1+r) - K\left\|\mathbf{H_c}^2\right\|_1 \frac{1 - \left(1 - 2h_c[Q]\,K\right)^{Q-1}}{2h_c[Q]\left(1 - 2h_c[Q]\,K\right)^{2Q-2}} \quad (54)$$

Given that $n = J_m$, substituting (30) into (53) results in (33) and substituting (30) into (54) results in

$$\frac{\|\mathbf{z}_k[J_m]\|}{\|\mathbf{z}_k[J_m-1]\|} \geq 1 - h_c[Q]\,K\,(1+r) - h_c[Q]\,K\,(1-r)\,g. \tag{55}$$

This finishes the proof because (55) implies that (32) with $i = n$ is satisfied provided $g < 1$. □

Theorem 2 extends the result of Theorem 1 to cover all possible initial conditions. It shows that while the specific form of $\mathbf{z}_k[n]$ depends on the system's initial conditions, the convergence of $||\mathbf{z}_k[n]||$ is still exponential for any K and $h_c[n]$ that satisfy the hypothesis of Theorem 1 regardless of the initial conditions.

Theorem 2: Provided $0 \leq r < 1$ and $0 < g < 1$, $\mathbf{z}_k[n]$ can be written as

$$\mathbf{z}_k[n] = \sum_{j=1}^{Q} \mathbf{z}_{k,j}[n], \tag{56}$$

where for every $J_m \geq Q - j$,

$$\left\|\mathbf{z}_{k,j}[J_m]\right\| \leq \left(1 - K\,(1-r)\,(1-g)\,h_c[Q]\right)\left\|\mathbf{z}_{k,j}[J_m-1]\right\|, \tag{57}$$

and for all non-negative $n \neq J_m$

$$\left\|\mathbf{z}_{k,j}[n]\right\| = \left\|\mathbf{z}_{k,j}[n-1]\right\|. \tag{58}$$

□

Proof: Let $\mathbf{z}_{k,j}[-1], \mathbf{z}_{k,j}[-2], \ldots, \mathbf{z}_{k,j}[-Q]$ for $j = 1, 2, \ldots, Q$, be

$$\mathbf{z}_{k,j}[n] = \begin{cases} \mathbf{z}_k[-j] - \mathbf{z}_k[-j-1], & \text{if } j < Q, \quad -j \leq n < 0, \\ \mathbf{0}, & \text{if } j < Q, \quad -Q \leq n < -j \\ \mathbf{z}_k[-Q], & \text{if } j = Q, \quad -Q \leq n < 0, \end{cases} \tag{59}$$

It can be verified by substituting (59) into (56) that (59) is a solution of (56) for $-Q \leq n < 0$. It follows from (25) that $\mathbf{z}_k[n]$ for all $n \geq 0$ is uniquely determined by (25) and the values of $\mathbf{z}_k[n]$ for $-Q \leq n < 0$. Consequently, $\mathbf{z}_k[n]$ for all $n \geq 0$ is uniquely determined by (25), (56), and (59).

Equation (25) is a linear matrix difference equation, so, as can be seen by substituting (56) into (25), $\mathbf{z}_{k,j}[n]$ for $n \geq 0$ can be defined as

$$\mathbf{z}_{k,j}[n] = \begin{cases} \mathbf{z}_{k,j}[n-1], & \text{if } s_k[n+P-Q] = 0, \\ \mathbf{z}_{k,j}[n-1] - K\mathbf{H_c}\mathbf{z}_{k,j}[n-Q], & \text{otherwise.} \end{cases} \tag{60}$$

This with (59) completely specifies $\mathbf{z}_{k,j}[n]$ for $n \geq -Q$.

It follows from (60) and the definition of J_m that (58) holds for all non-negative $n \neq J_m$, so it remains to show that (57) holds for all $J_m \geq Q - j$. This is done below by induction.

For all $n \geq 0$, (60) implies that $\mathbf{z}_{k,j}[n] = 0$ if $\mathbf{z}_{k,j}[-1], \mathbf{z}_{k,j}[-2], \ldots, \mathbf{z}_{k,j}[-Q]$ are all zero. In this case, (57) holds for all $J_m \geq Q - j$, and (58) holds for all non-negative $n \neq J_m$. All other cases are considered in the remainder of the proof.

As can be seen from (59), the first j values of $\mathbf{z}_{k,j}[-1], \mathbf{z}_{k,j}[-2], \ldots, \mathbf{z}_{k,j}[-Q]$ are non-zero and equal, and the remaining $Q - j$ values are $\mathbf{0}$. This and (60) imply that all Q values of $\mathbf{z}_{k,j}[n+Q-j]$ for $n = -Q, -Q+1, \ldots, -2, -1$ are non-zero and equal. Therefore, by exactly the same reasoning used for the induction base step in the proof of Theorem 1,

$$\frac{\left\|\mathbf{z}_{k,j}[i]\right\|}{\left\|\mathbf{z}_{k,j}[i-1]\right\|} \geq 1 - 2h_c[Q]\,K, \tag{61}$$

for all $-j+1 \leq i < J_p$. where p is the smallest integer for which $J_p \geq Q - j$. This is the induction *base step*.

By exactly the same reasoning used in the proof of Theorem 1, the following inductive step holds for each $\mathbf{z}_{k,j}[n]$: for any $m = p, p+1, p+2, p+3, \ldots$, if (61) holds for all $-j+1 \leq i < J_m$ then the conditions of the theorem's hypothesis are sufficient to ensure that (61) holds for $i = J_m$ and (57) holds.

It follows from induction that (57) holds for all $J_m \geq Q - j$. □

Theorems 1 and 2 provide conditions for which the convergence of $||\mathbf{z}_k[n]||$ is bounded from above by a decaying exponential sequence. The following corollary shows that these same conditions ensure that the convergence of $||\mathbf{z}_k[n]||$ is also bounded from below by a decaying exponential sequence.

Corollary: Provided $0 \leq r < 1$ and $0 < g < 1$,

$$\|\mathbf{z}_{k,j}[J_m]\| \geq (1 - K(2-(1-r)(1-g))h_c[Q])\|\mathbf{z}_{k,j}[J_m-1]\|, \tag{62}$$

for every $J_m \geq Q - j$.

Proof: The proof follows directly from that of Theorem 2.

E. Noise Versus Convergence Rate Tradeoff

As described in Section III-C, the MNC technique causes the impulse responses of the adaptive filters shown in Fig. 6, i.e., $h_k[m] = a_{k,m}[n]$ for $m = 0, 1, \ldots, N-1$ and $k = 1, 2, \ldots, 35$, to converge toward their ideal values as $n \to \infty$. As shown in Section III-D, the $a_{k,m}[n]$ coefficients are well-modelled as random variables with means that converge to their ideal values as $n \to \infty$. Thus, once the convergence transient has died out, each $a_{k,m}[n]$ is equal to its ideal value plus zero-mean noise.

As with most adaptive filter analyses, the analysis of Section III-D does not provide insight into the variance of the noise component in each $a_{k,m}[n]$ sequence. It does not even rule out the possibility that the variance could diverge as $n \to \infty$, which, of course, would be catastrophic for the MNC technique. Fortunately, intuitive reasoning and extensive simulations run by the authors, some of which are presented in Section IV, indicate that the variance of the noise can be made arbitrarily small by reducing the feedback loop gain, K. Specifically, it is reasonable to expect from (17) that reducing K reduces the sample-to-sample variability, and therefore the variance, of the noise component of $a_{k,m}[n]$. Simulation results presented in the next section bear this out. This and the results of Section III-D imply the usual tradeoff

between convergence rate and accuracy in adaptive systems. Reducing K reduces the convergence error variance, but it also reduces the convergence rate.

At first glance it might also appear that there is a tradeoff between the convergence rate and how frequently non-zero values of each $s_k[n]$ sequence occur. As described in [16], the values of n for which $s_k[n] = 0$ are partly dependent on the DEM DAC's input sequence, so it follows from the results of Section III-D that the convergence rate of $a_{k,m}[n]$ has a dependency on the DEM DAC's input sequence. For example, if the input sequence were such that $s_k[n] = 0$ for all n, then $a_{k,m}[n]$ would remain constant. On the other hand, it can be seen from (8) that the error term in $e_{DAC}[n]$ corresponding to $s_k[n]$ would be zero for this case, so the lack of convergence would not be a problem. More generally, the less frequently non-zero values of each $s_k[n]$ sequence occur, the slower the convergence rate with n but the lower the noise introduced by the corresponding term in $e_{DAC}[n]$. These two effects tend to cancel each other out in practice.

It can be seen from Figures 4 and 5 that a change in the ADC gain is mathematically equivalent to a change in K. Therefore, any variations in the ADC gain simply change the tradeoff between the convergence error variance and the convergence rate. This suggests that the system is not highly sensitive to ADC gain variations such as might be caused by temperature variations during background calibration. Indeed, simulation results performed by the authors during which the ADC gain was varied by up to 50% during background calibration showed negligible effect on MNC accuracy.

F. Clock Jitter and Feedback Path Noise and Nonlinearity

It follows from the analysis in Section III-D that the multiplication of the decimation filter output, $r[n]$, by $s_k[n + P - Q - m]$ in Fig. 5 causes $\bar{u}_{k,m}[n]$ to be the signal of interest and $u_{k,m}[n] - \bar{u}_{k,m}[n]$ to be noise from the perspective of estimating $a_{k,m}[n]$. It can be verified by subtracting (19) from (16) that the signal to noise ratio associated with each $a_{k,m}[n]$ estimation is low even in the absence of any noise from the ADC. This is because $r[n] = r_{ideal}[n] + r_e[n] + r_c[n]$, where $r_{ideal}[n]$ and all but small portions of $r_e[n]$ and $r_c[n]$ contribute only noise terms to $u_{k,m}[n] - \bar{u}_{k,m}[n]$ given that they are uncorrelated with $s_k[n + P - Q - m]$. For example, error introduced anywhere in the system by clock jitter is generally uncorrelated with $s_k[n + P - Q - m]$, so it is simply another noise term in $u_{k,m}[n] - \bar{u}_{k,m}[n]$, and it only needs to be on the order of 6 dB lower than the variance of the other terms in $u_{k,m}[n] - \bar{u}_{k,m}[n]$ to have a negligible effect on the error variance of $a_{k,m}[n]$.

The same is true of ADC noise provided it is uncorrelated with $s_k[n + P - Q - m]$. Consequently, an ADC with a low SNR can be tolerated as demonstrated in the next section. In the design example a VCO-based ADC is used because the noise it introduces is essentially uncorrelated with its input signal, which ensures that it is uncorrelated with $s_k[n + P - Q - m]$. Most other types of $\Delta\Sigma$ ADCs have this property too, so they could be used in place of the VCO-based ADC, although in most such cases a high-impedance input buffer would be necessary to prevent the ADC's input network from disturbing the main DAC's output waveform.

It is also demonstrated in the next section that an ADC with relatively high nonlinearity can be tolerated by the MNC technique. The reasons for this nonlinearity tolerance are explained in the remainder of this section.

As described in Section III, the additive terms in the ADC's input signal which are proportional to $s_k[n]$ for $k = 1, 2, \ldots, 35$ are the terms that the MNC technique measures. In this sense they can be viewed as the *desired terms* from the perspective of the MNC technique's measurement process. Each desired term consists of two additive parts: one that comes from $e_{DAC}[n]$ so it has the form $s_k[n]d_k(t)$, and the other that comes from the correction DAC. The first part is very small relative to the ADC's input range because $d_k(t)$ arises from component mismatches. The second part is similarly small by design because it is intended to cancel the first part over the first Nyquist band.

It follows that nonlinear distortion from the ADC causes the decimation filter output to contain numerous additive terms that are each proportional to the products of multiple values of $(s_i[j])^p$ for different integer values of i, j, and p. From the perspective of estimating $a_{k,m}[n]$, most of these terms contribute noise to $u_{k,m}[n] - \bar{u}_{k,m}[n]$ because they get multiplied by $s_k[n + P - Q - m]$. Only the terms from nonlinear distortion that are proportional to $(s_k[n + P - Q - m])^p$ where p is 1, 3, 5, 7, …, and not also proportional to $s_i[j]$ for any $i \neq k$ or $j \neq n + P - Q - m$ contribute an error bias to the estimate of $a_{k,m}[n]$. Not only are there relatively few such terms, but the terms are much smaller than the corresponding desired terms even when the ADC is fairly nonlinear. Each such error term is proportional to one of the ADC's second-or-higher-order Taylor coefficients, which is much less than unity, as well as one of the desired terms raised to the pth power. For $p = 3, 5, 7, \ldots$, the terms are particularly small because the desired terms are small to begin with.

Furthermore, the estimate of $e_{DAC}[n]$ need not be highly accurate to significantly improve the system's overall SNR. For example, suppose that $e_{DAC}[n]$ degrades the main DEM DAC's peak SNR in the absence of the MNC technique by more than 6 dB. Then, even if the MNC technique were applied for a case where the error terms described above are so severe that they cause the estimate of $e_{DAC}[n]$ to deviate from the actual $e_{DAC}[n]$ by 50%, the MNC technique would still improve the overall SNR by as much as 6 dB.

IV. Simulation Results

The system shown in Fig. 4 and described above was simulated in the Cadence Virtuoso environment with the STMicroelectronics FDSOI 28 nm CMOS process design kit. Relevant additional design details and two sets of simulation results are presented in this Section. The first set of simulation results demonstrates the performance of the MNC technique after convergence. The second set demonstrates the convergence behavior of the MNC technique.

Both the main and correction DACs incorporate RZ 1-bit DACs similar to the type described in [20] with an RZ duration of 25% of the clock period. All operate from a 1.8 V supply

and their combined differential outputs are loaded with a 15 Ω resistor and 14 pF capacitor to ground on each side. The main DAC has a differential minimum step-size of $\Delta = 2.44\ \mu$A. It has 36 1-bit DACs, 16 of which have a weight of 1024, and 20 of which have respective weights of 1, 1, 2, 2, 4, 4, 8, 8, …, 512, 512. The correction DAC has a differential minimum step-size of $\Delta_c = \Delta/4 = 0.61\ \mu$A. It has 14 1-bit DACs, 7 of which have a weight of 64, 3 of which have a weight of 16, and 4 of which have respective weights of 1, 2, 4, 8.

The static mismatch of each of the smallest 1-bit DACs in the main DAC was chosen as a Gaussian random variable with a standard deviation of 3.2% of the 1-bit DAC's step-size, Δ. That of each larger 1-bit DAC in the main DAC was chosen the same way except with a standard deviation of 3.2% divided by the square root of the 1-bit DAC's weight, e.g., the standard deviation of the largest 1-bit DACs is 0.1% of their 1024 Δ step-size. The static mismatches in the correction DAC were chosen in the same fashion except starting from minimum-size 1-bit DACs with a standard deviation of 6.4% of their step-size, Δ_c.

The dynamic mismatches of the 1-bit DACs were implemented in two ways. A random Gaussian time skew with a standard deviation of 1.8 ps was applied to each 1 bit DAC switch driver. Additionally, for the 1-bit DAC of lower weights, the sizes of their current steering switches were not scaled in proportion due to minimal width limitation of technology, which introduces systematic dynamic mismatches.

The VCO-based ADC is similar to that presented in [17] except without the digital calibration circuitry. As in [17], each VCO consists of an open-loop voltage-to-current (V/I) converter followed by a current-controlled ring oscillator (ICRO). The V/I converter is a source degenerated differential pair, and the ICRO is a pseudo-differential ring of current-starved inverters. Accordingly, the VCO, and, thus, the VCO-based ADC, are highly nonlinear. For example, simulations indicate that for a full-scale sinusoidal input signal the ADC's 2nd, 3rd, and 4th harmonics are −26 dBc, −47 dBc, and −64 dBc, respectively. As demonstrated below, and for the reasons described in Section III-F, this nonlinearity does not limit the simulated system's performance.

The decimation filter is implemented as a 33-tap polyphase FIR filter for low hardware complexity [21]. As described in Section III, $h_c[n]$ is defined as the impulse response from the input of the correction DAC to the output of the decimation filter. The values of $h_c[n]$ were extracted from circuit simulation of the correction DAC, ADC, and decimation filter operating together, and the gain of the decimation filter was normalized such that $h_c[Q] = 1$. The extracted values were found to depend only weakly on the behavior of the correction DAC and ADC so they do not change significantly over process and temperature variations. Substituting the extracted values of $h_c[n]$ into (23), (29), and (30) results in $g = 0.0018$ and $r = 0.25$, which easily satisfy the hypotheses of the theorems in Section III-D.

In the first set of simulations (shown in Figures 7, 8, and 9) all the 1-bit DAC current sources and switches and the ADC's V/I converters were simulated at the transistor level. The remaining analog circuitry, e.g., the 1-bit DAC switch drivers

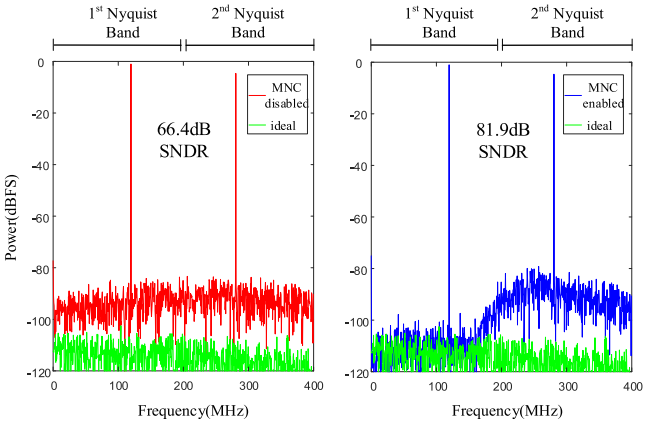

Fig. 7. Representative simulated output Spectra without/with MNC for a −1 dB full scale signal. The SNDR bandwidth is 0 to $0.42 f_s$.

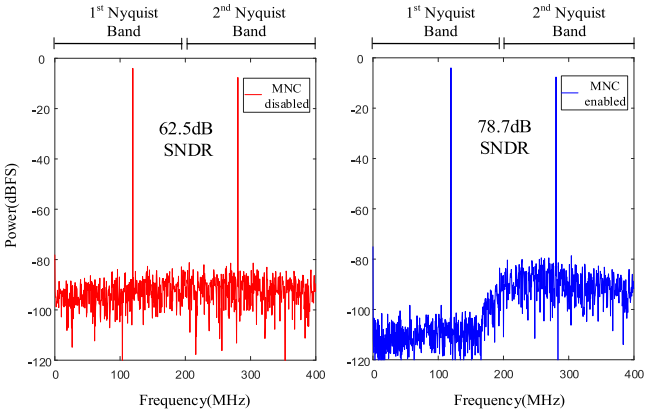

Fig. 8. Representative simulated output Spectra without/with MNC with −4dBFS input tone.

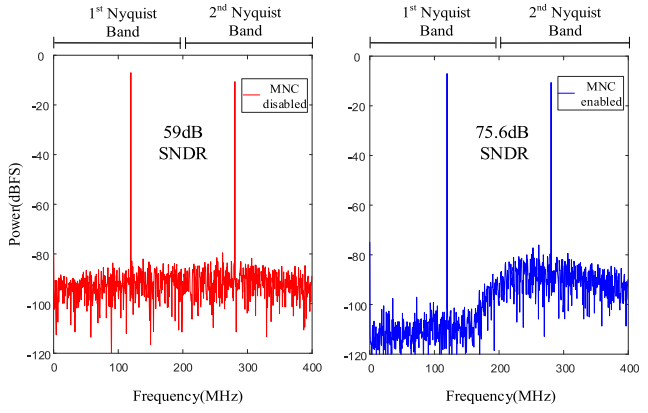

Fig. 9. Representative simulated output Spectra without/with MNC with −7dBFS input tone.

and the ADC's ICROs, as well as all the digital logic was simulated at the behavioral level using Verilog-AMS to reduce simulation time. The transistor-level portions of the simulations enhance realism, but significantly increase simulation time, so the simulations were run with the MNC technique implemented in foreground mode to minimize convergence time and, therefore, simulation time.

The DEM DAC was driven by a digital sequence that toggles back and fourth between -2389.5Δ and -2388.5Δ at the clock rate. This input sequence was chosen because it

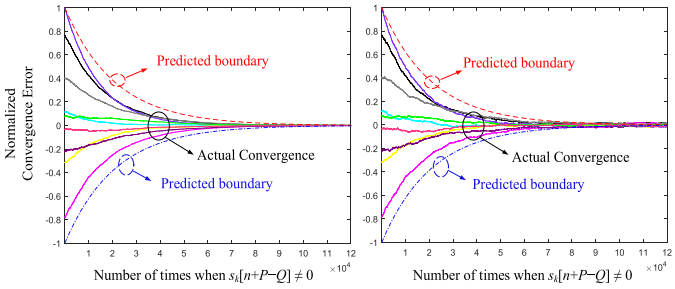

Fig. 10. Simulated coefficient convergence without ADC noise (left plot) and with ADC noise (right plot).

is both simple and ensures that each $s_k[n]$ sequence is non-zero at least 30% of the time. Two minor enhancements were applied to reduce convergence time. The first enhancement is the use of a few extra 1-bit DACs to cancel most of the signal component of the main DACs output prior to the ADC. This allowed the loop gain, K, to be increased without a significant noise penalty. The extra 1-bit DACs were simulated at the transistor-level with mismatches chosen as described above. The second enhancement is to use a $4\times$ larger value of K for the first 100 μs of convergence time than used for the remaining convergence time. With these enhancements the total convergence time was 250 μs, which corresponds to approximately three weeks of simulation time.

Representative simulated output spectra are shown in Fig. 7 for a -1 dB full-scale sinusoidal input without and with the MNC technique enabled. In each case the 14-bit input signal was generated by adding a dither sequence that is white and uniformly distributed between $-\Delta/2$ and $\Delta/2$ to a floating point sinusoidal signal and quantizing the result to 14 bits. Output spectra of the main DAC for the ideal case of no unit element mismatches are also shown in Fig. 7 to provide a comparison baseline. The decimation filter's relatively short length resulted in aliasing that limits MNC performance in the top 16% of the first Nyquist band.[4] This was considered a reasonable design tradeoff, so the signal band is taken to range from zero to 0.42 $f_s = 168$ MHz.

The simulation results indicate that the MNC technique increased the signal-to-noise-and-distortion ratio (SNDR) from 66.4 dB (10.8 bits) to 81.9 dB (13.4 bits). Separate simulations suggest that the static mismatch error and dynamic mismatch error for this case contribute roughly equal SNR degradation over the first Nyquist band.

Additional simulated output spectra are shown in Figures 8 and 9 for different input signal amplitudes without and with the MNC technique enabled. In each case the results show the expected SNDR improvement when the MNC technique is enabled. Other simulations that have been run by the authors for many different input signals and random number seeds yield comparable results.

The second set of simulations model the system with the same parameters and non-ideal behavior described above except that K was set to its final value from the start, and all components were simulated at the behavioral level to avoid excessive simulation time. The left plot in Fig. 10 shows the convergence of the elements of $[a_{k,0}[n], a_{k,1}[n+1], \ldots, a_{k,N-1}[n+N-1]]^{\mathrm{T}} - \mathbf{a}'_k$, for a representative value of k and the artificial case of no ADC quantization noise. It also shows the upper and lower bounds of the means of these trajectories predicted by Theorem 1, i.e., $\pm||\mathbf{z}_k[n]||$. As expected, all coefficients converge to their ideal values within the bounds predicted by Theorem 1. The right plot in Fig. 10 shows the corresponding results with ADC quantization noise included. The results suggest that the means of the trajectories are still within the predicted bounds even though the noise causes the instantaneous values to exceed the bounds from time to time. These results as well as those from all of many other such simulations run by the authors are in agreement with the theoretical results of Section III-D.

[4]This percentage can be arbitrarily reduced at the costs of greater hardware complexity and power consumption by increasing the decimation filter length.

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