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A Reconfigurable Mostly-Digital ΔΣ ADC with a Worst-Case FOM of 160dB

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INTEGRATED SIGNAL PROCESSING GROUP

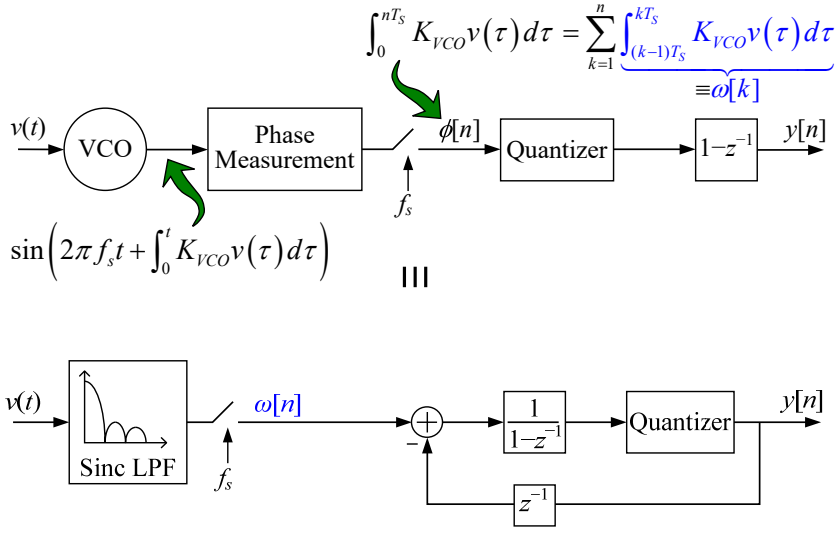
Outline

- Motivation
- Review of VCO-based delta-sigma ADCs
- Overview and limitations of our 1st generation IC presented in **[Taylor, Galton, *ISSCC*, Feb. 2010]**
- Enhancements leading to 2nd generation IC (this work)
- Measured results and comparison table
- Conclusions

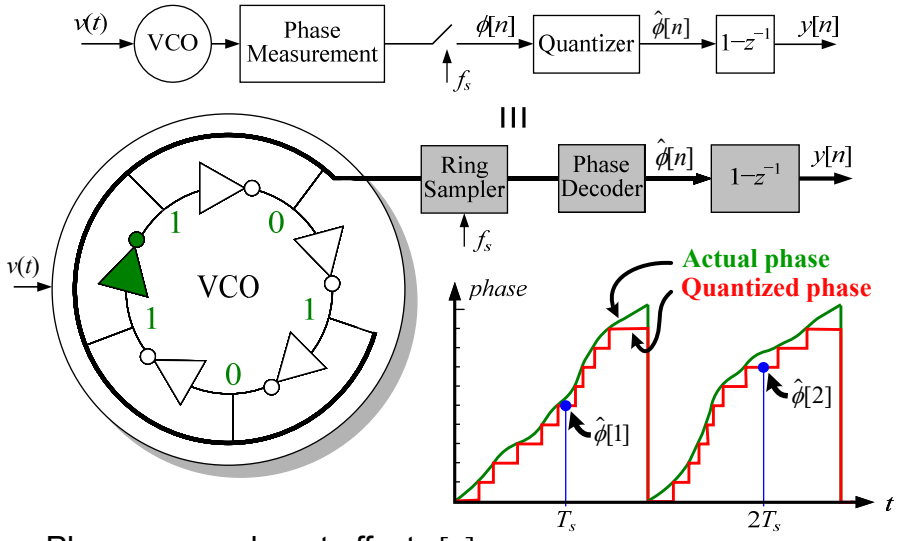
Motivation

- Conventional continuous-time ΔΣ ADCs require:
  - Low-leakage analog integrators
  - High-linearity feedback DACs
  - Low-noise reference voltages
  - High-speed comparators
  - Low-jitter clocks
- So they are increasingly difficult to design as CMOS technology scales and supply voltages reduce
- But highly-scaled CMOS technology offers very fast, dense, and low-power digital circuitry
- This work is a 2nd generation reconfigurable ΔΣ ADC that avoids the above analog blocks in favor of digital circuitry

Review: VCO-Based ΔΣ Modulator Idea

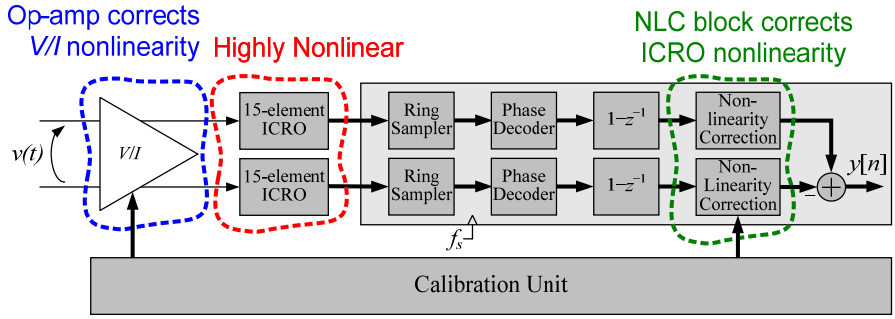


Review: VCO Phase Measurement



Phase wraps do not affect $y[n]$

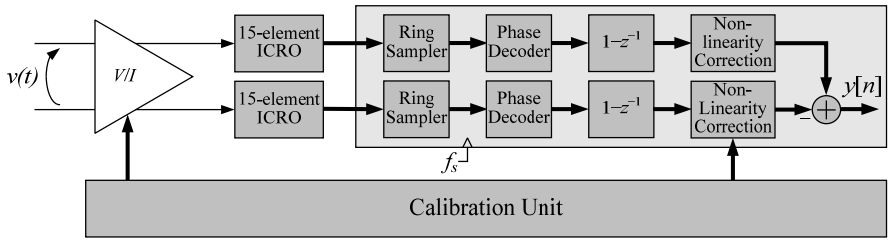
Review: 1st Generation IC Simplified Block Diagram



- Pseudo-differential to suppress common-mode noise and remove residual even-order distortion
- Calibration Unit generates NLC values in background

  $\Rightarrow$ Enables reconfigurability

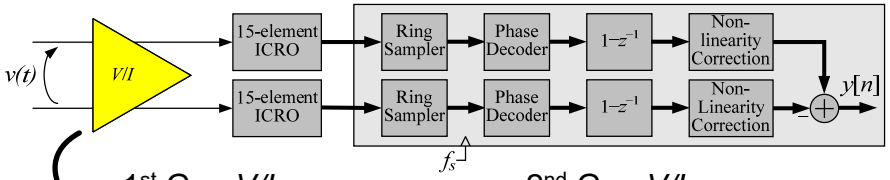
Limitations of 1st Generation ADC



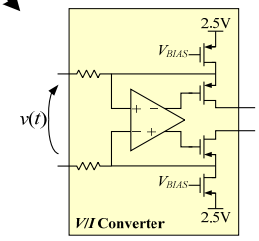
- No digital calibration of *V/I* so need op-amp
  ⇒Op-amp needs 2.5V supply for high performance
- 65nm CMOS inverter delay ⇒ coarse quantization
- Memory in Ring Sampler ⇒ distortion
- Phase wraps limit no-overload range

The 2nd generation IC addresses these limitations as follows…

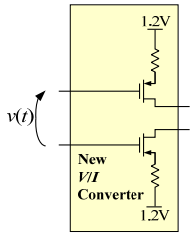
1st Gen Versus 2nd Gen *V/I* Converter



1st Gen *V/I*:



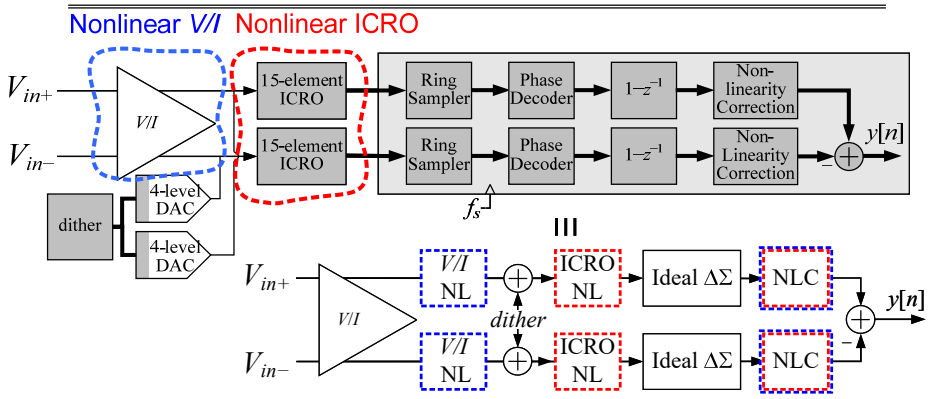
2nd Gen *V/I*:



- V/I linearized with op-amp feedback
- Highly nonlinear but *V/I* is now linearized with NLC

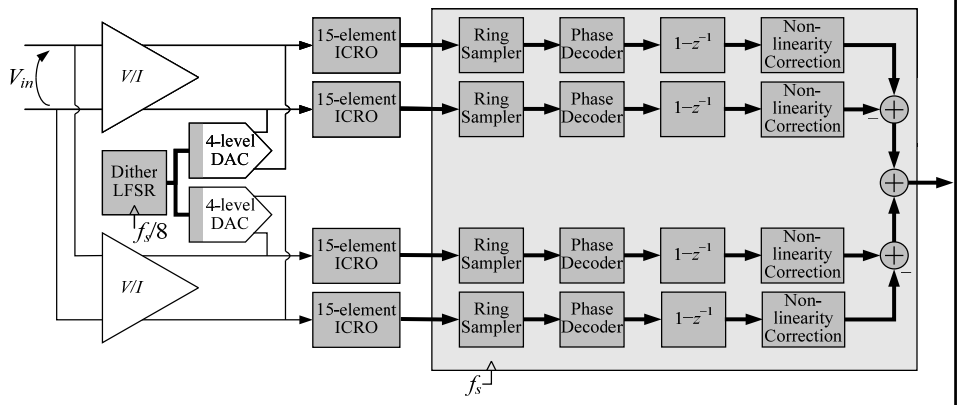
But linearizing V/I and ICRO with one NLC is tricky…

Dither Problem with Nonlinear V/I Converter



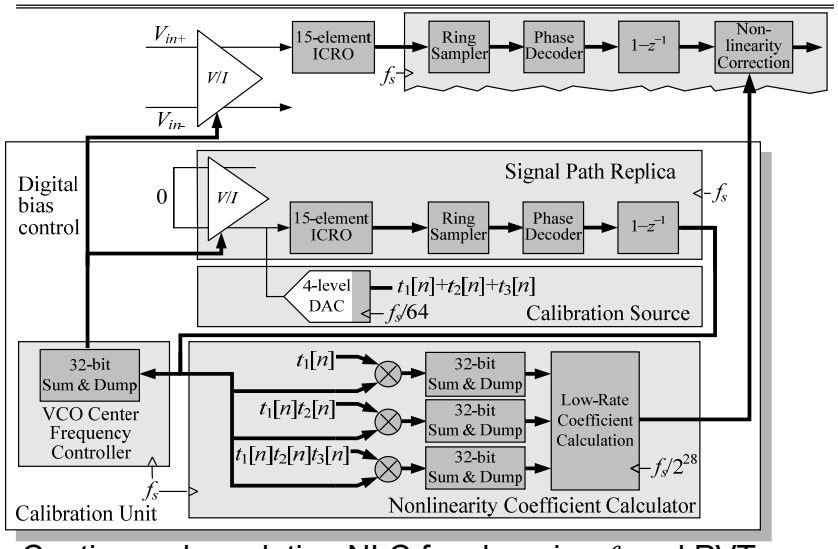
- First-order ΔΣ noise performance is poor without low-pass dither
- Common-mode dither signal works and self-cancels at the output
- Dither added after *V/I* to avoid adding in voltage domain
- But $\Rightarrow V_{in}$ & *dither* see different nonlinearities
- NLC block corrects V_{in} nonlinearity but not *dither* nonlinearity
  $\Rightarrow$ Unwanted V_{in} & *dither* intermodulation products

Solution to Dither Nonlinearity Problem



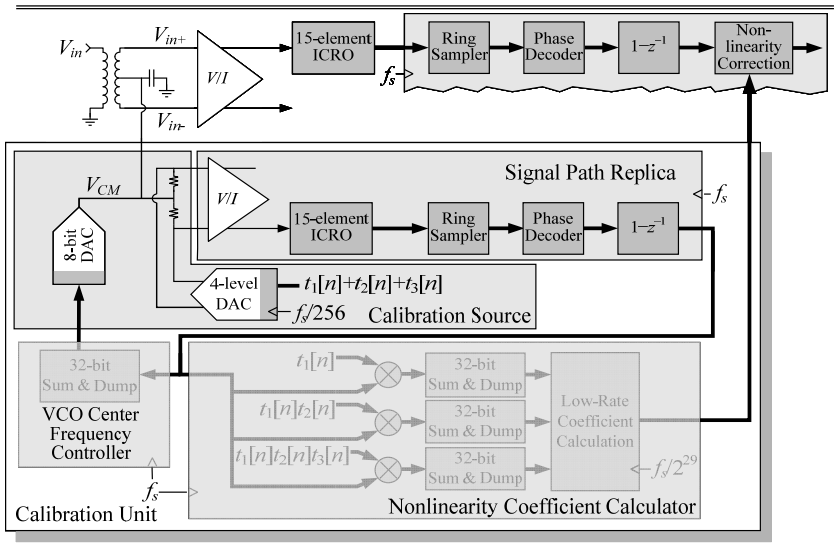
- Differential dither self-cancels
- Even-order intermodulation products cancel
- Odd-order intermodulation terms are not significant
- 1st generation ADC also has 2 paths but there used to increase SQNR

1st Generation Calibration Unit



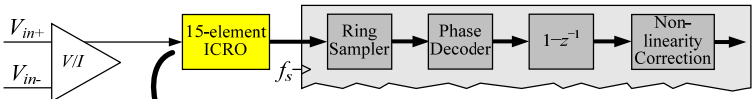
- Continuously updating NLC for changing f_s and PVT
- $t_1[n]$, $t_2[n]$, $t_3[n]$ are ± 1 pseudo-random sequences
  [Panigada, Galton, *ISSCC*, Feb. 2009]

2nd Generation Calibration Unit

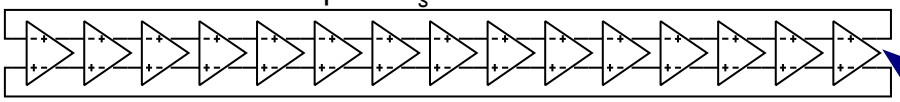


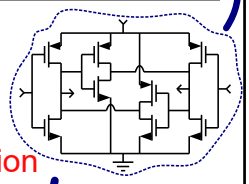
- Calibration unit measures nonlinearity of replica V/I and ICRO
- VCO Center Frequency Controller sets output common-mode of the circuit driving the signal converter

Min Inverter Delay Limited 1st Gen ADC

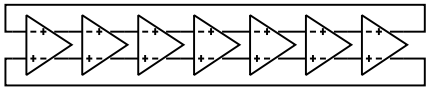


Previous ICRO: τ = 30ps so f_s = 1.15GHz:



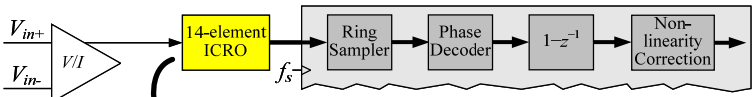


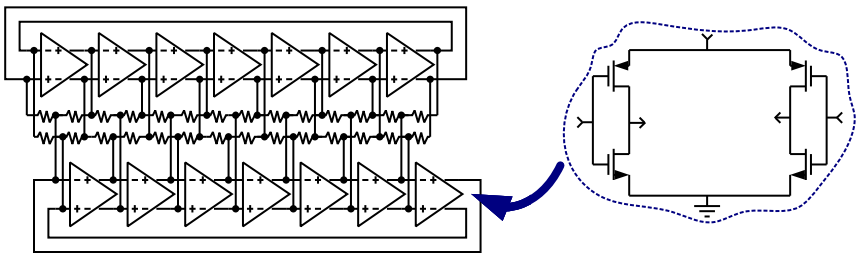
- Quantization step size is set by the minimum inverter delay, τ
- Going from 15 to 7 elements would have doubled f_s but halved the number of quantization levels:



- **The Point**: The peak signal to quantization noise ratio (SQNR) is set by τ in the 1st generation design

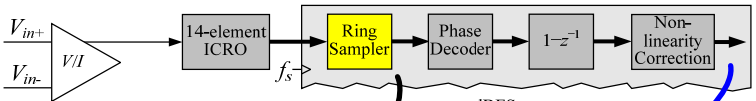
Quadrature Coupled ICROs Reduce This Limitation



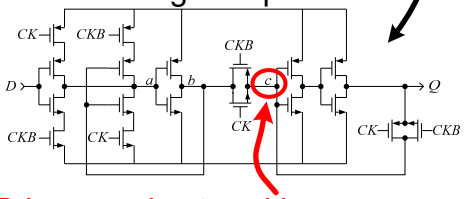


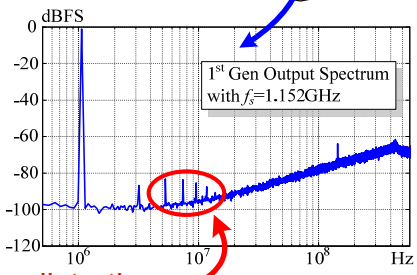
- **Idea**: Injection lock two ring oscillators with an offset of $\tau/2$ to reduce the quantization noise by 6dB
- Resistors keep pseudo-differential inverters 180-degrees out-of-phase, and keep the two rings phase locked with $\tau/2$ offset
- With 7-element ring oscillators and τ = 30ps have f_s=2.4GHz
  $\Rightarrow$ 9dB increase in SQNR relative to 1st generation design

Hysteresis Problem in 1st Gen Ring Sampler



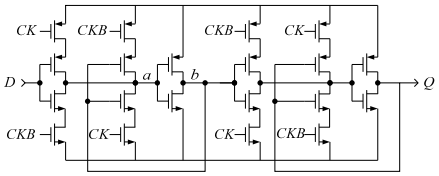
Previous Ring Sampler DFF:



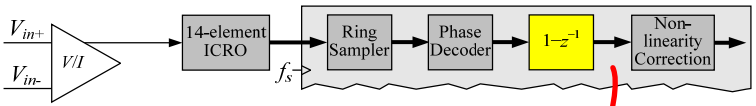


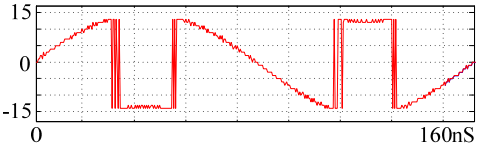
Prior sample stored here
⇒signal dependent hysteresis ⇒distortion

New design avoids problem with non-transmission-gate DFF:



No-Overload Range Limitation in 1st Gen ADC





- Phase wraps when f_{vco} is outside $0.5f_s < f_{vco} < 1.5f_s$

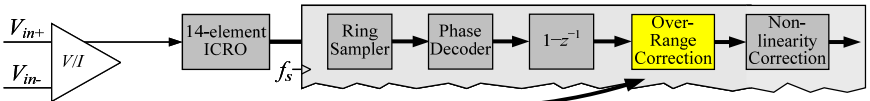
  ⇒ In previous design ADC overloads when $|V_{in}| > \pi f_s/K_{vco}$

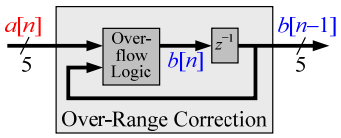
- But, high OSR implies $f_{in} << f_s$

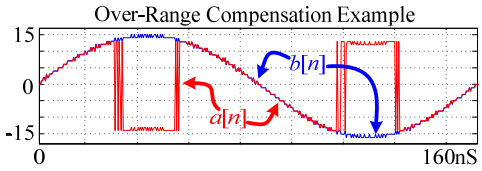
  ⇒ Use previous sample to determine if f_{vco} is outside of $0.5f_s$ to $1.5f_s$ range

  ⇒ Extend $|V_{in}|$ range beyond $\pi f_s/K_{vco}$

Over-Range Extension Technique

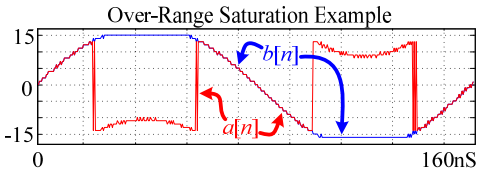






Overflow Logic:

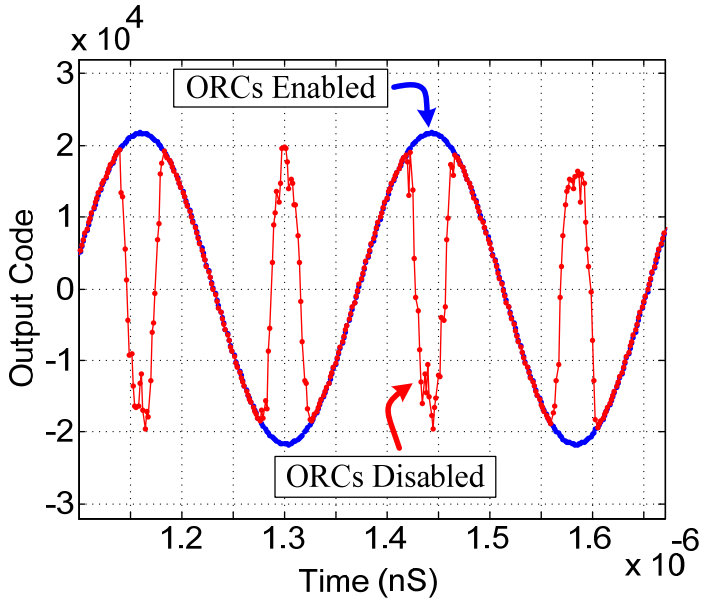
if $a[n] > 7$ and $b[n-1] < 0$
then $b[n] = \max\{-16, a[n]-32\}$
else if $a[n] < -8$ and $b[n-1] > 0$
then $b[n] = \min\{15, a[n]+32\}$
else $b[n] = a[n]$



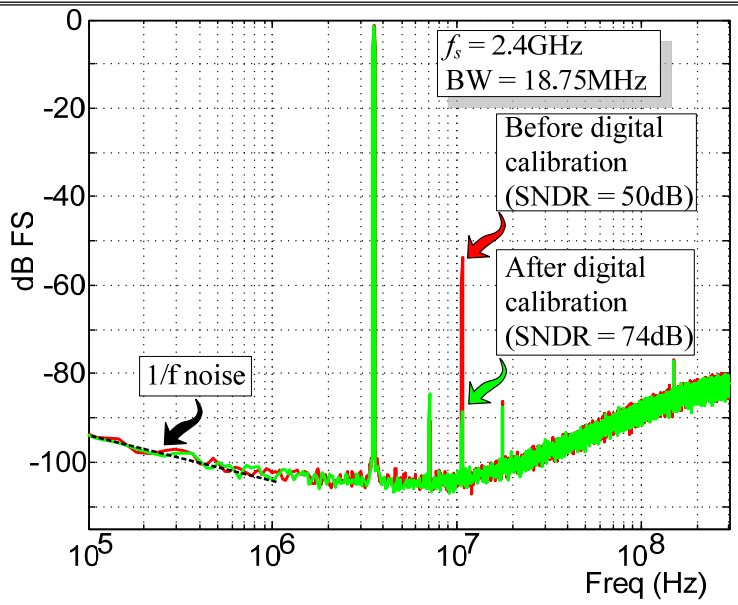
- Over-Range Correction (ORC) extends no-overload range
- ADC saturates like a flash converter

  ⇒ No ΔΣ modulator instability with large input signals

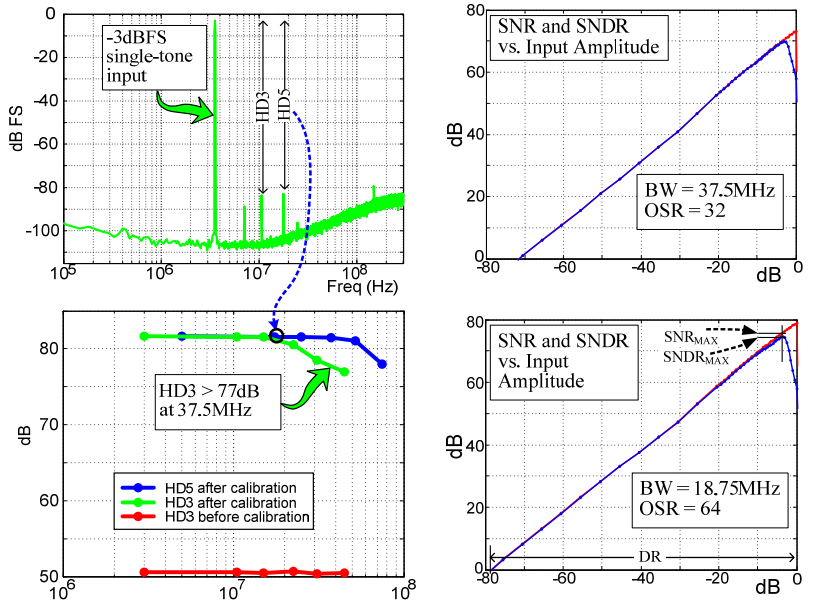
Measured Overload Output



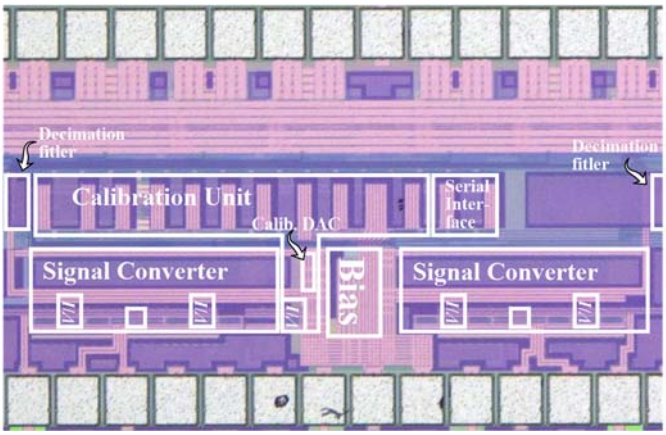
Example Measured Output Spectra



Measured PSD, HD, SNR, and SNDR



Die Photograph



- Signal converter area = 0.040mm^2
- Calibration unit area = 0.070mm^2
- I and Q ADCs share one calibration unit
  $\Rightarrow$ Area per converter = 0.075mm^2

IC Performance Comparison

	This Work						1st Gen		[2]	[3]	[4]	[5]	[6]	[7]
Area (mm^2)	0.075						0.07		0.7	1.5	0.45	0.9	0.15	0.4
Process	65nm G+						65nm LP		180nm	130nm	130nm	45nm	90nm	90nm
f_s (MHz)	1300			2400			500	1152	640	640	900	4000	500	640
OSR	128	64	32	64	48	32	64	32	32	16	22.5	16	10	32
BW (MHz)	5.1	10.2	20.3	18.75	25	37.5	3.9	18	10	20	20	125	25	10
f_{in} (MHz)	1*	1*	3.5*	3.5*	4.9*	7.49*	1*	2.3*	2.4	3.68	2	41	2	2
SNR (dB)	76	74	70	76	74	71	71.5	70	84	76	81.2	65.5	64	
SNDR (dB)	75	73	69	74	73	70	71	67.3	82	74	78.1	65	63.5	65
SFDR (dB)	82	82	82	81	81	77							81	72
Power Supply (V)	0.9			1.2			2.5/1.2	2.5/1.2	1.8	1.2	1.2	1.1/1.8	1.2	1.2
Power Total (mW)	11.5			39			8	17	100	20	87	256	8	6.8
Power Analog (mW)	3			7			2.5	5						
Power Digital (mW)	8.5			32			5.5	12						
FOM (dB) **	161	162	161	161	161	160	158	158	162	164	162	152	158	157
FOM2 (fJ/conv) ***	246	155	123	254	214	201	354	249	486	122	331	705	131	234

*** Worst-case input frequency value over stated BW**
**** FOM (SNDR) = SNDR + 10 log$_{10}$(BW/Power)**
***** FOM2 = Power / (2BW*2^ENOB)**

- Power FOM equivalent to state-of-the art
- Much smaller die size
- Single, low-voltage power supply
- Very large max signal bandwidth

Conclusion

- Have presented an enhanced high-performance stand-alone VCO-based $\Delta\Sigma$ ADC with:
  - Increased maximum signal BW
  - Improved FOM ≥160dB over entire range
  - An op-amp free signal path
  - Saturation characteristics like a flash converter
- Unlike conventional ADCs it does not require:
  - Analog integrators
  - Feedback DACs
  - Reference voltages
  - Comparators
  - A low-jitter clock
- Its performance is limited mainly by the speed of digital circuitry, so unlike conventional ADCs its performance improves as CMOS technology scales