A Highly-Digital Frequency Synthesizer Using Ring Oscillator Frequency-to-Digital Conversion and Noise Cancellation

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Outline

- Fractional-$N$ PLL background information
- Build-up of the proposed PLL architecture
- Circuit details
- Measured results
Conventional Analog Fractional-N PLL

- $f_{PLL} = (N+\alpha)f_{ref}$ where $N$ is integer and $-\frac{1}{2} \leq \alpha \leq \frac{1}{2}$
- Charge in $n^{th}$ ref period's CP pulse = $-\theta_{PLL}[n] + e_q[n]$
- $\theta_{PLL}[n] = \text{sampled phase error}$
- $e_q[n] = \text{integrated 2nd-order } \Delta\Sigma \text{ quant noise}$

- Lowest noise and spurs to date
- Analog LPF is big & CP is sensitive to nonlinearity/leakage
- $\Rightarrow$ Not compatible with highly-scaled CMOS technology

“Digital” Fractional-N PLLs Avoid These Problems

- $p[n] \approx -\theta_{PLL}[n] + e_q[n]$ (reference-rate digital sequence)
- In prior digital PLLs:
  - $e_q[n] = \text{coarse uniform or 1st-order } \Delta\Sigma \text{ quantization error so it usually contains large spurs}$
  - Dither sometimes used to reduce spurs but increases noise
- This work is a new digital PLL in which:
  - $e_q[n] = \text{integrated 2nd-order } \Delta\Sigma \text{ quantization error just like in an analog PLL}$
  - 2nd-order $\Delta\Sigma$ self-dithering property $\Rightarrow$ low spurs & noise
2nd-Order FDC-Based Phase Error to Dig. Converter

\[
\Delta \Sigma \text{ FDC:} \quad y[n] + \alpha = -\theta_{PLL}[n] + \theta_{PLL}[n-1] + (2^{\text{nd}}\text{-order } \Delta \Sigma \text{ quantization error})
\]

\[
p[n] = -\theta_{PLL}[n] + e_q[n] - e_q[n-1]
\]

\[
\therefore \text{2}^{\text{nd}}\text{-ord } \Delta \Sigma \Rightarrow p[n] \text{ has 1}^{\text{st}}\text{-order shaped noise but low spurs}
\]
DMRO and Ring Phase Calculator Behavior

Counter Output

\[ y[n] + 60 \]

\[ y[n-1] + 60(n-1) \]

\[ n^{th} \text{ Reference Period} \]

\[ \therefore \text{Counter output} = \text{quantized integral of DMRO frequency} \]

ΔΣ FDC Behavior When PLL is Locked

Negative feedback within ΔΣ FDC through divider:

- Larger \( y[n] \)
  - \( \Rightarrow \) larger \( v[n] \)
    - \( \Rightarrow \) earlier \( v_{\text{div}} \) edge
      - \( \Rightarrow \) shorter \( u \) pulse
        - \( \Rightarrow \) less DMRO phase change
          - \( \Rightarrow \) smaller \( y[n+1] \)

- Causes \( f_{\text{DMRO}} \) to be \( 60f_{\text{ref}} \) on average and keeps \( |y[n]| \leq 2 \)
What Causes the $\Delta\Sigma$ Modulator Behavior?

\[ v[n] = \frac{v[\text{PLL}[n-1]]}{1-z^{-1}} + 2z^{-1} \]

Behavior of the $\Delta\Sigma$ FDC:

\[ v[n] = \frac{v[\text{PLL}[n-1]]}{1-z^{-1}} + \frac{1}{1-z^{-1}} \]

Recall:

Practical implementation:

But How to Avoid an $\infty$-Range Counter?

Recall:

Practical implementation:
How to Make Use of All The DMRO Outputs?

- DMRO has 13 outputs
- Counter is clocked by just 1 DMRO output
- Counter quantizes DMRO phase ramp by counting integer cycles ⇒ very coarse quantization
- Can use all DMRO outputs to measure fractional quantization error in steps of 1/26 of a cycle

More Ring Phase Calculator Details

Ring Phase Calculator:
- Standard cell logic
- Samples DMRO phase on falling edges of $v_{\text{ref}}$
- Asynchronous sampling issue/solution described shortly
- $y[n]$ is integer-valued, $-\hat{e}_q[n]$ is fractional
- When PLL is locked, clipper has no effect
- Otherwise, clipper avoids roll-overs to reduce locking time
Behavior of the ΔΣ FDC:

\[-\alpha \theta_{PLL}[n] + \theta_{PLL}[n-1]\]

- Quantization noise cancellation (QNC) uses \(-\hat{e}_q[n]\) to cancel coarse quantization noise prior to loop filter
- QNC allows wider loop filter bandwidth without noise penalty

DMRO Details

- \(f_{high} - f_{low} \approx f_{PLL}\) set with 5% resolution via ring supply resistances
- SPI selectable ranges: 0.4\(f_{low}\) < 3.4 and 1.8\(f_{high}\) < 5.1 GHz
RPC Asynchronous Sampling Issue

- Only one DMRO output bit changes at a time
  - Bit transitions occur at 1/26 quantization boundaries
  - $-\hat{e}_q[n]$ errors from sampling during bit transitions $\ll 1/26$
  - Asynchronous sampling of DMRO phases not a problem
- Multiple counter bits can change at once (e.g., 127 to 128)
  - $c[n]$ errors from sampling during bit transitions can be huge
  - Asynchronous sampling of counter output is a problem

RPC Asynchronous Sampling Solution

- $s_0, \ldots, s_{12} = $ DMRO outputs sampled on falling reference edge (phase decoder input bits)
- $s_0$ and $s_6$ indicate in which of 3 regions the edge occurred
- Retiming logic samples counter exactly 1.5 DMRO periods after the DMRO period in which the edge occurred
Digitally Controlled Oscillator

- Integer Boundary Avoider
- 2nd-Ord ΔΣ Modulator
- DEM
- SPI Coarse Ctrl
- PLL/8-rate FCEs
- SPI-controlled DCO tuning range: 2.8-3.7 GHz

Additional Design Information

DCO
- Unit FCE frequency step: 25 kHz
- PLL feedback-controlled DCO tuning span: 1.8 MHz
- SPI-controlled DCO tuning range: 2.8-3.7 GHz

Divider
- 6 ÷2/3 pulse swallowing stages
- \( f_{PLL}/8 \)-rate clock is output of 3\(^{rd} \) ÷2/3 pulse swallowing stage

Digital
- All digital logic synthesized except divider and DMRO sampling circuitry
- Synthesized logic clocked by \( f_{PLL}/8 \)-rate clock
Measured Spurious Tone Performance at 3.5 GHz

Largest measured fractional spurious tone powers for several fractional frequency settings ranging from 800 Hz to 13 MHz

Measured PLL Output Spectrum

- Reference spur from DCO input and coupling < -81 dBc
- Asymmetry ⇒ reference spur from DCO input only < -88 dBc
### Performance Summary

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>65</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.0</td>
</tr>
<tr>
<td>Power Diss. (mW)</td>
<td>15.6</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.35</td>
</tr>
<tr>
<td>Ref Freq (MHz)</td>
<td>26</td>
</tr>
<tr>
<td>PLL Freq (GHz)</td>
<td>3.5</td>
</tr>
<tr>
<td>PLL BW (kHz)</td>
<td>140</td>
</tr>
<tr>
<td>In-Band PN (dBc/Hz)</td>
<td>-93</td>
</tr>
<tr>
<td>PN@1MHz (dBc/Hz)</td>
<td>-126</td>
</tr>
<tr>
<td>PN@3MHz (dBc/Hz)</td>
<td>-138</td>
</tr>
<tr>
<td>PN@20MHz (dBc/Hz)</td>
<td>-151</td>
</tr>
<tr>
<td>Reference Spur (dBc)</td>
<td>-81</td>
</tr>
<tr>
<td>In-Band Fract. Spur (dBc)</td>
<td>-60</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Diss. Breakdown</th>
<th>mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital</td>
<td>4.6</td>
</tr>
<tr>
<td>Reference Oscillator</td>
<td>0.3</td>
</tr>
<tr>
<td>DCO and Output Buffer</td>
<td>9.0</td>
</tr>
<tr>
<td>ΔΣ FDC</td>
<td>1.7</td>
</tr>
</tbody>
</table>

### Performance Comparison

<table>
<thead>
<tr>
<th>Citation</th>
<th>This Work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
<th>[6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>65</td>
<td>90</td>
<td>130</td>
<td>130</td>
<td>65</td>
<td>55</td>
<td>65</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.0</td>
<td>1.2</td>
<td>1.5</td>
<td>?</td>
<td>1.2</td>
<td>1.5</td>
<td>1.5/1.2</td>
</tr>
<tr>
<td>Power Diss. (mW)</td>
<td>15.6</td>
<td>?</td>
<td>39</td>
<td>&gt;40</td>
<td>8.7</td>
<td>41.6</td>
<td>45</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.35</td>
<td>?</td>
<td>0.95</td>
<td>0.86</td>
<td>0.44</td>
<td>0.7</td>
<td>0.6</td>
</tr>
<tr>
<td>Ref Freq (MHz)</td>
<td>26</td>
<td>26</td>
<td>50</td>
<td>26</td>
<td>26</td>
<td>26</td>
<td>78</td>
</tr>
<tr>
<td>PLL Freq (GHz)</td>
<td>3.5</td>
<td>3.6</td>
<td>3.7</td>
<td>3.6</td>
<td>3.5</td>
<td>1.8</td>
<td>4.0</td>
</tr>
<tr>
<td>PLL BW (kHz)</td>
<td>140</td>
<td>40</td>
<td>500</td>
<td>50</td>
<td>3400</td>
<td>800</td>
<td>1000</td>
</tr>
<tr>
<td>Norm In-Band PN (dBc/Hz)</td>
<td>-93</td>
<td>-81</td>
<td>-107</td>
<td>-79</td>
<td>-101</td>
<td>-102</td>
<td>-109</td>
</tr>
<tr>
<td>Norm PN@1MHz (dBc/Hz)</td>
<td>-126</td>
<td>-117</td>
<td>?</td>
<td>-126</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>Norm PN@3MHz (dBc/Hz)</td>
<td>-138</td>
<td>?</td>
<td>-136</td>
<td>-136</td>
<td>?</td>
<td>-122</td>
<td>?</td>
</tr>
<tr>
<td>Norm PN@20MHz (dBc/Hz)</td>
<td>-151</td>
<td>-152</td>
<td>-149</td>
<td>-152</td>
<td>-129</td>
<td>-154</td>
<td>-149</td>
</tr>
<tr>
<td>Reference Spur (dBc)</td>
<td>-81</td>
<td>-92</td>
<td>-65</td>
<td>-84</td>
<td>-61</td>
<td>?</td>
<td>-56</td>
</tr>
</tbody>
</table>

Phase noise normalized to 3.5 GHz
Conclusion

- Have presented a new type of digital PLL
- Its quantization noise is equivalent to that of an analog PLL with 2\textsuperscript{nd}-order ΔΣ modulation
- Consequently, it circumvents the spurious tone versus noise tradeoff of prior digital PLLs
- This is demonstrated by state-of-the-art measured results
  - Lower power dissipation than all prior digital PLLs with comparable noise performance
  - Lower spurious tones than all prior digital PLLs