Presented at the 2010 IEEE International Solid-State Circuits Conference

A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator

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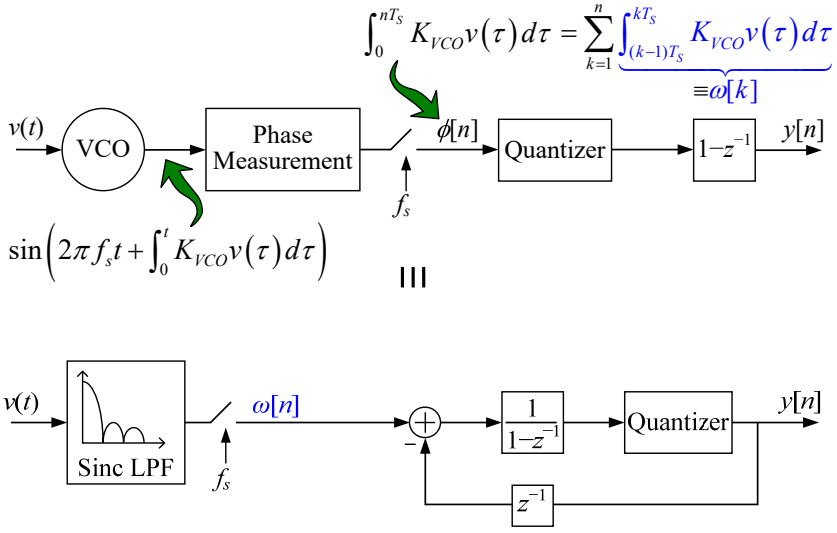
Motivation

- Conventional continuous-time ΔΣ ADCs require:
  - Low-leakage analog integrators
  - High-linearity feedback DACs
  - Low-noise reference voltages
  - High-speed comparators
  - Low-jitter clocks
- So they are increasingly difficult to design as CMOS technology scales and supply voltages reduce
- But highly-scaled CMOS technology offers very fast, dense, and low-power digital circuitry
- This work is a continuous-time ΔΣ ADC that avoids the above analog blocks in favor of digital circuitry

VCO-Based ΔΣ Modulator Idea



The VCO-Based ΔΣ Modulator Idea is Not New

Prior work:

[Straayer, Perrott, JSSC 2008]
[Kim, Cho, ISCAS 2006]
[Naiknaware, Tang, Fiez, TCASII 2000]
[Itawa,Sakimura, Nagata, Morie, TCASII 1999]
[Høvin, Olsen, Sverre, Toumazou, JSSC 1997]

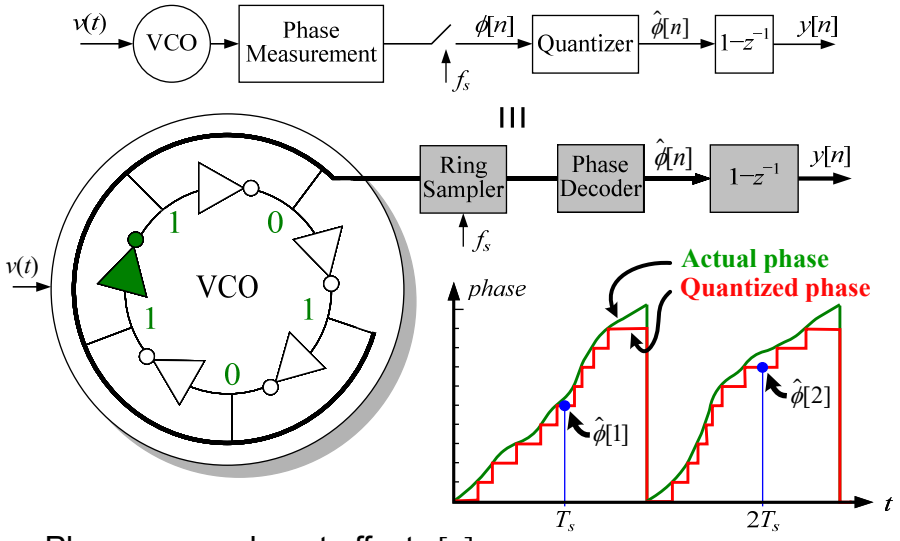
But VCO nonlinearity and ΔΣ idle tones limit approach
⇒ the only high-performance prior work requires a conventional continuous-time ΔΣ modulator first stage

This work:

Addresses above problems to enable the first high-performance stand-alone VCO-based ΔΣ ADC

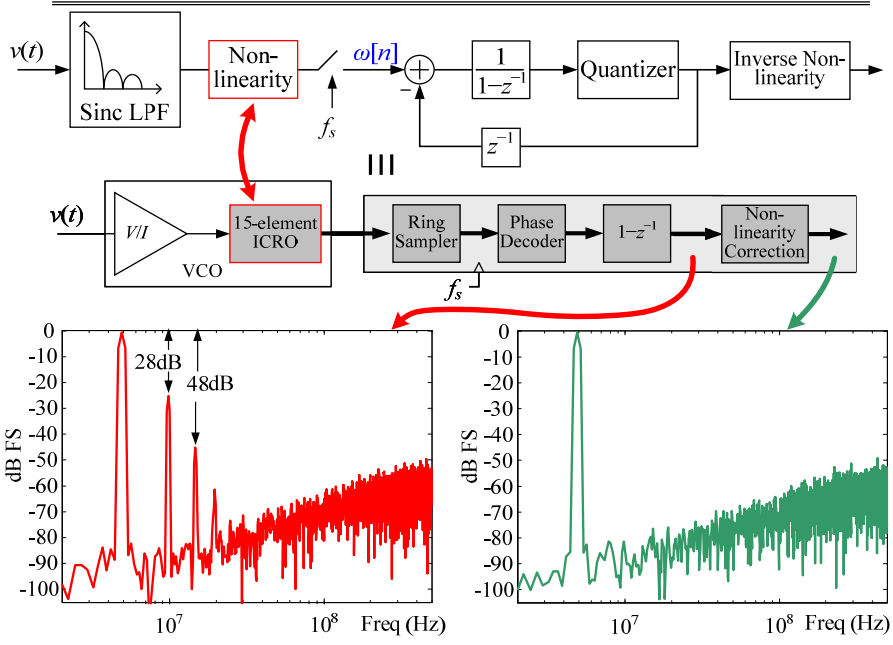
Target Specifications: f_s: 500-1152 MHz, BW: 3.9-18 MHz, SNDR: 67-78 dB, Power Dissipation: 8-17 mW

VCO Phase Measurement

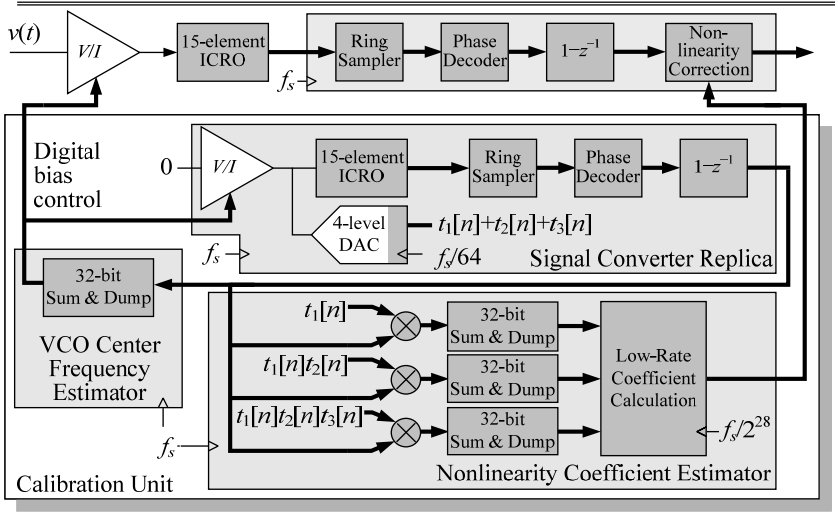


Phase wraps do not affect $y[n]$

VCO Nonlinearity

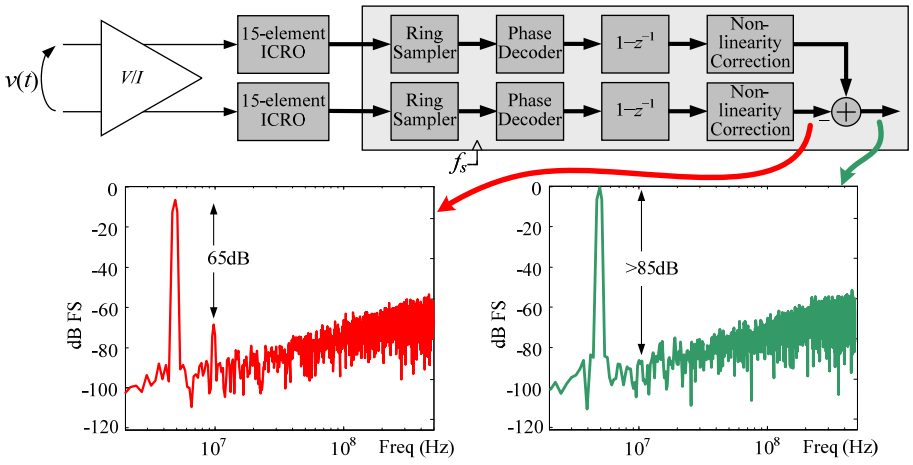


Calibration Unit



- $t_1[n]$, $t_2[n]$, $t_3[n]$ are ±1 pseudo-random sequences [Panigada, Galton, *ISSCC*, Feb. 2009]
- Replica allows fast convergence time – 233ms

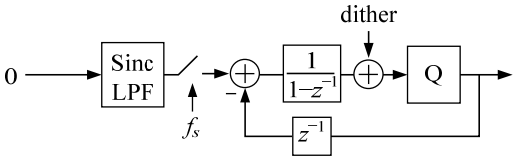
Pseudo-Differential Signal Converter

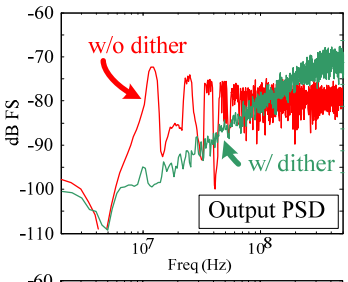


- Problem: Replica mismatch limits 2nd order correction
- Solution: pseudo-differential signal path
- Doubles area and power but fixes problem and increases SNR by 3dB (so figure of merit does not change)

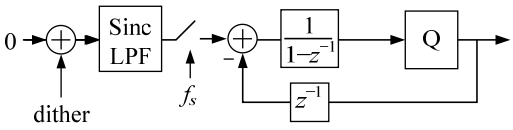
Idle Tone Problem

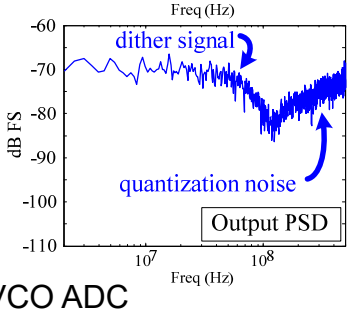
Dither method 1:





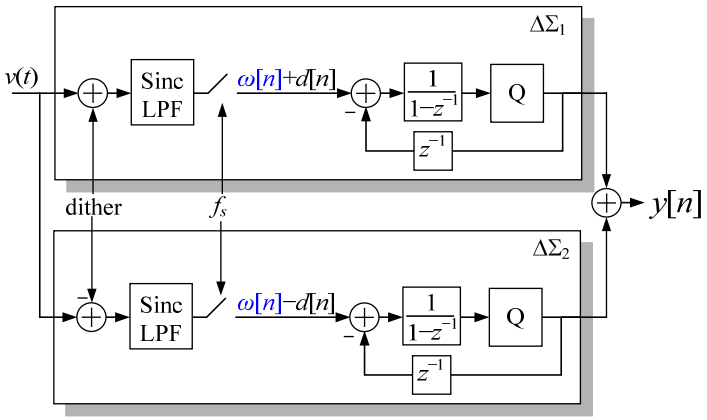
Dither method 2:





- Must use dither
- Dither method 1 not available for VCO ADC
- Dither method 2 works but corrupts signal band

Self-Cancelling Dither Solution



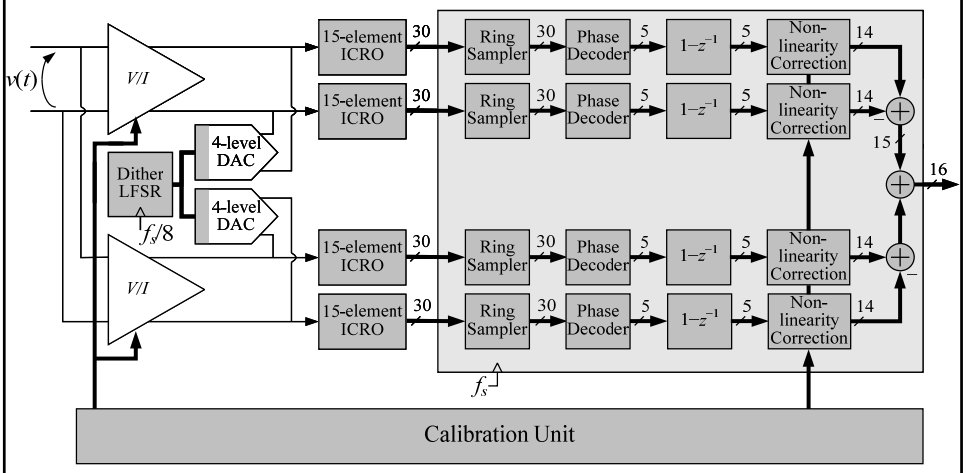
$$y[n] = 2\omega[n] + d[n]-d[n] + \Delta\Sigma_1 \text{ noise} + \Delta\Sigma_2 \text{ noise}$$

Signal +6dB

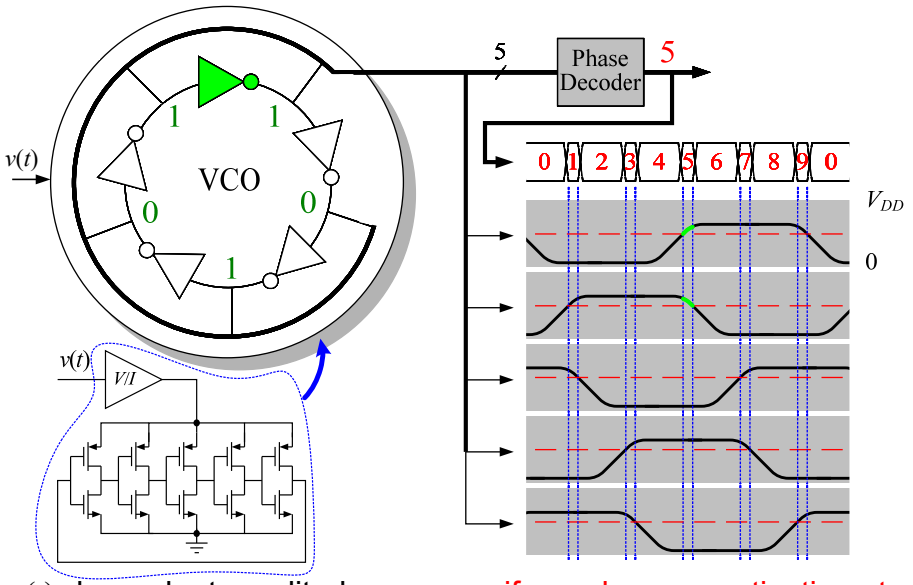
Dither cancels

$\Delta\Sigma$ noise +3dB

Full System Block Diagram

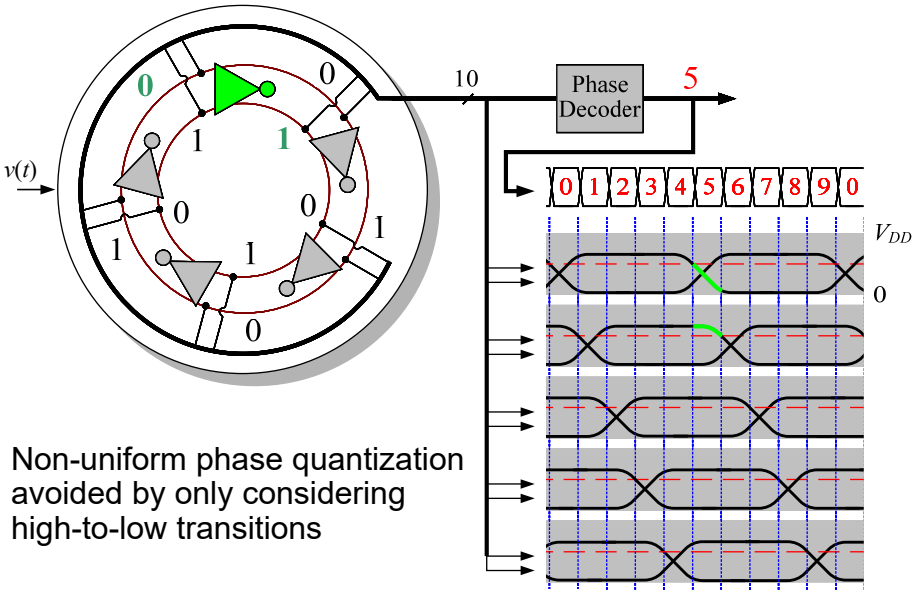


Non-Uniform Phase Quantization Problem



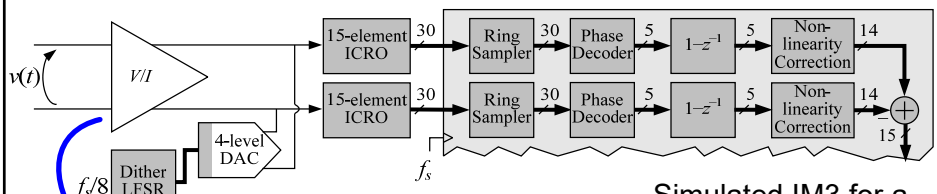
$v(t)$-dependent amplitude ⇒non-uniform phase quantization steps

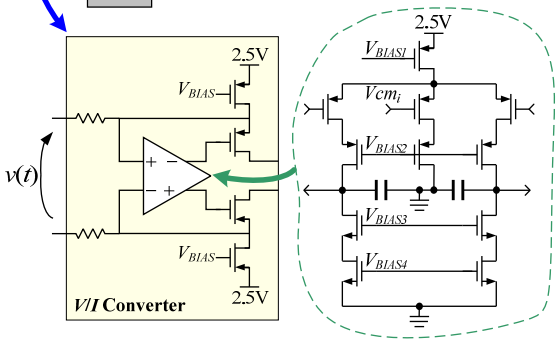
Phase Quantization Solution



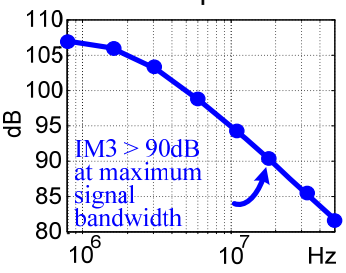
Non-uniform phase quantization avoided by only considering high-to-low transitions

V/I Details



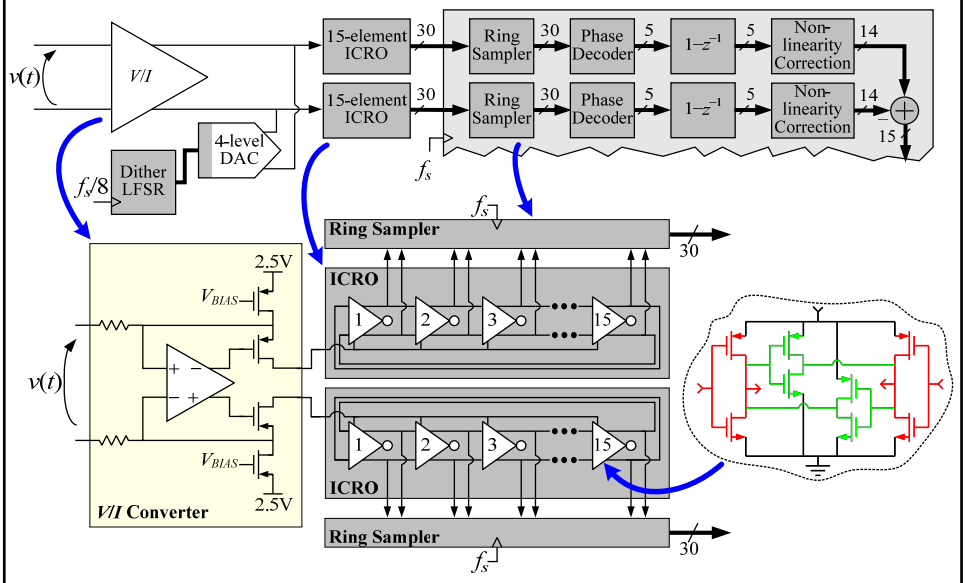


Simulated IM3 for a 0dBFS, 2-tone, out-of-band input:

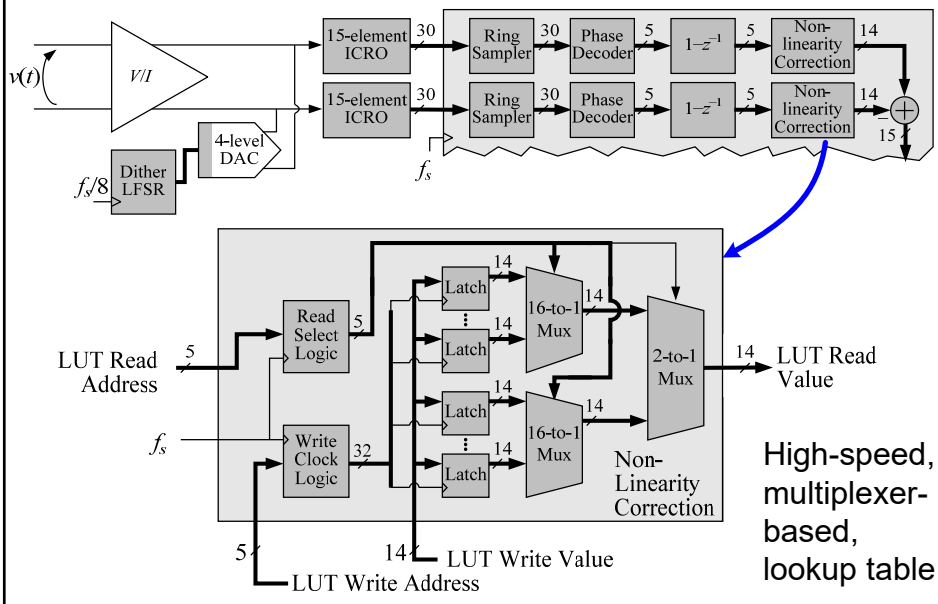


Amplifier bandwidth limited by only by f_T of devices in feedback path $\Rightarrow$ *V*/I bandwidth increases with process technology

Simplified Diagram of V/I and ICRO Circuits



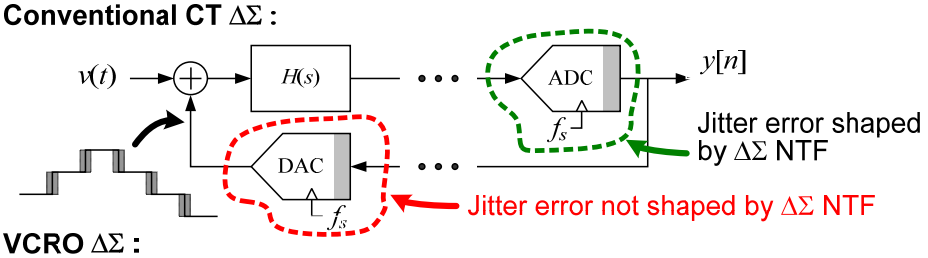
Nonlinearity Correction Block



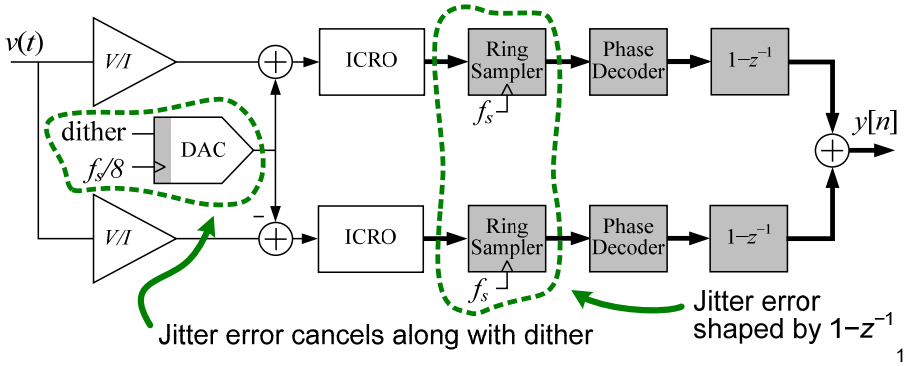
High-speed, multiplexer-based, lookup table

The VCRO ΔΣ Has Low Clock Jitter Sensitivity

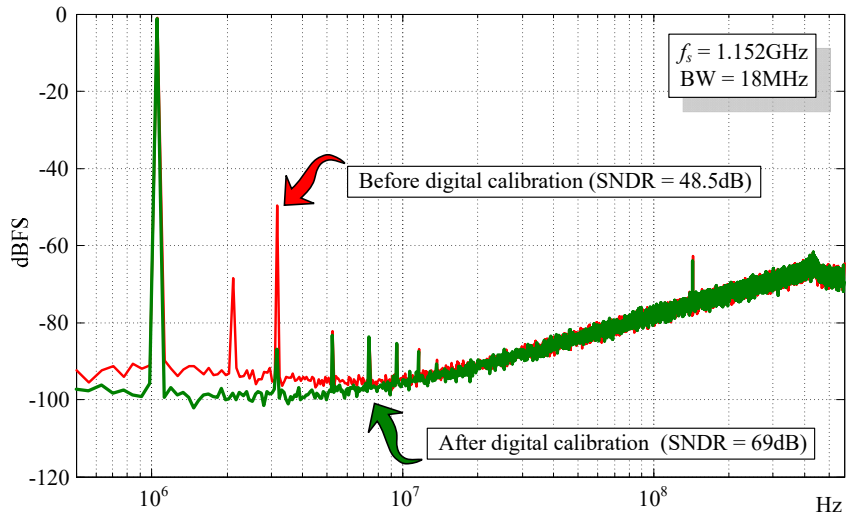
Conventional CT ΔΣ :



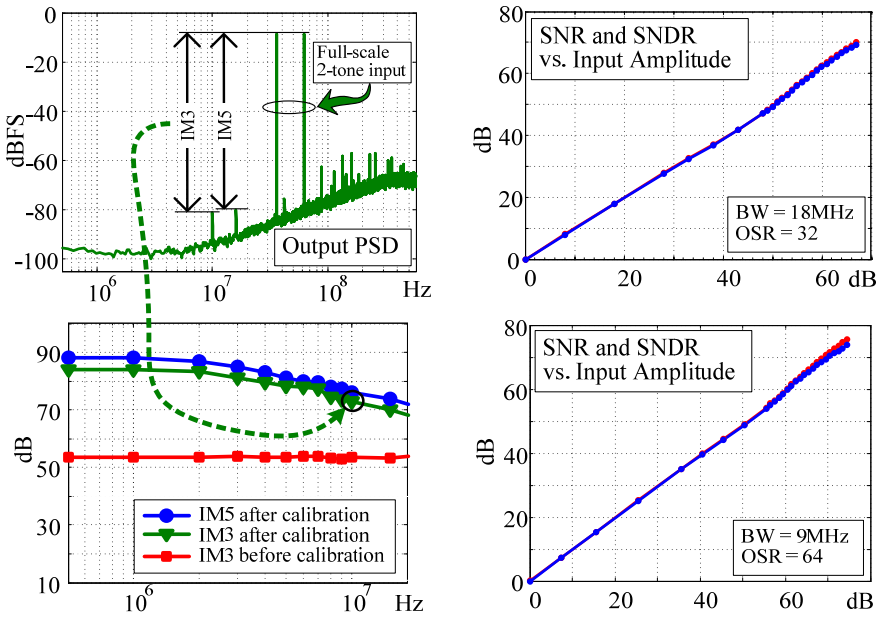
VCRO ΔΣ :



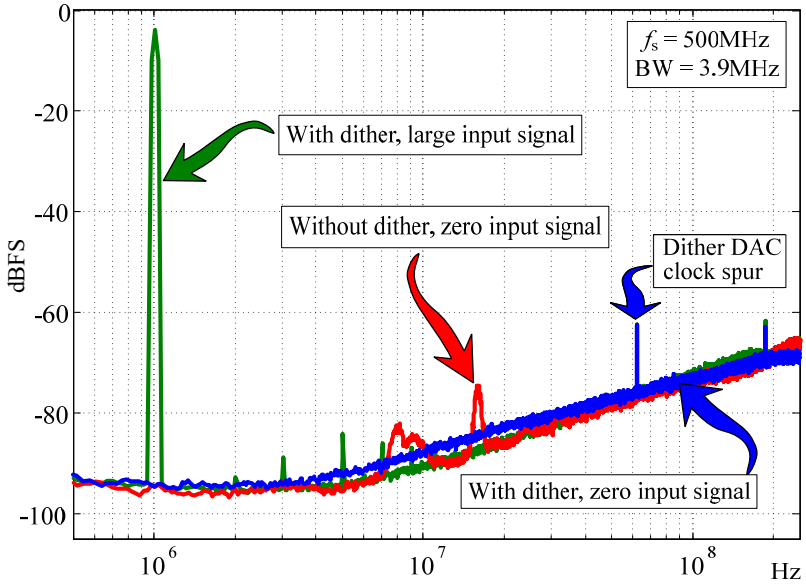
Measured Output Spectra



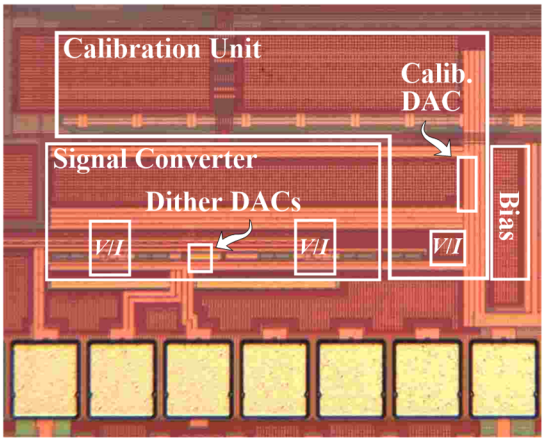
Measured PSD, IMD, SNR, and SNDR



Measured Output Spectra



Die Photograph



- Signal converter area = 0.040mm^2
- Calibration unit area = 0.060mm^2
- I and Q ADCs share one calibration unit
  $\Rightarrow$ Area per converter = 0.07mm^2

Worst-Case Measured Performance Summary

Process / Package	TSMC 65nm LP / 64 pin LFCSP	
Active area	0.07 mm^2	
f_s range	500 − 1152 MHz	
Number of ADCs tested	10	
f_s	1152 MHz	500 MHz
Signal bandwidth	18 MHz	3.9 MHz
Peak SNR	70 dB	71.5 dB
Lowest peak SNDR	67 dB	71 dB
f_{in} at which lowest peak SNDR occurs	5 MHz	1 MHz
Power dissipation: Analog + Digital = Total	5 + 12 =17 mW	2.5 + 5.5 = 8 mW

Relative to best published comparable CT ΔΣ ADCs have:

- Much smaller area
- Lower clock jitter sensitivity
- Greater reconfigurability
- Higher sample-rate
- Two supply voltages (2.5V for *V*/I converter, 1.2V for all else)
- Worse figure of merit by 2-5 dB (in this process)

Conclusion

- Have presented the first high-performance stand-alone VCO-based $\Delta\Sigma$ ADC enabled by digital background correction of VCO nonlinearity and self-cancelling dither
- Unlike conventional ADCs it does not require:
  - Analog integrators
  - Feedback DACs
  - Reference voltages
  - Comparators
  - A low-jitter clock
- Its performance is limited mainly by the speed of digital circuitry, so unlike conventional ADCs its performance improves as CMOS technology scales