Presented at the 2009 IEEE International Solid-State Circuits Conference

A 130mW 100MS/s Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction

Andrea Panigada, Ian Galton

University of California at San Diego, La Jolla, CA

INTEGRATED SIGNAL PROCESSING GROUP

Motivation

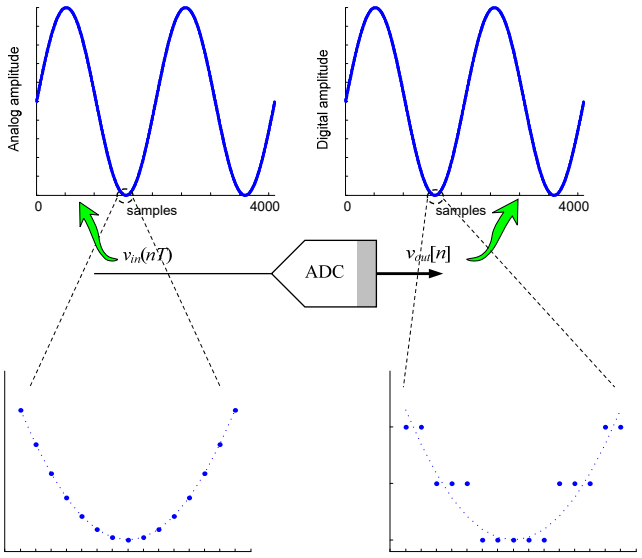
- In a conventional pipelined ADC:
  - High ADC accuracy $\Rightarrow$ high op-amp linearity
  - This dictates high power dissipation
- Alternatively, can save power using:
  - Op-amps with poor linearity
  - Digital background calibration to compensate for the nonlinearity*
- This talk presents a pipelined ADC enabled by a new such technique called Harmonic Distortion Correction (HDC)

*e.g., [Murmann, Boser, *IEEE J. Solid-State Circuits*, Dec. 2003]

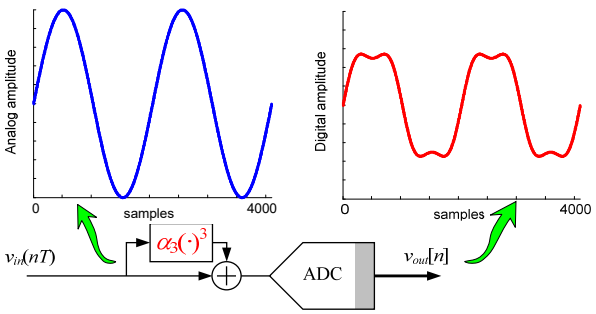
Outline

- The concept underlying HDC
- Application of HDC to pipelined ADCs
- Circuit details of the implemented pipelined ADC
- Measurement results

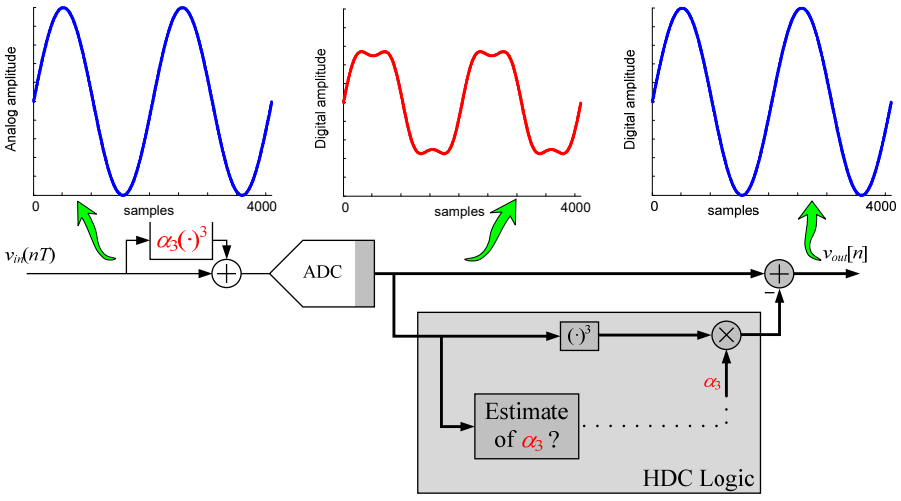
An Ideal High Resolution ADC



An ADC with 3rd-Order Distortion



Concept Underlying HDC

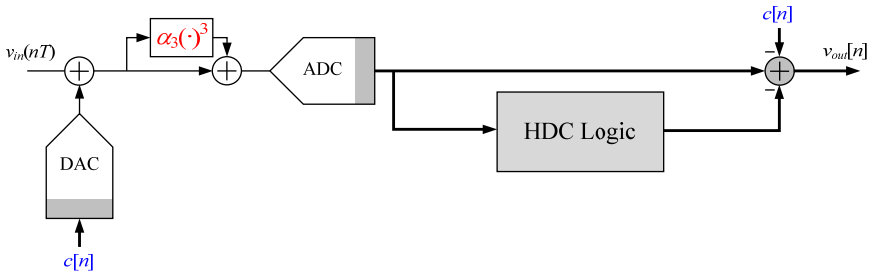


Could correct distortion at the output,
if the distortion coefficient α_3 were known

Concept Underlying HDC

Want:

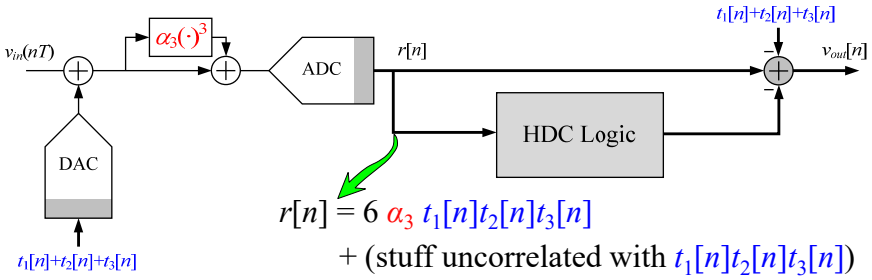
1. $c[n]$ to facilitate measurement of α_3 by HDC
2. $c[n]$ to be uncorrelated from $v_{in}(nT)$
3. $c[n]$ to have low amplitude



Concept Underlying HDC

Use: $c[n] = t_1[n]+t_2[n]+t_3[n]$

where $t_k[n] = \pm A$ (2-level), independent, zero mean pseudo-random sequences



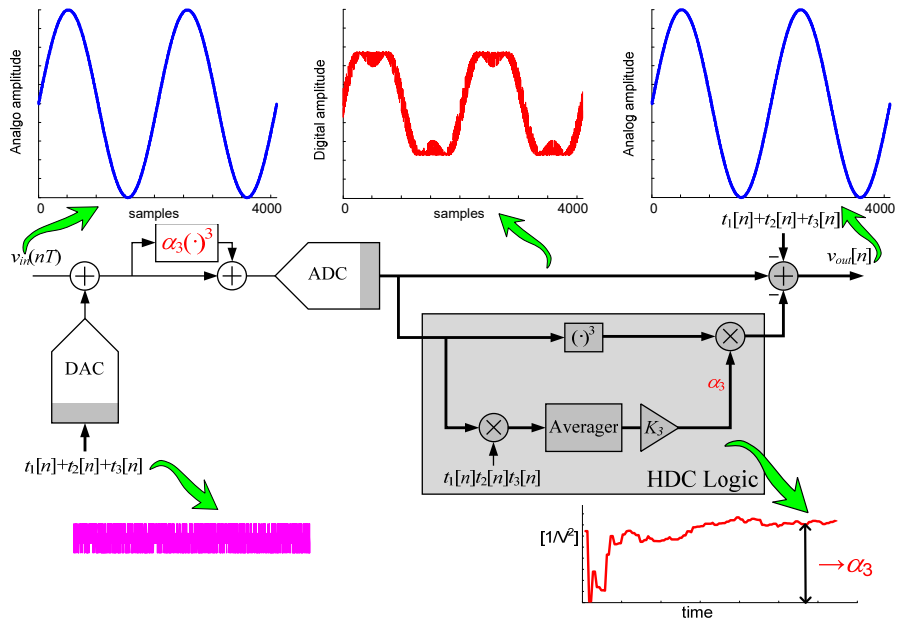
$r[n] = 6\ \alpha_3\ t_1[n]t_2[n]t_3[n]$

$+$ (stuff uncorrelated with $t_1[n]t_2[n]t_3[n]$)

$\Rightarrow r[n]\ t_1[n]t_2[n]t_3[n] / (6\ A^6) = \alpha_3 +$ zero mean random sequence

$\Rightarrow$ averages to α_3

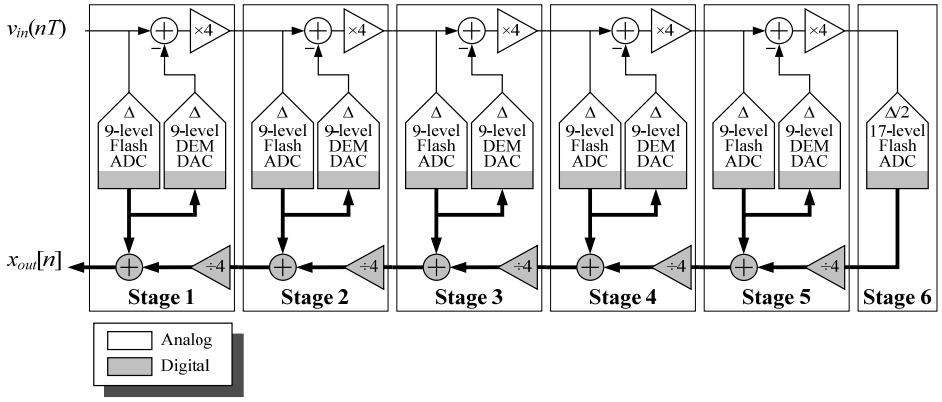
Concept Underlying HDC



Still to be Discussed…

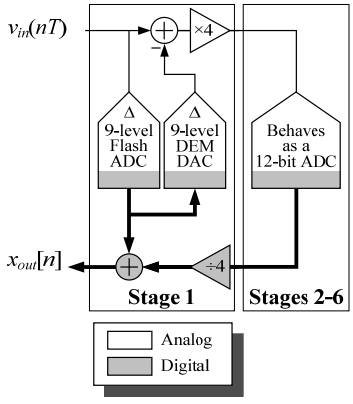
- This simple model so far has assumed:
  - No ADC gain error
  - Only third-order distortion
  - An ideal DAC
  - Negligible quantization noise
- These issues will be addressed soon in the context of the pipelined ADC

14-bit Pipelined ADC Architecture



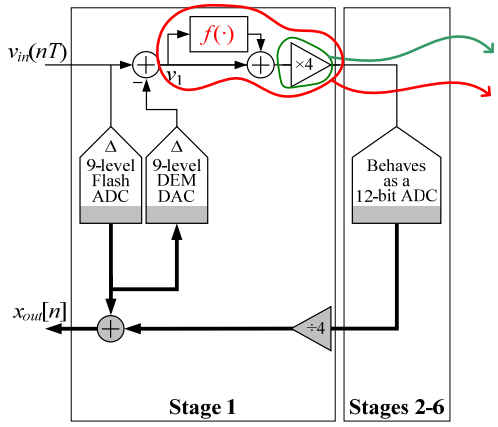
- Input sample-and-hold not shown
- Delays not shown

Behavior of Stages 2-6



Property: two adjacent stages with *n* and *m*-bit resolution behave as a single (*n*+*m*-1)-bit stage

Residue Amplifier Distortion Problem



Ideal residue amp behavior

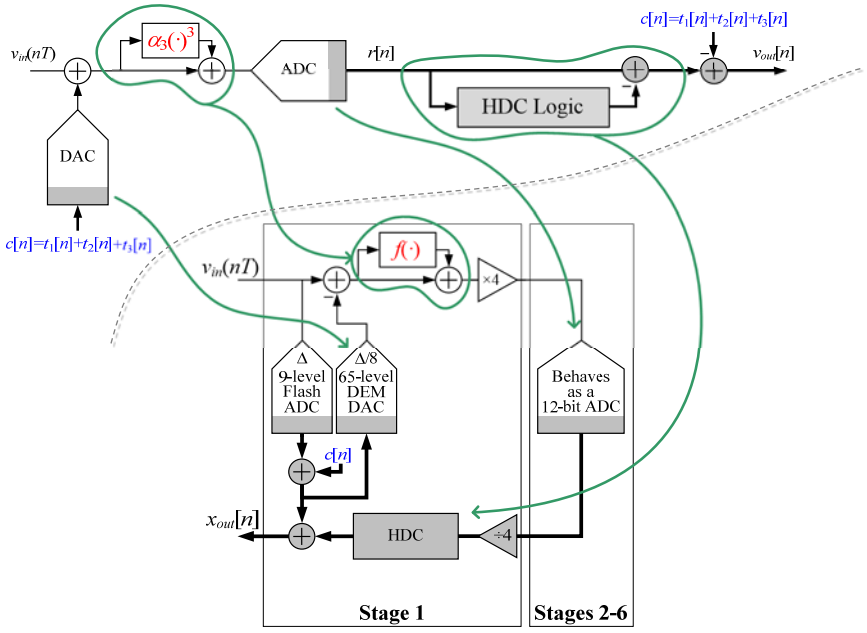
Real residue amp behavior

$$f(v_1) = \sum_{k=1}^{N} \alpha_k v_1^k$$

Typical: $f(v_1) \approx \alpha_1 v_1 + \alpha_3 v_1^3$

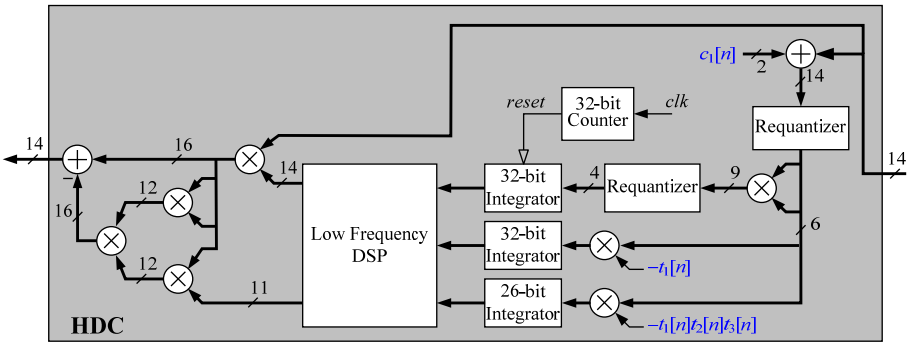
- **Problem:** high SNDR $\Rightarrow \alpha_k \approx 0 \Rightarrow$ high power consumption
- **Solution:** reduce residue amp power in trade for large α_k, correct using HDC

HDC Concept Applied to the Pipeline



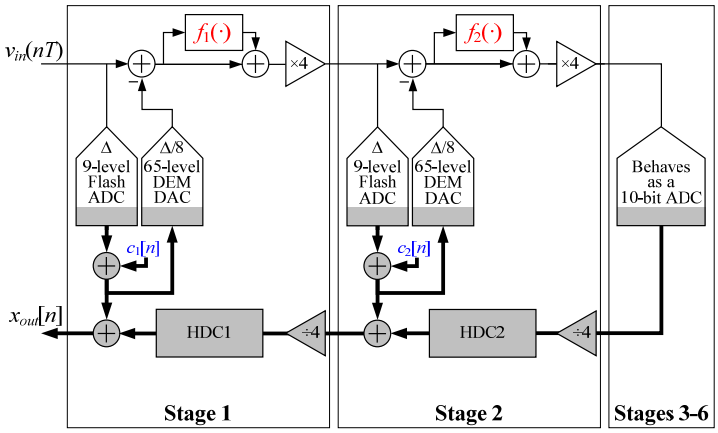
HDC Extension to Handle α_1 and α_3

- Recall typical distortion: $f(v_1) \approx \alpha_1 v_1 + \alpha_3 v_1^3$
- Must combine estimation & correction for α_1, α_3



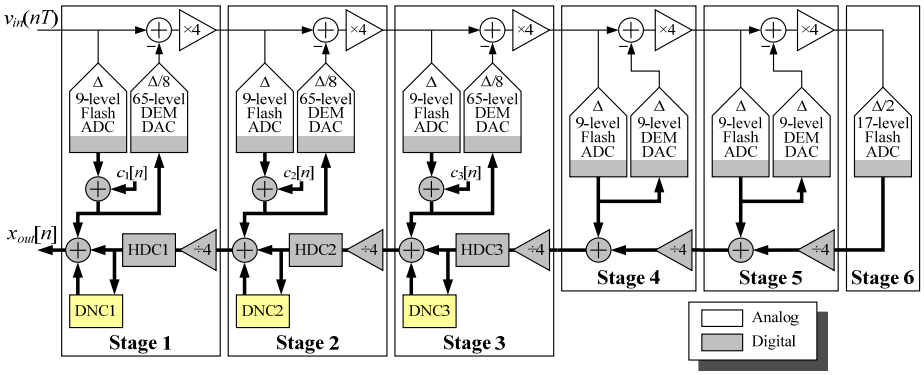
[Panigada, Galton, *IEEE Trans. on Circ. and Sys. I*, Sept. 2006]

Application of HDC to Other Stages



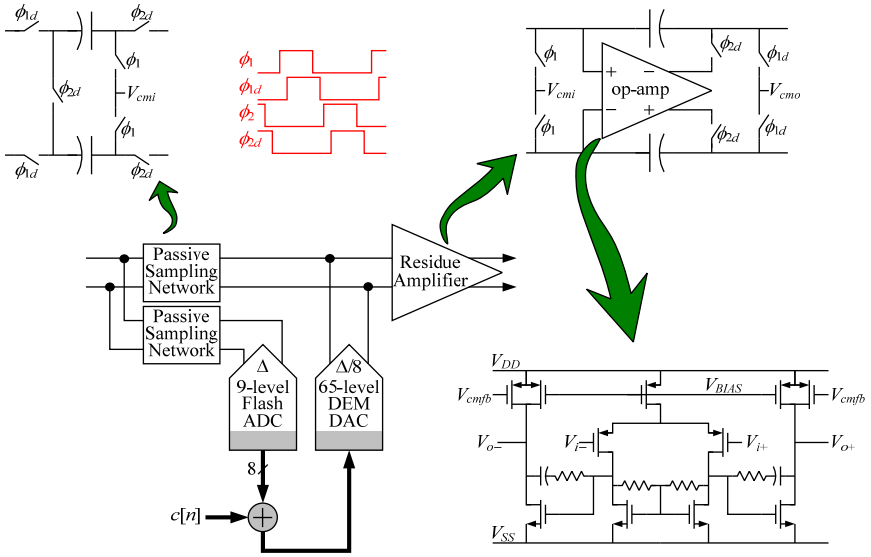
- HDC could be applied to all stages
- But typically it is only required in first few stages

14-bit 100MS/s Pipeline ADC



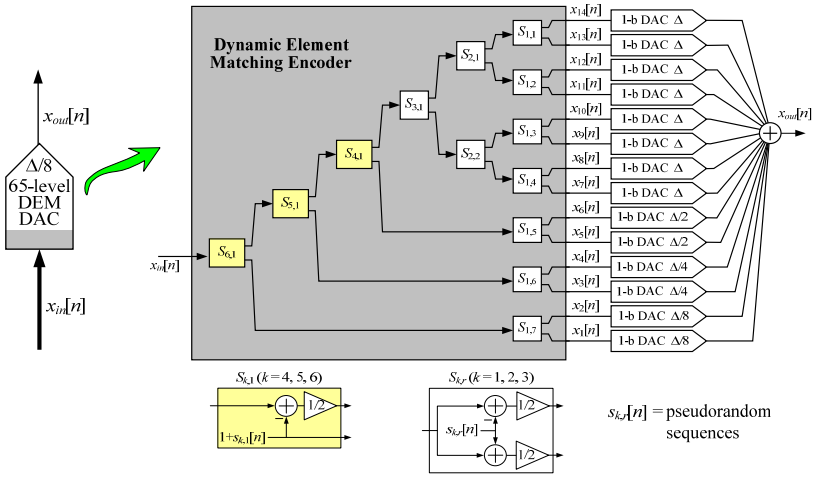
- Dynamic Element Matching (DEM) to scramble DAC mismatches
- DAC Noise Cancellation (DNC) implemented as in [Siragusa, Galton, *IEEE J. Solid-State Circuits*, Dec. 2004]

Stage Implementation Details



DEM DAC Signal Processing

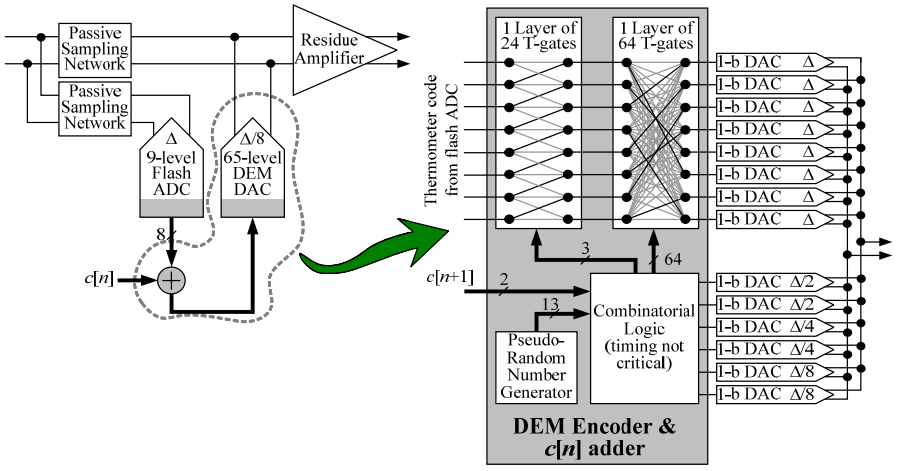
Segmented DAC to reduce area and complexity:



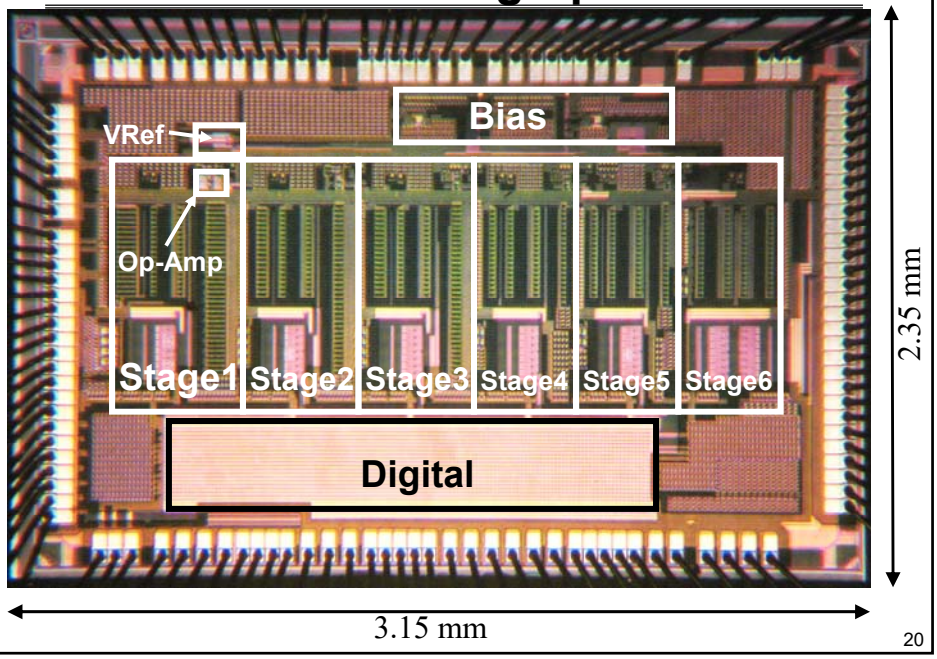
[Chan, Zhu, Galton, *IEEE J. Solid-State Circuits*, Sept. 2008]

Low-Latency Implementation

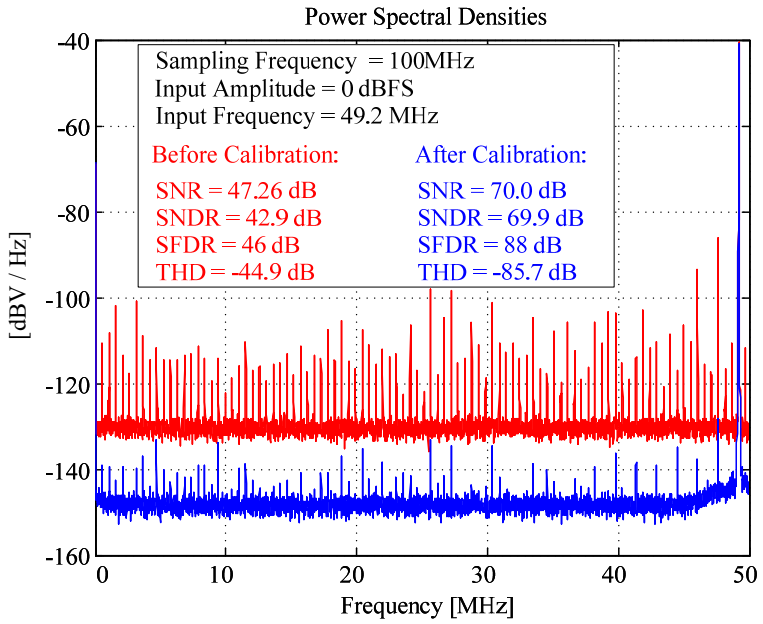
- DEM tree structure and $c[n]$ adder logic are flattened together
- Computations that don't need ADC data are done in advance
- Remaining computations are done with 2 T-gate layers



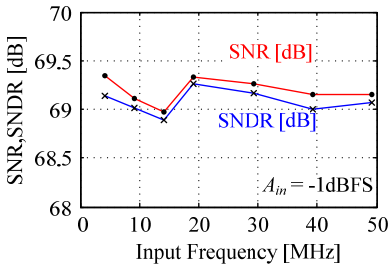
Die Photograph

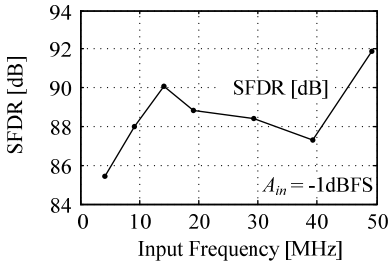


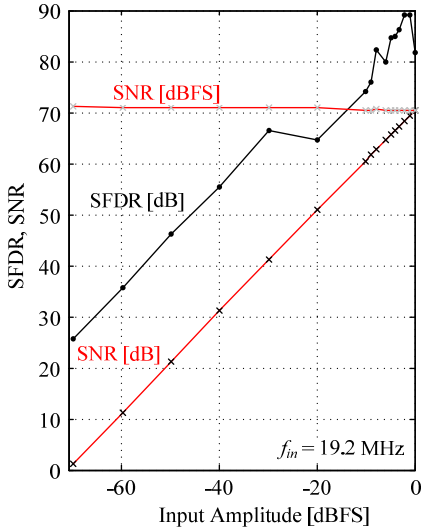
Typical Measured Output Spectra



Measured SNR, SNDR, and SFDR







Measured Performance Table

Design Details						
Technology	90 nm CMOS					
Package	56 pin QFN					
Die Size Including Pads and ESD Protection	2.15 mm × 3.35 mm					
Active Area	4 mm^2					
Digital Calibration	on-chip					
Voltage References	on-chip					
Worst Case Measured Results Over Nyquist Band for f_s = 100 MHz						
Power Supplies	**V_{DD} Test Case 1**			**V_{DD} Test Case 2**		
	V_{DD}	Power Dissipation		V_{DD}	Power Dissipation	
Analog	1.2 V	93 mW	130 mW	1.0 V	62 mW	92 mW
Digital	1.0 V	17 mW		0.7 V	7 mW	
Clock Generator	1.0 V	1 mW		1.0 V	1 mW	
Clock Drivers and DEM	1.35 V	19 mW		1.35 V	22 mW	
Performance with HDC and DNC On						
Peak *SNR*	70 dB			68.3 dB		
SNDR at −1dBFS	68.8 dB			66.6		
SFDR at −1dBFS	85 dB			75 dB		
2-tone *SFDR* at −1dBFS	86 dB			80 dB		
Maximum *INL*	3.6 LSB			3.8 LSB		
Maximum *DNL*	0.54 LSB			0.39 LSB		

Worst case over all the three tested boards

Comparison to Prior ADCs

Reference or Part Number	f_s (MS/s)	*SNDR* (dBFS)	*SFDR* (dB)	V_{DD} (V)	P_{tot} (mW)	*FOM*1 (pJ/step)	*FOM*2 (pJ·V/step)
[3]	75	68	76	3	314	2.04	6.12
LTC2259	80	73	90	1.8	93	0.32	0.57
AD9233	80	70.5	90	1.8	248	1.13	2.03
ADS6123	80	72.3	89	3.3	318	1.18	3.89
LTC2260	105	73	90	1.8	112	0.29	0.53
AD9233	105	70.5	90	1.8	320	1.11	2.00
ADS6124	105	72.3	84	3.3	374	1.06	3.49
[6]	250	65.9	82	1.8	150	0.37	0.67
This work	100	69.8	85	1.2	130	0.52	0.62
This work	100	67.6	75	1.0	92	0.47	0.47

$$FOM1 = \frac{P_{tot}}{2^{ENOB} f_s} \quad \text{and} \quad FOM2 = FOM1 \times V_{DD} \quad \text{where} \quad ENOB = \frac{SNDR - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

Design Issues

- **Limitations of our design**
  - HDC convergence time is 120 seconds
  - Stages 2-6 are not optimized so area and power are higher than necessary
- **Practical solutions**
  - HDC auto-calibration phase would reduce convergence time to < 1 second
  - Fewer bits per stage after stage 1 and more aggressive scaling would reduce power and area

Conclusion

Have:

- Explained the concept underlying HDC
- Explained how HDC can be applied to pipelined ADCs
- Presented a 14-bit 100MS/s pipelined ADC enhanced with HDC

The work demonstrates:

- HDC enables high ADC resolution despite low-power, low-voltage circuitry
- HDC complements DEM and DNC

Acknowledgements

The authors would like to thank:

- Nevena Rakuljic[1], for technical advice and analog layout assistance
- Everest Zuffetti[2], for technical advice, digital synthesis, and place & route
- Angelo Contini[2], for CAD support
- Gerry Taylor[1] and Kevin Wang[1] for valuable technical advice
- Cuong Vu[1], for lab assistance
- Maurizio Zuffada[2]: for support of this research project
- Pietro Erratico[2]: for early-stage support of this project

[1] UCSD
[2] STMicroelectronics