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Spurious-Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHz Fractional-*N* PLL

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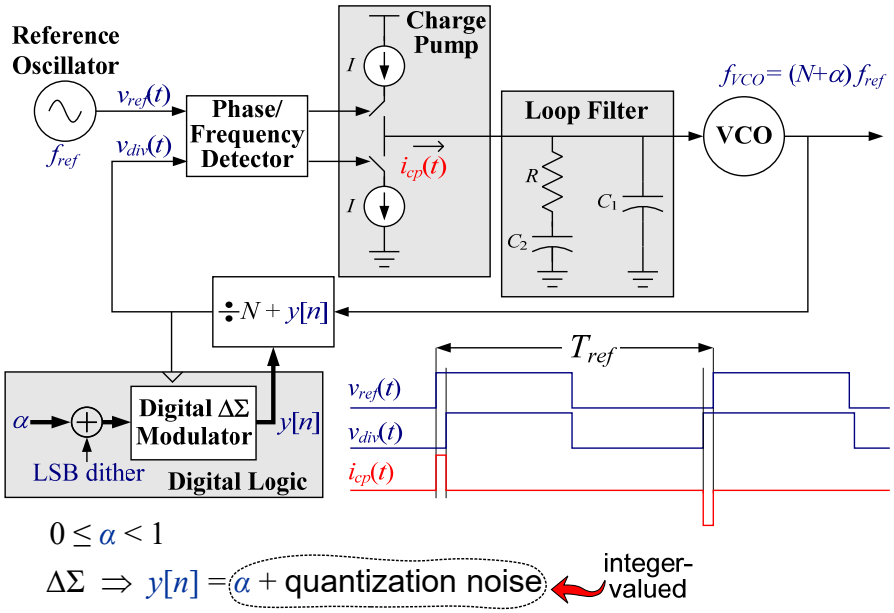
Outline

- Overview of spurious tones in fractional-*N* PLLs
- The two mechanisms that cause fractional spurs
- A replacement for the $\Delta\Sigma$ modulator to mitigate one of the mechanisms
- A charge pump offset and sampled loop filter to mitigate the other mechanism
- Circuit details and measurement results

A Typical Fractional-*N* PLL

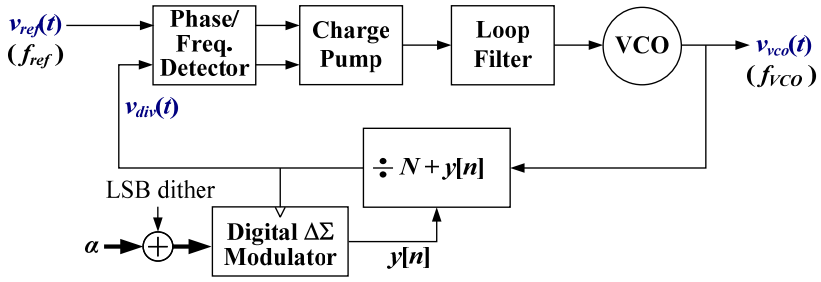


$0 \le \alpha < 1$

$\Delta\Sigma \Rightarrow y[n] = \alpha +$ quantization noise

integer-valued

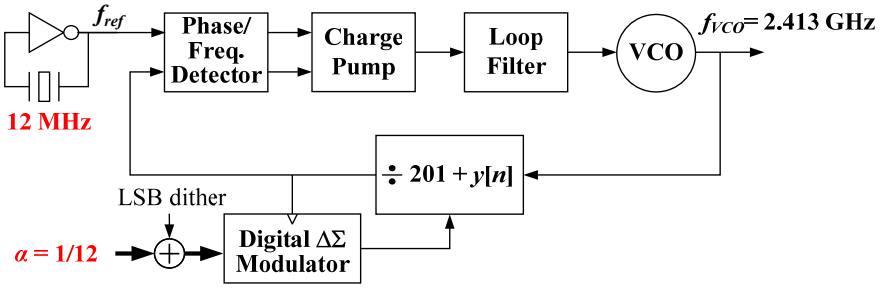
Spurs in Phase Noise are Unavoidable



- Fractional-*N* PLLs always contain *spurious tones*
- Have *reference spurs* at multiples of f_{ref} just like integer-*N* PLLs
- Also have *fractional spurs* at multiples of αf_{ref} and $(1-\alpha) f_{ref}$

Fractional Spur Overview

- Example

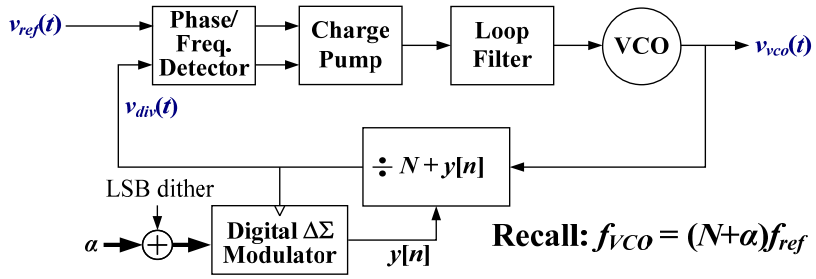


$\Rightarrow$ fractional spurs at multiples of αf_{ref} = 1 MHz

- In general, a PLL lowpass filters fractional spurs
  - Effective only for spurs above the loop bandwidth (LBW)
  - Spurs within the LBW are unfiltered (typ. > -60dBc)

$\Rightarrow \alpha, f_{ref}$, and PLL BW affect fractional spur power

The Two Fractional Spur Mechanisms



Mechanism 1:

Non-linear coupling of $v_{ref}(t)$ and $v_{vco}(t)$ (or $v_{div}(t)$)

e.g., [N^{th} harmonic in $v_{ref}(t)$]$\times v_{vco}(t) \Rightarrow \alpha f_{ref}$ spur

Mechanism 2:

ΔΣ quantization noise passing through non-linearities

(same spur frequencies as Mechanism 1)

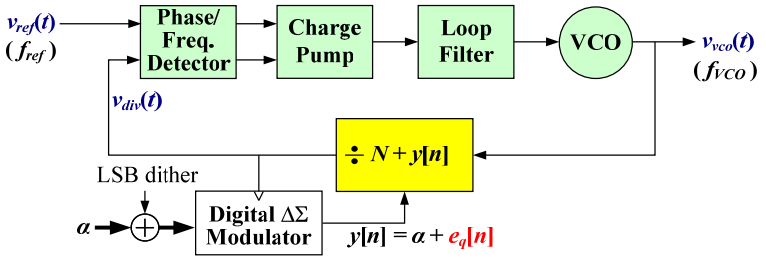
Let's focus on Mechanism 2…

Fractional Spur Mechanism 2

Non-linearities come from the analog circuits:

- Non-linearities in the divider operate on $e_q[n]$
- Non-linearities from other blocks operate on $\sum_{k=0}^{n} e_q[k]$

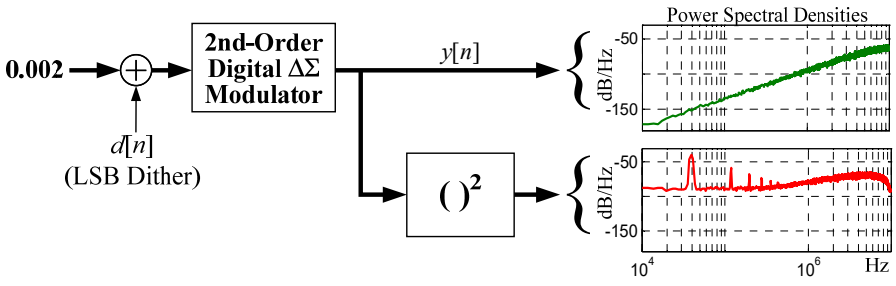
"running sum of $e_q[n]$"



If the non-linearity applied to $e_q[n]$ or its running sum causes spurs, then the PLL's phase noise contains spurs

Fractional Spur Mechanism 2

Example: Effect of second-order distortion:



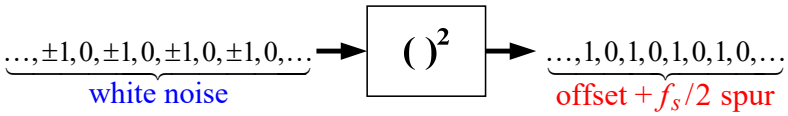
- Similar results occur with other types of non-linear distortion
- Similar results occur regardless of the ΔΣ modulator and dither used

  ⇒ The ΔΣ modulator is the root cause of the problem!

Plausibility Argument for Mechanism 2

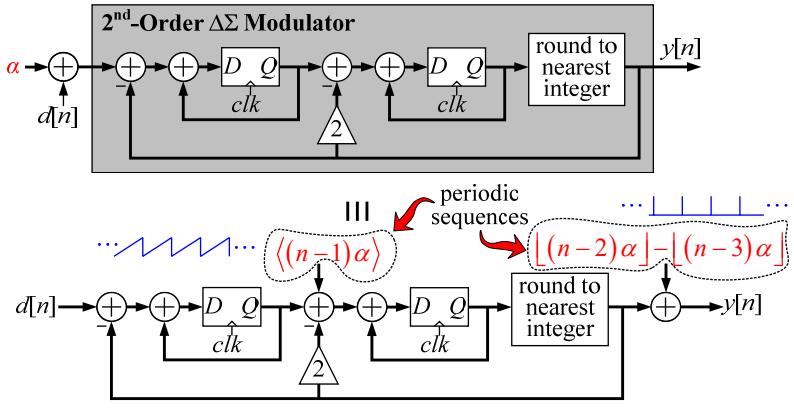
Q: How can non-linear distortion create spurs from a "spur-free" sequence?

A: The following example gives a simple "plausibility demonstration":



The randomness in the input is *sufficient* to ensure no spurs.
However, it is *insufficient* to ensure that its square is spur-free.

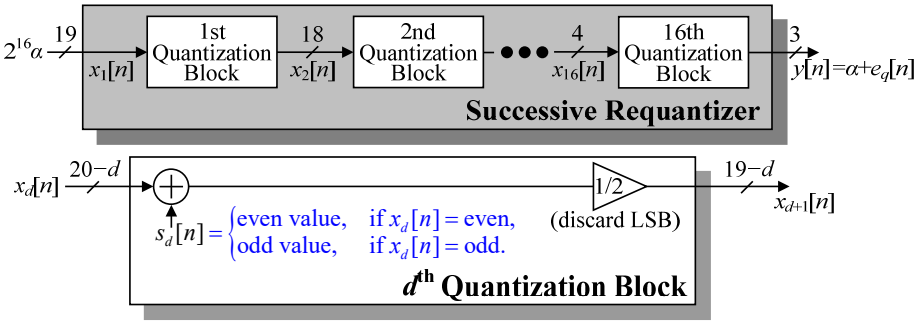
Details of Mechanism 2



where $\langle x \rangle$ = fractional part of x, and $\lfloor x \rfloor = x - \langle x \rangle$

- Each periodic sequence has spurs. Randomness from the dither prevents spurs in $y[n]$, but not in $y^k[n]$ for $k > 1$
- Similar effect as in previous example

A ΔΣ Modulator Replacement



- $2^{16}\alpha$ = integer (resolution of α is 2^{-16})
- Each QB divides by two and quantizes by one bit
- LSB of $s_d[n] + x_d[n]$ is zero so discarding it implements ÷2
- $e_q[n]$ is a linear combination of the $s_d[n]$ sequences
- $s_d[n]$ sequences must have properties desired of $e_q[n]$

Must Design Good $s_d[n]$ Sequences

Quantization block operation: $x_{d+1}[n] = \frac{1}{2}\left(x_d[n] + s_d[n]\right)$

In this work, have designed $s_d[n]$ to:

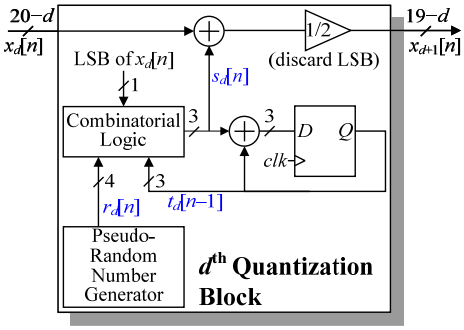
1. Ensure that the bit-width of $x_{d+1}[n]$ is that of $x_d[n]$ minus one
   $\Rightarrow$ parity of $s_d[n]$ must equal parity of $x_d[n]$
   $\Rightarrow$ magnitude of $s_d[n]$ must not be too large
2. Keep $t_d[n]$ bounded ($\Rightarrow$ 1st-order shaped PSD)
3. Prevent spurs in $(s_d[n])^p$, $p = 1, \ldots, 5$, and $(t_d[n])^q$, $q = 1, 2, 3$ (this requires $s_d[n] \in \{0, \pm 1, \pm 2, \pm 3\}$)

where $t_d[n]$ is the running sum of $s_d[n]$

Tradeoff: Achieving item 3 increases power of $s_d[n]$

This work uses a phase noise canceling PLL to avoid problem

The Quantization Block Details



Combinatorial Logic Truth Table:

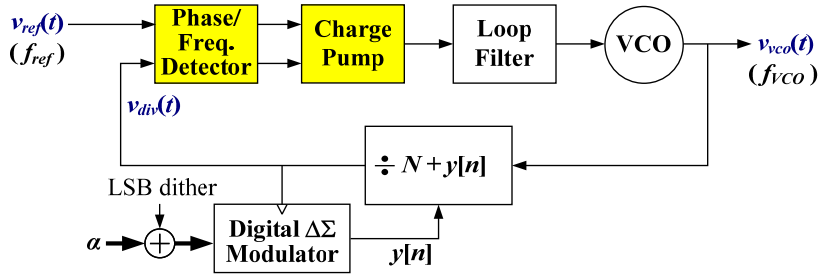
LSB of $x_d[n] = 0$		
$t_d[n-1]$	$r_d[n]$	$s_d[n]$
2	≥ 0 and ≤ 3	0
2	≤ −1 or ≥ 4	−2
1	≤ −1 or ≥ 6	0
1	≥ 0 and ≤ 5	−2
0	0 or 1	2
0	≤ −1 or ≥ 4	0
0	2 or 3	−2
−1	≤ −1 or ≥ 6	0
−1	≥ 0 and ≤ 5	2
−2	≥ 0 and ≤ 3	0
−2	≤ −1 or ≥ 4	2

LSB of $x_d[n] = 1$		
$t_d[n-1]$	$r_d[n]$	$s_d[n]$
2	≤ −1 or ≥ 4	−1
2	≥ 0 and ≤ 3	−3
1	≥ 1 and ≤ 3	1
1	≤ −1 or ≥ 4	−1
1	0	−3
0	≥ 0	1
0	≤ −1	−1
−1	≥ 1 and ≤ 3	−1
−1	≤ −1 or ≥ 4	1
−1	0	3
−2	≤ −1 or ≥ 4	1
−2	≥ 0 and ≤ 3	3

- $t_d[n]$ = running sum of $s_d[n]$
- $t_d[n]$ kept bounded ⇒ 1st-order PSD shape
- No spurs in $(s_d[n])^p$, $p = 1, 2, \ldots, 5$, and $(t_d[n])^q$, $q = 1, 2, 3$
- See [Swaminathan, et. al., *IEEE Trans. Signal Processing*, Nov. 2007] for the math

Fractional Spur Mechanism 1

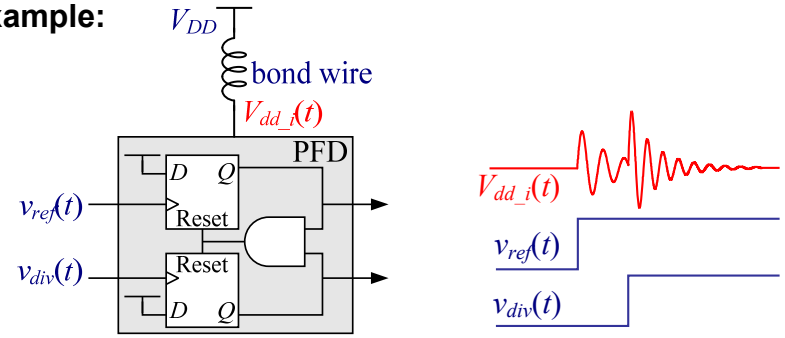
- Non-linear coupling of $v_{ref}(t)$ and $v_{vco}(t)$ (or $v_{div}(t)$) cause fractional spurs at multiples αf_{ref} and $(1-\alpha)f_{ref}$
- The greatest opportunities for such coupling occur in the PFD and CP because they process signals aligned to $v_{ref}(t)$ and $v_{div}(t)$:



Fractional Spur Mechanism 1

Power supplies to the PFD and CP are the main coupling paths

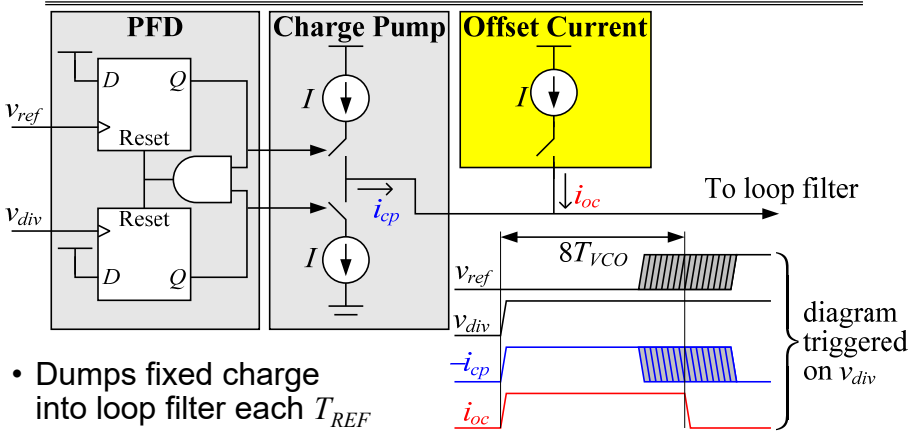
Example:



- The $v_{ref}(t)$ edge causes ringing through the V_{DD} bond wire
- If ringing persists to the next $v_{div}(t)$ edge, the output of the bottom flip-flop is affected by $v_{ref}(t)$ as well as $v_{div}(t)$

  $\Rightarrow$ non-linear coupling of $v_{ref}(t)$ and $v_{div}(t)$

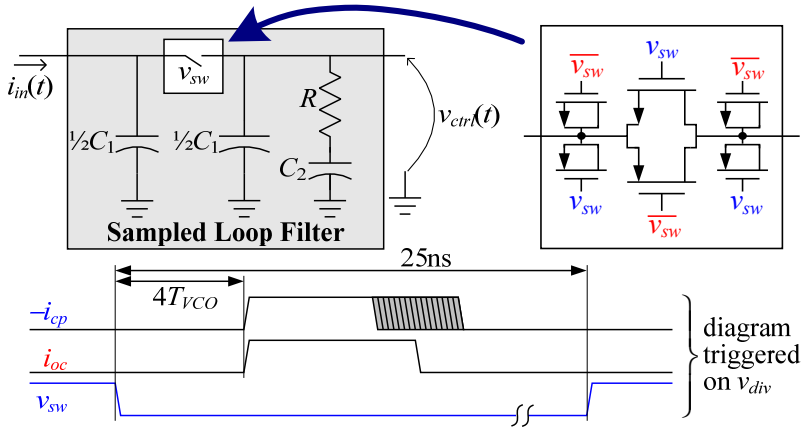
Offset Current to Separate PFD Edges



- Dumps fixed charge into loop filter each T_{REF}
- This separates edges of v_{ref} and v_{div}

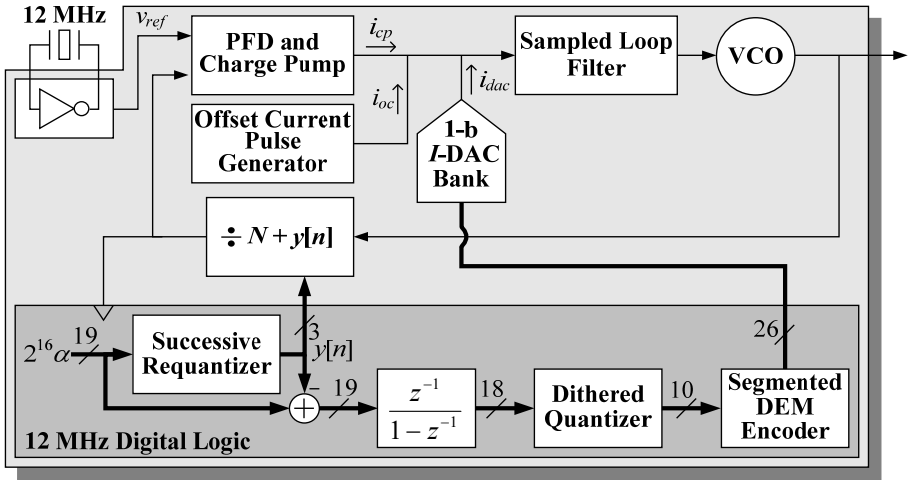
  $\Rightarrow$ V_{DD} ringing has time to die out
- Similar method in [Temporiti, et. al., *IEEE JSSC*, Sept. 2004]
- But current source mismatches cause big reference spur!

Sampled Loop Filter to Suppress Ref Spur



- Switch is closed only when $i_{in} = 0$
  $\Rightarrow$ current source mismatches do not cause reference spur
- Charge injection sees $R \approx$ open circuit, so it splits evenly
  $\Rightarrow$ minimizes reference spur caused by charge injection

High-Level Diagram of IC

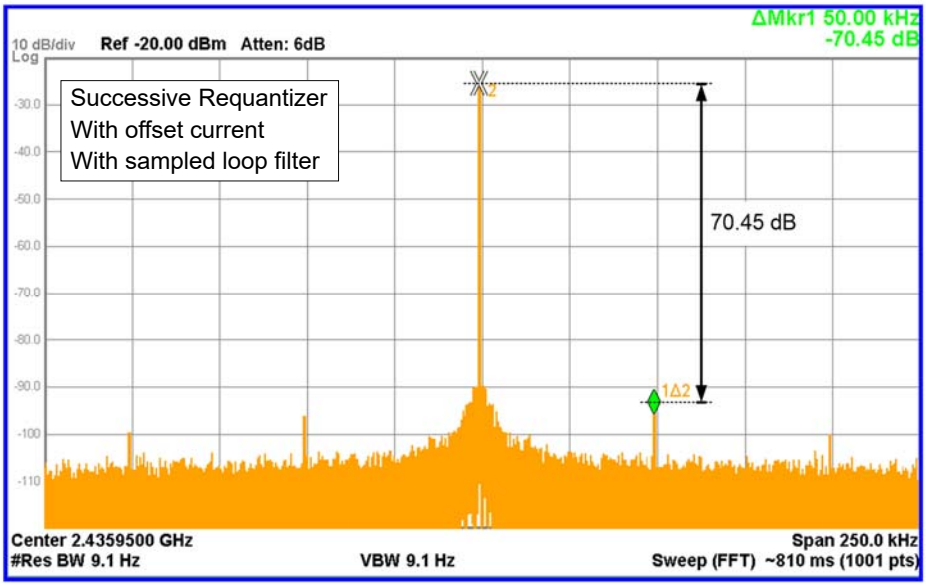


- $f_{VCO} \in$ 2.4 GHz ISM band; f_{ref} = 12 MHz; PLL BW = 975 kHz
- Phase noise cancellation with calibration (not shown) as in [Swaminathan, et. al., *IEEE JSSC*, Dec. 2007]

Other IC Details

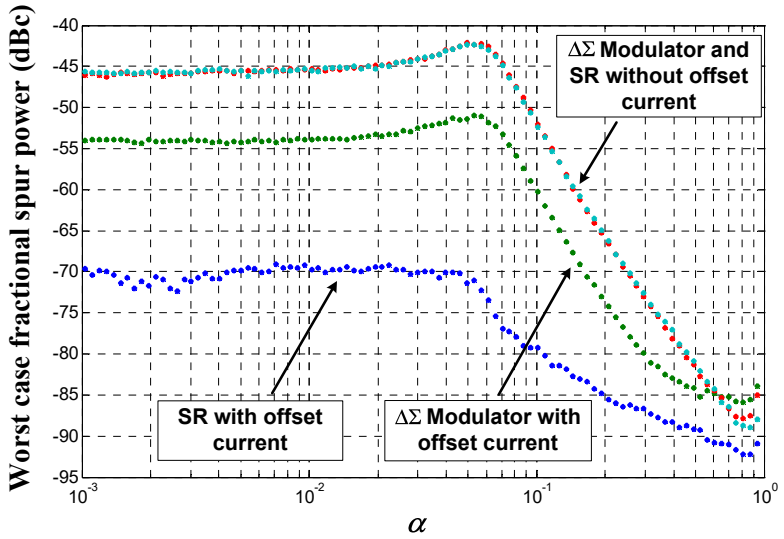
- **Divider**: Pulse-swallowing 2/3 dividers; 2 stages CML, 5 stages CMOS
- **VCO**: $-g_m$ CMOS LC; coarse switched-capacitor tuning in 12MHz steps
- **Loop Filter**: On-chip; Poly and MiM capacitors; poly resistors with coarse tuning to account for PVT shift
- **Test Features**:
  - can select the SR or a 2nd-order ΔΣ modulator
  - can disable the offset current pulse generator
  - can enable conventional loop filter operation

Typical Measured Close-In Fractional Spur

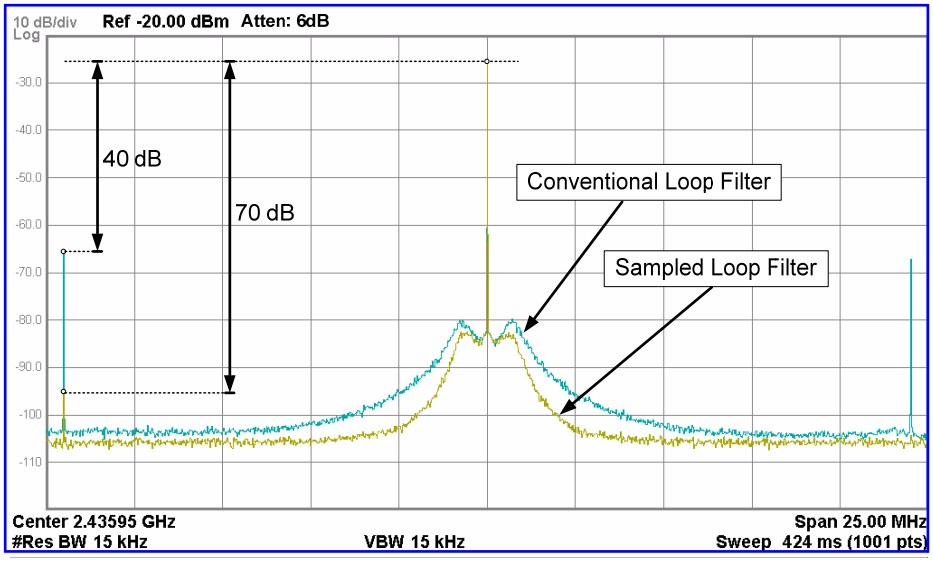


Measured Fractional Spur Levels

Comparison between ΔΣ Modulator and SR with and without offset current:



Measured Effect of Sampled Loop Filter

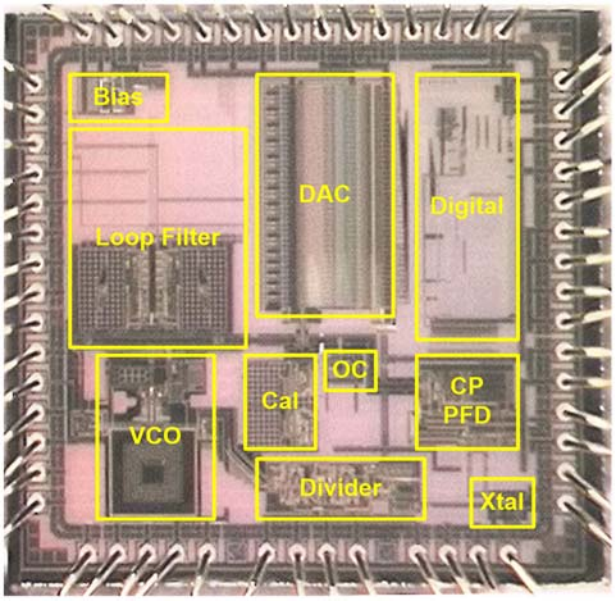


Performance Table

Design Details		
Technology	0.18 um 1P6M CMOS	
Package and die area	32 pin TQFN, 2.2 × 2.2 mm^2	
Reference frequency, output frequency band	12 MHz, 2.4 – 2.5 GHz	
Measured loop bandwidth	975 kHz	
Measured Current Consumption (V_{DD} = 1.8V)		
VCO and divider buffer	5.9 mA	Core 27.1 mA
Divider	7.3 mA	
Charge pump, PFD, and buffers	8.6 mA	
Offset current pulse generator	0.6 mA	
Digital	1.9 mA	
DAC	2.8 mA	
Bandgap ref, crystal buffer, external buffer	9.8 mA	
Measured Fractional-N Performance		
Phase noise at 100 kHz	-98 dBc/Hz	
Phase noise at 3 MHz	-121 dBc/Hz	
Worst case inband fractional spur†	-64 dBc	
Worst case reference spur	-70 dBc	

†Over 4 IC copies each measured with 100 values of $0 < \alpha < 1$

Die Photograph



Conclusion

- Have identified the $\Delta\Sigma$ modulator as a major source of fractional spurs in fractional-*N* PLLs.
- Have demonstrated the SR, as a replacement for the $\Delta\Sigma$ modulator, significantly mitigates the problem.
- Have used a charge pump offset technique to realize the benefits of the SR and a sampled loop filter to prevent the offset technique from causing a large reference spur.
- Have demonstrated state-of-the-art fractional and reference spur performance based on these techniques in a phase noise canceling fractional-*N* PLL.