A Wide-Bandwidth 2.4GHz ISM Band Fractional-N PLL with Adaptive Phase Noise Cancellation

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Outline

- Phase-Noise Canceling Phase-locked loops
- Adaptive Phase-Noise Cancellation
- Circuits
- Experimental Results
- Conclusion
**Fractional-N PLL Tradeoff**

A pity, because it also:
- reduces PLL settling time
- reduces sensitivity to VCO pulling
- enables an on-chip loop filter
- enables in-loop transmit modulation

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**Fractional-N Phase Noise**

- Each CP pulse is mostly ΔΣ quantization noise
- But the ΔΣ quantization noise is known, so it can be cancelled with a DAC
**ΔΣ Phase Noise Cancellation**

- The DAC cancels most of the ΔΣ quantization noise prior to loop filter so PLL bandwidth need not be small.

**Result of DAC Gain Error**

- Ideally, residual ΔΣ noise in $v_{ctrl}$ is zero except during CP and DAC pulses.
- DAC gain error spoils this result
  - $\Rightarrow$ Increased phase noise!
- Each halving of $f_{ref}$ increases the required matching accuracy by 9 dB!
A Sign-LMS algorithm adjusts $\Delta I_{bias}$ until DAC gain is correct

- Term proportional to $e_{cp}[n]$ remains in $v_{ctrl}$ if DAC cancellation is not perfect
- Since $\text{sgn}(e_{cp}[n]) \times e_{cp}[n] = |e_{cp}[n]|$, integrator ramps up or down until $\Delta I_{bias}$ is adjusted properly

What’s the Catch?

- $v_{ctrl}$ can have a large DC component (it sets the VCO freq)
- Hence, the LMS loop contains a large $\text{sgn}(e_{cp}[n])$ term
- But $\text{sgn}(e_{cp}[n])$ contains large spurious tones
- To suppress the tones, the LMS loop BW must be very low
  $\Rightarrow$ Very slow calibration settling, e.g., 1s in prior art
Proposed Adaptive Calibration

**Idea:** Split the VCO’s varactor into 2 parallel halves; use the common-mode voltage to control the VCO and the differential-mode voltage to control the calibration loop

- VCO is controlled by its common-mode input voltage, but is insensitive to differential-mode voltage
- The differential-mode voltage is now available to independently control calibration loop

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Proposed Adaptive Calibration Cont.

- Two parallel half-sized loop filters and varactors create differential signal path for calibration loop
- Multiplication by ±1 performed by current steering
- Calibration feedback loop is DC-free
The Calibration Loop Signal Path

The calibration loop is controlled by a differential-mode signal that has no DC component

⇒ Calibration signal does not have to be filtered out by the calibration loop
⇒ Can have a wide calibration loop BW!

The PLL Signal Path

The VCO output is insensitive to calibration signal
⇒ Calibration does not affect operation of PLL!
A Side-Effect of Wideband PLLs

If PLL BW is increased, must decrease CP noise to maintain same out-of-band performance

Example:

Case 1: PLL BW is 100kHz
Case 2: PLL BW is 500kHz but CP current sources are 64× larger than in Case 1 to reduce CP noise

⇒ CP current consumption becomes significant as PLL loop BW is increased
Dynamic CP Biasing to Save Current

- The CP pulses are on for only a fraction of the reference period, so the CP itself only consume 50 uA on average.

- But if the CP bias is left on for the whole reference period, it consumes 11 mA!

- By powering down the bias circuitry between CP pulses, the average current consumption is reduced by over 8 mA.

(circuit details on next slide)

CP & Bias Circuit Details

- $en_1$ and $en_2$ are high during CP pulse
- Cascode transistors switch pulses between loop filter halves
Cancellation DAC Structure

Segmented dynamic element matching used to eliminate harmonic distortion from non-ideal DAC weights and pulse shapes (extension of that in [Chan & Galton, ISSCC 06])

Segmented DEM Encoder

- $d_1[n]$, $d_2[n]$, ..., $d_9[n]$ are pseudo-random independent, white ±1 sequences
1-bit DAC Circuit Details

- $M_1$ and $M_2$ used to minimize injection of channel charge into loop filter
- Separate DAC connected to each loop filter

Additional Circuit Details

- **Divider**: Pulse-swallowing 2/3 dividers; 2 stages CML, 5 stages CMOS

- **VCO**: $-\frac{1}{g_m}$ CMOS LC; coarse switched-capacitor tuning in 12MHz steps

- **Calibration loop op-amp**: folded-cascode; 67dB DC gain, 28MHz UGBW

- **Loop Filter**: On-chip; Poly and MiM capacitors; poly resistors with coarse tuning to account for PVT shift

- **Digital**: 0.18$\mu$m standard cell library
Die Photograph

Measured Phase Noise
Calibration Loop Settling

Spurious Performance
Performance Table

<table>
<thead>
<tr>
<th>Design Details</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 0.18 μm 1P6M CMOS</td>
</tr>
<tr>
<td>Package and Die Area</td>
<td>32 pin TQFN, 2.2 × 2.2 mm²</td>
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<tr>
<td>Reference Frequency</td>
<td>12 MHz</td>
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<tr>
<td>Output Frequency</td>
<td>2.4 – 2.5 GHz</td>
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<tr>
<td>Loop Bandwidth</td>
<td>&gt; 730 kHz</td>
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<tr>
<td>Measured Core Current Consumption (at 1.8V)</td>
<td>20.9 mA</td>
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<tr>
<td>VCO and Divider Buffer</td>
<td>6.9 mA</td>
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<tr>
<td>Divider</td>
<td>5.8 mA</td>
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<tr>
<td>CP (dynamic biasing enabled)</td>
<td>2.7 mA</td>
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<tr>
<td>Digital</td>
<td>0.5 mA</td>
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<tr>
<td>DAC</td>
<td>3.6 mA</td>
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<tr>
<td>Calibration</td>
<td>1.4 mA</td>
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<tr>
<td>Measured Worst Case Integer-N Performance</td>
<td></td>
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<tr>
<td>Phase Noise @ 100 kHz</td>
<td>-104 dBc/Hz</td>
</tr>
<tr>
<td>Phase Noise @ 3 MHz</td>
<td>-120 dBc/Hz</td>
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<tr>
<td>Reference Spur</td>
<td>-55 dBc</td>
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<tr>
<td>Measured Worst Case Performance with DAC and Calibration Disabled</td>
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<tr>
<td>Phase Noise @ 100 kHz</td>
<td>-88 dBc/Hz</td>
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<tr>
<td>Phase Noise @ 3 MHz</td>
<td>-91 dBc/Hz</td>
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<tr>
<td>Fractional Spur ≤ 3 MHz</td>
<td>-83 dBc</td>
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<tr>
<td>Reference Spur</td>
<td>-52 dBc</td>
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<tr>
<td>Measured Worst Case Performance with DAC and Calibration Enabled</td>
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<tr>
<td>Phase Noise @ 100 kHz</td>
<td>-101 dBc/Hz</td>
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<td>Phase Noise @ 3 MHz</td>
<td>-124 dBc/Hz</td>
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<tr>
<td>Fractional Spur ≤ 3 MHz</td>
<td>-92 dBc</td>
</tr>
<tr>
<td>Reference Spur</td>
<td>-53 dBc</td>
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</tbody>
</table>

Conclusion

• Have presented an adaptive calibration technique that solves the path matching problem in phase-noise cancelling fractional-N PLLs and avoids the slow settling problem

• Have demonstrated the technique in a fractional-N PLL IC, which, compared to relevant prior art, has
  - the lowest reference frequency, $f_{ref}$ (12 MHz)
  - the highest reported BW/$f_{ref}$ (730 kHz/12 MHz)
  - significantly lower calibration settling time