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A Digitally Enhanced 1.8-V 15-b 40-Msample/s CMOS Pipelined ADC

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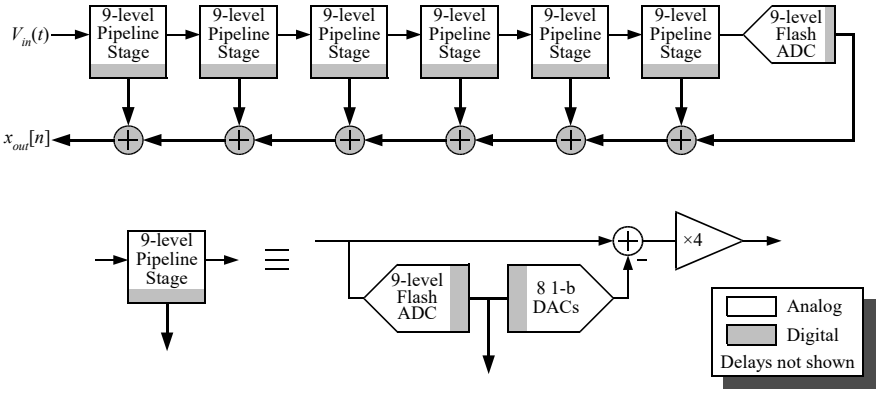
Outline

- Conventional PADC Example
- Digitally Enhanced PADC Prototype
- System-Level Design Details
- Circuit-Level Design Details
- Measured Results
- Conclusion

A Conventional Pipelined ADC Example



- Seven stages
- Each resolves slightly more than 3 bits
- 1-b of redundancy per stage
- Ideal DACs and gains ⇒ accuracy is just over 15b

Conventional Switched Capacitor PADC

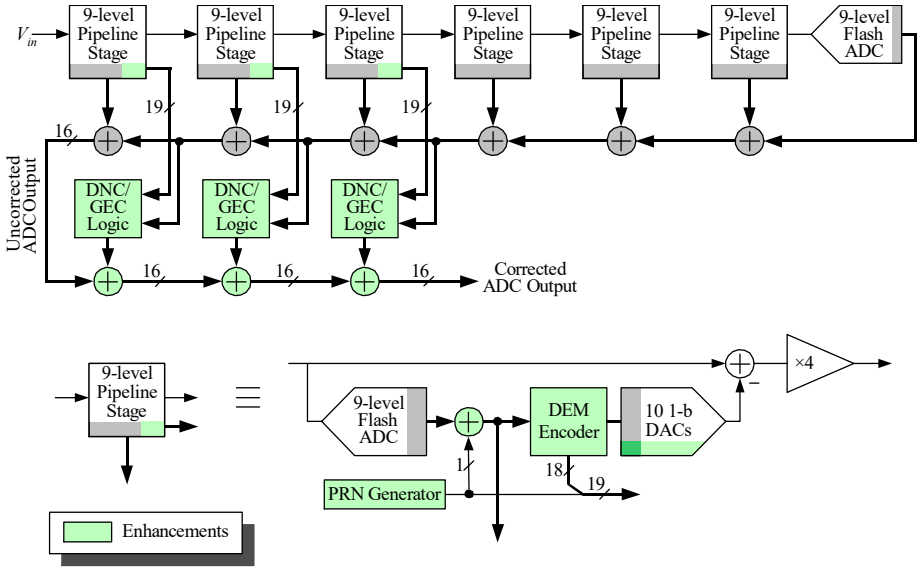
- **Interstage gain error:**
  - *Sources*: capacitor mismatch, finite open-loop amplifier gain, incomplete amplifier settling
  - *Effect*: "leakage" of quantization noise into PADC output
- **DAC Noise:**
  - *Source*: capacitor mismatch
  - *Effect*: introduction of signal-dependent errors
- **Conventional solutions:**
  - Large capacitors, high-gain op-amps
  - Foreground calibration techniques
  - Analog-intensive calibration techniques
  - Trimming

Digitally Enhanced PADC Prototype

- **Analog performance limitations are mitigated by background digital signal processing:**
  - Gain error correction (GEC) [1]
  - DAC noise cancellation (DNC) [2]
  - Segmented mismatch-scrambling DACs [3]
- **Demonstrated in a 0.18 µm CMOS prototype:**
  - 1.8 V, 15 bit, 40 Msamples/s, 400 mW
  - 90 dB SFDR, 72 dB peak SNR, 88 dB THD

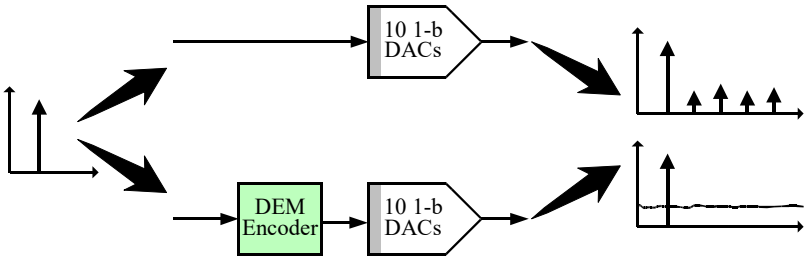
1. E. J. Siragusa, I Galton, *IEE Electronics Letters*, March 30, 2000
2. I. Galton, *IEEE TCAS-II*, March, 2000
3. A. Fishov, E. Siragusa, J. Welz, E. Fogleman, I. Galton, *IEEE ISCAS*, May 2002.

IC Prototype – High-Level Architecture



Dynamic Element Matching Overview

When DAC mismatches are present:

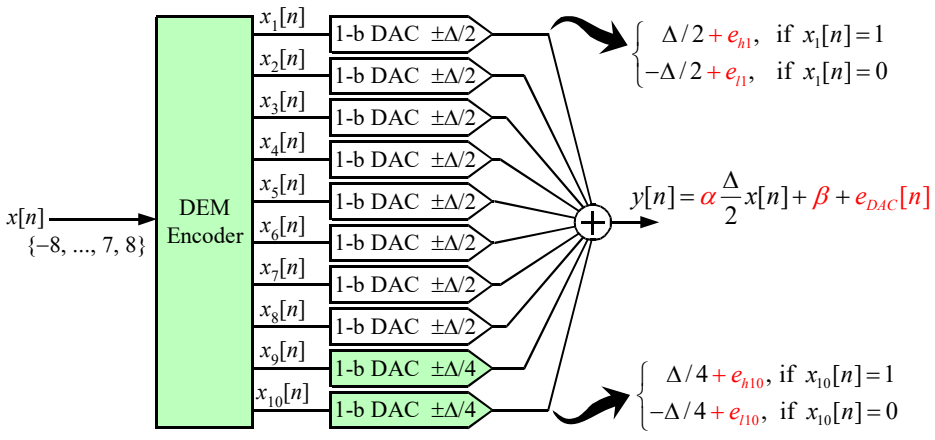


- DEM alone improves SFDR …but not SNDR!

However DEM causes the noise to have "structure":

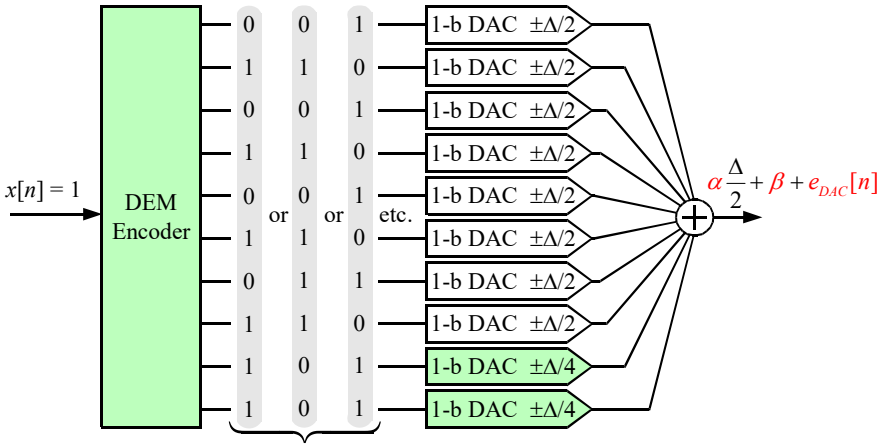
- Noise was "manipulated" with known pseudo-random sequences and digital logic in the encoder
- DNC technique will exploit the structure to remove the noise

Dynamic Element Matching DAC



DEM Encoder uses pseudo-randomization to convert 1-b DAC mismatches, e_{hi} and e_{li}, into a constant gain, α, a constant offset, β, and *white* DAC noise, $e_{DAC}[n]$.

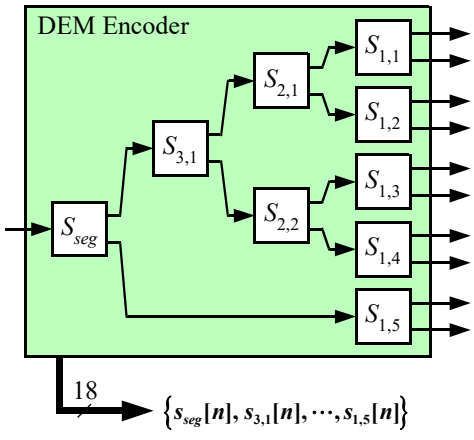
DEM DAC Example for $x[n] = 1$



Chosen pseudo-randomly once per sample period

- α and β are independent of $x[n]$ and pseudo-random choice
- $e_{DAC}[n]$ depends on pseudo-random choice

The DEM Encoder: A Closer Look



where:

$x_{k,r}[n] \rightarrow S_{k,r} \rightarrow \frac{x_{k,r}[n]+s_{k,r}[n]}{2}$, $\frac{x_{k,r}[n]-s_{k,r}[n]}{2}$

and $s_{k,r}[n] = \begin{cases} 0 & \text{if } x_{k,r}[n] = \text{even} \\ \pm 1 & \text{else} \end{cases}$

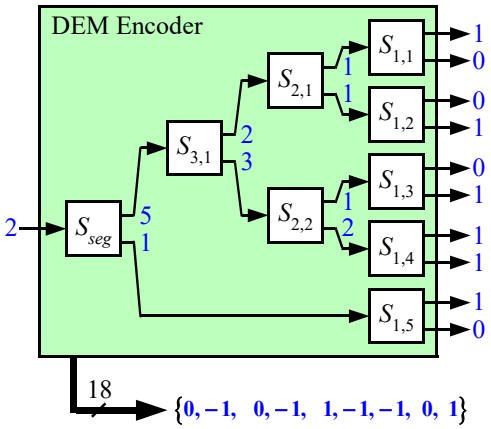
$x_{in}[n] \rightarrow S_{seg} \rightarrow \frac{x_{in}[n]+8+s_{seg}[n]}{2}$, $1-s_{seg}[n]$

and $s_{seg}[n] = \begin{cases} 0 & \text{if } x_{in}[n] = \text{even} \\ \pm 1 & \text{else} \end{cases}$

- $s_{seg}[n]$ and $s_{j,k}[n]$ are independent pseudo-random 0, ±1 sequences
- $s_{seg}[n]$ and $s_{j,k}[n]$ are known by the digital logic

The DEM Encoder: Example

One example set of choices for $x[n] = 2$:



where:

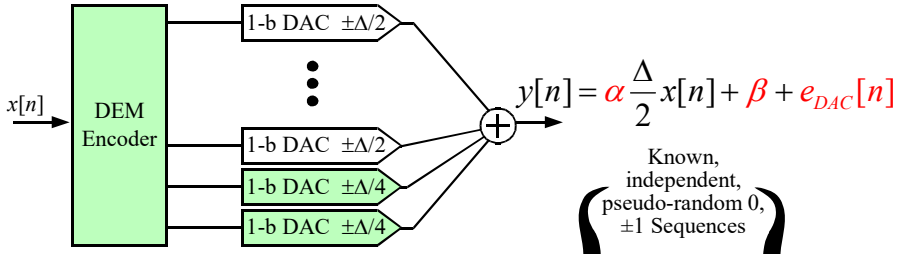
$x_{k,r}[n] \rightarrow S_{k,r} \rightarrow \dfrac{x_{k,r}[n]+s_{k,r}[n]}{2}$, $\dfrac{x_{k,r}[n]-s_{k,r}[n]}{2}$

and $s_{k,r}[n] = \begin{cases} 0 & \text{if } x_{k,r}[n] = \text{even} \\ \pm 1 & \text{else} \end{cases}$

$x_{in}[n] \rightarrow S_{seg} \rightarrow \dfrac{x_{in}[n]+8+s_{seg}[n]}{2}$, $1-s_{seg}[n]$

and $s_{seg}[n] = \begin{cases} 0 & \text{if } x_{in}[n] = \text{even} \\ \pm 1 & \text{else} \end{cases}$

Structure of the DAC Noise



Known, independent, pseudo-random 0, ±1 Sequences

Can Show: $e_{DAC}[n] = \sum_k \sum_r \Delta_{k,r} s_{k,r}[n] + \Delta_{seg} s_{seg}[n]$

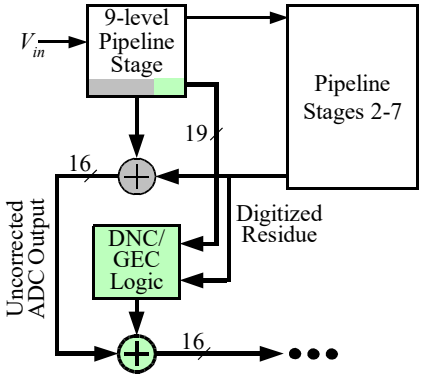
Unknown constants that depend only on the 1-b DAC mismatches

$e_{DAC}[n]$ is like a spread spectrum signal:

- $\Delta_{k,r}$ and Δ_{seg} are the *unknown* (constant) "message signals"
- $s_{k,r}[n]$ and $s_{seg}[n]$ are the *known* "spreading codes"

The DNC Technique

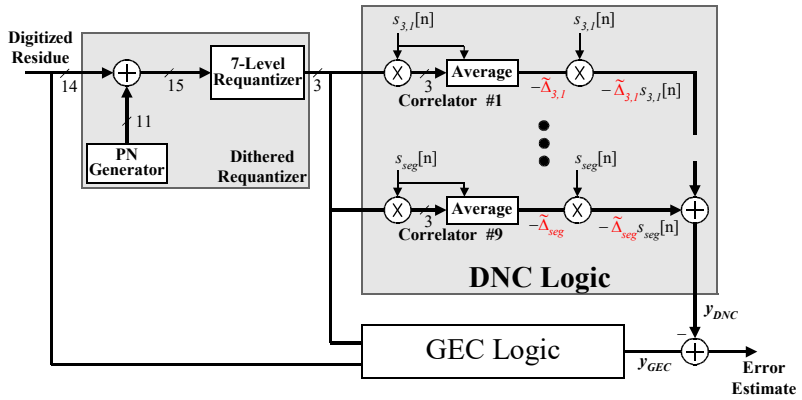
The DAC noise directly corrupts the uncorrected ADC output:



The DNC logic is a spread spectrum "receiver" that:

- correlates the *digitized residue* against $s_{k,r}[n]$ and $s_{seg}[n]$ to estimate $\Delta_{k,r}$ and Δ_{seg}
- uses the DAC noise equation to cancel $e_{DAC}[n]$

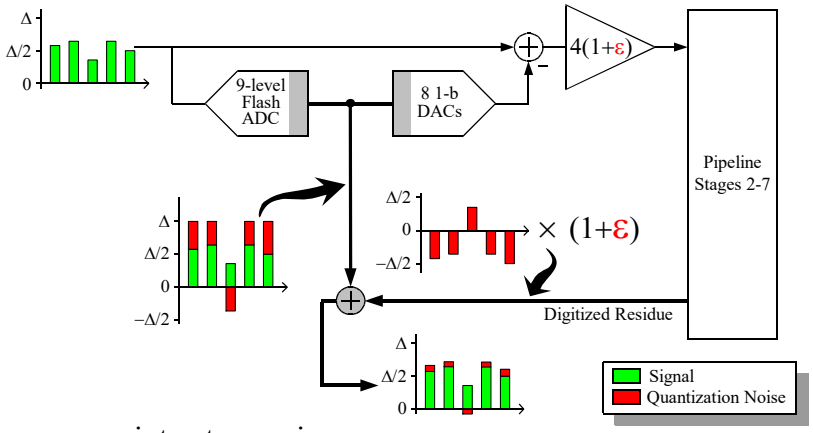
First Stage Calibration Logic - DNC



- 9 simple spread-spectrum "receivers"
- Requantization:
  - reduces DNC logic size
  - dithered to avoid corrupting correlations

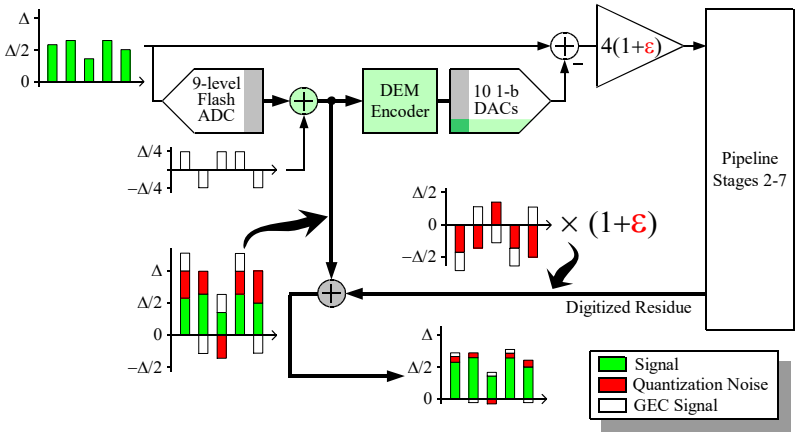
Interstage Gain Error

Conventional PADC:



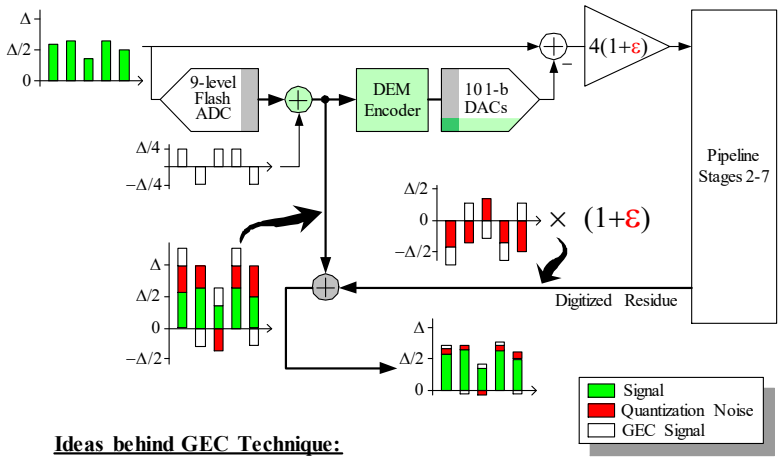
- ε = interstage gain error
- Causes imperfect cancellation of ADC quantization noise
- Reduces SFDR and SNDR

The GEC Technique (1)

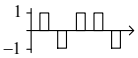


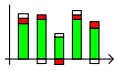
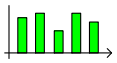
- A pseudo-random ±Δ/4 sequence is introduced to the DAC path
- It occupies a portion of error headroom created by redundancy
- It follows the same path and sees the same gain as the quantization noise

The GEC Technique (2)

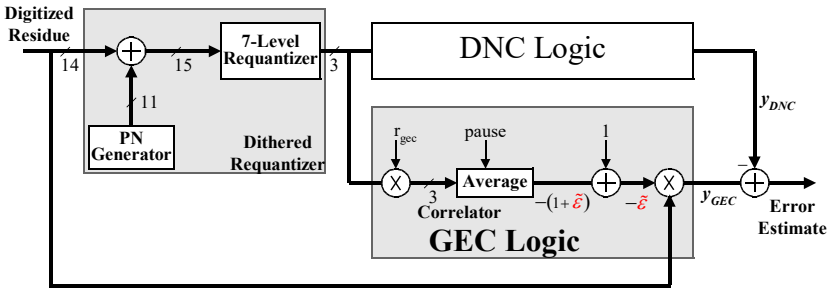


Ideas behind GEC Technique:

Average of:  × (Digitized Residue) ⟶ Correction Factor

 − (Digized Residue) / (Correction Factor) = 

First Stage Calibration Logic -GEC

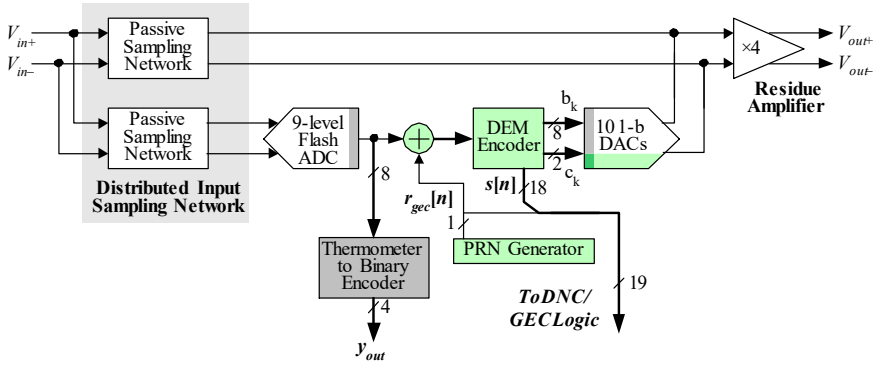


Instead of dividing the digitized residue by the gain estimate:

- a linear Taylor series approximation is used: $\frac{1}{(1+\tilde{\varepsilon})} \approx 1-\tilde{\varepsilon}$
- the resulting correction signal is added directly to output

Any linear contribution to gain error is corrected!

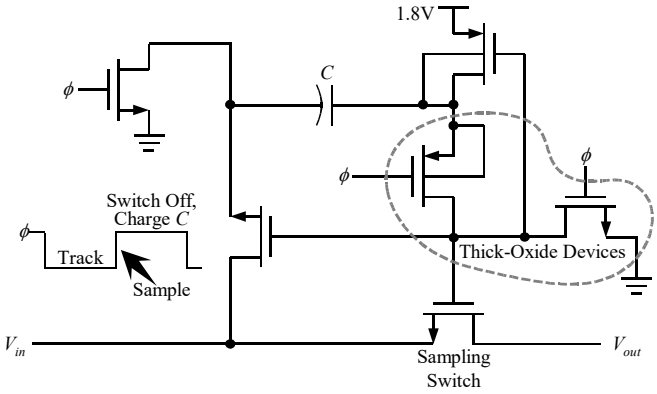
Circuit-Level Details



- Distributed input sampling[4]
- Separate input and DAC sampling capacitors
- DNC&GEC => no special attention to cap matching

4. I. Mehr and L. Singer, *IEEE Journal of Solid State Circuits*, March 2000

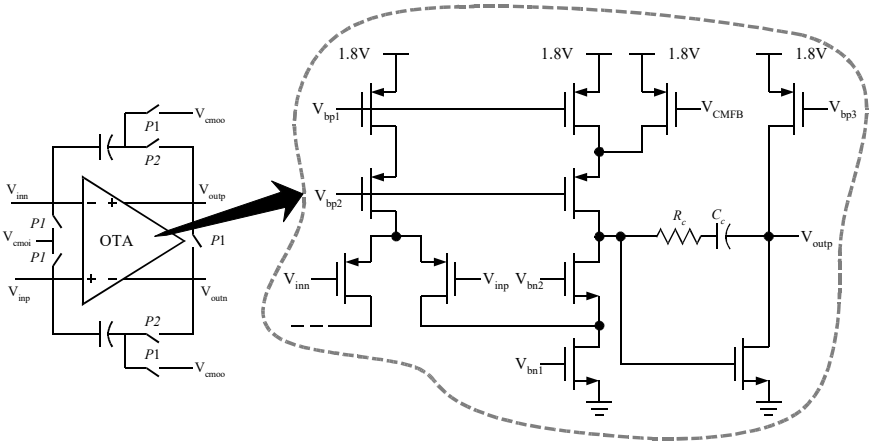
Bootstrapped Switch Circuitry



- **Modified version of circuitry presented in [5]**
  - Thick-oxide devices to avoid exceeding technology limits
- **Uses a single 1.8V clock**

5. M. Dessouky and A. Kaiser, *IEE Electronics Letters*, January 1999

Residue Amplifier (1)



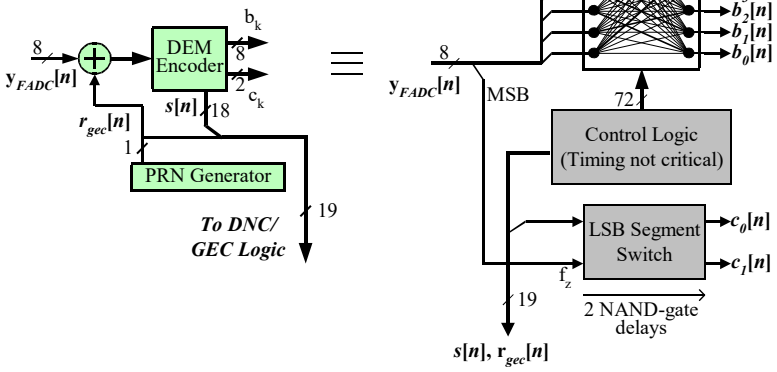
- Closed loop gain of 4
- Two-stages for high gain and wide output swing

Residue Amplifier (2)

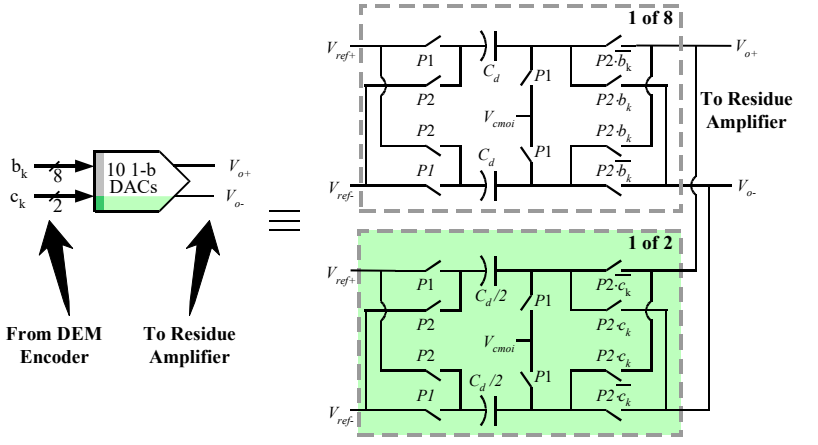
- **Conventional PADC:**
  - Open-loop gain requirement >100dB
  - Gain-boosting is typically required
  - Simulated gain: >125dB with gain-boosting, 85dB without
- **Prototype IC:**
  - Gain-boosting with enable/disable circuitry is included
  - As expected, measured PADC performance with GEC enabled and gain-boosting disabled does not change!
- **Scaled down once and used in the remaining stages without further scaling**

DEM Encoder and GEC Adder Implementation

- Control logic block presets paths
- Critical path is 1 T-gate delay
- Encoder & adder implemented together to minimize latency



DAC Sampling Network

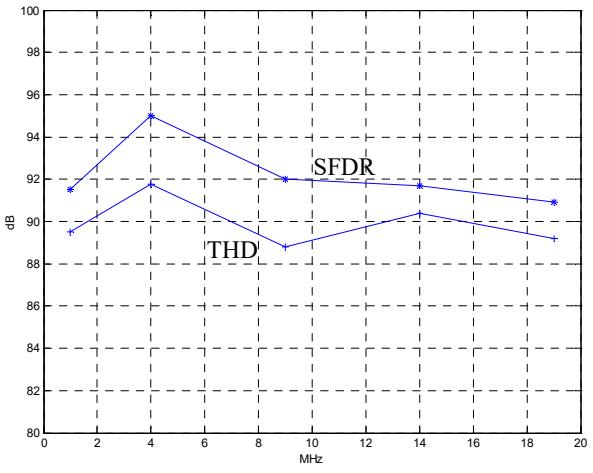


- **10 1-b DACs:**
  - 8 step-size Δ
  - 2 step-size Δ/2
- **References are "double sampled"**
  - Capacitor sizes halved
  - Reduces kT/C noise

Process, Layout and Packaging Overview

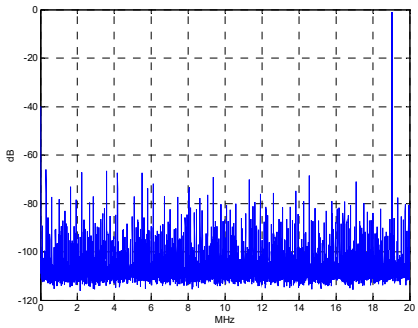
- **Process**
  - 0.18μm CMOS
  - MiM capacitors, deep Nwells, thick-oxide devices, low-V_T devices
- **Layout**
  - Deep Nwells and multiple supply domains
  - No special attention to capacitor matching
  - ESD protection circuitry on all pads
- **Packaging**
  - 56-pin QFN package with exposed die paddle
  - Down-bonding of all grounds to exposed paddle
  - Double-bonding of critical supply pins

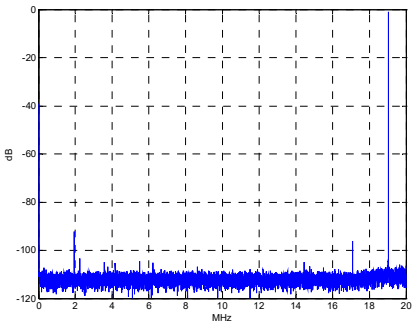
Measured SFDR and THD vs. Input Frequency



- DNC and GEC enabled

Measured PSD with a 19 MHz Input





With DNC and GEC disabled

SFDR 64.8 dB

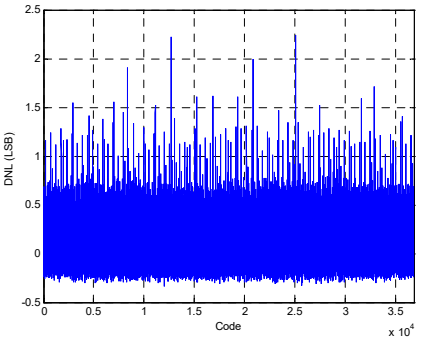
SNDR 54.7 dB

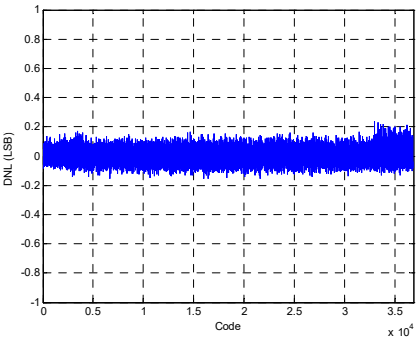
With DNC and GEC enabled

SFDR 90.9 dB

SNDR 71.6 dB

Measured DNL (f_{in} = 1 MHz)





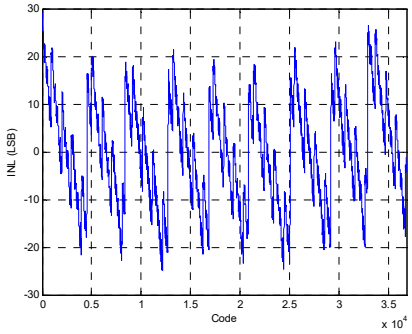
With DNC and GEC disabled

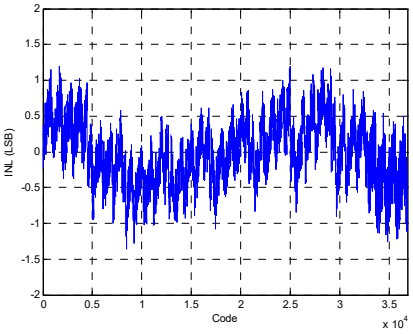
DNL = 2.3 LSB

With DNC and GEC enabled

DNL = 0.25 LSB

Measured INL (f_{in} = 1 MHz)





With DNC and GEC disabled

INL = 25 LSB

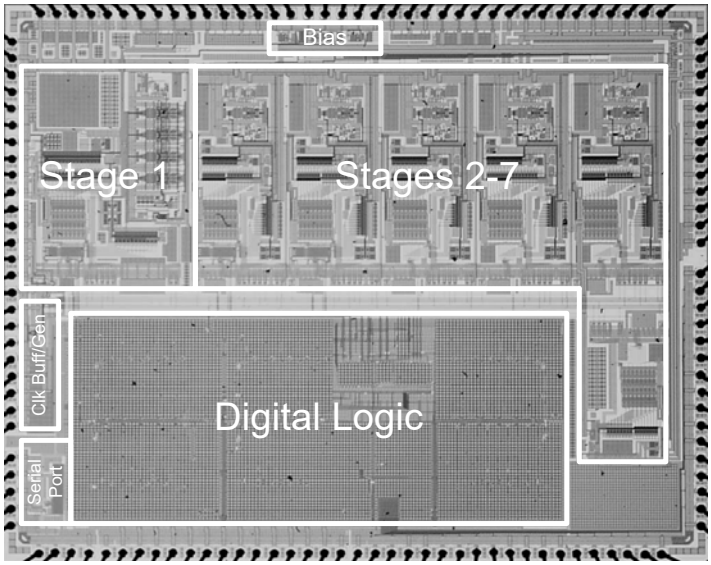
With DNC and GEC enabled

INL = 1.5 LSB

Fabrication and Measurement Summary

Resolution	**15 b**
Sample Rate	**40 MHz**
Input Voltage Range	**2.25 Vp-p differential**
SFDR	**90 dB**
THD	**88 dB**
Peak SNR	**72 dB**
DNL	**0.25 LSB**
INL	**1.5 LSB**
SFDR Improvement with DNC and GEC enabled	**> 20 dB**
SNDR Improvement with DNC and GEC enabled	**> 12 dB**
Total Power	**400 mW**
Analog Power	**343 mW (1.8 V)**
Digital Power	**51 mW (2.1 V)**
Output Drivers Power	**6 mW (1.8 V)**
Technology	**0.18µm 1P6M CMOS**
Die Size	**4mm x 5mm (including pads)**
Package	**56-Pin QFN with ground downbonding**

Die Photo



Conclusion

- The silicon implementation of two digital signal processing background calibration techniques has been presented
  - DNC to compensate for DAC mismatch noise
  - GEC to compensate for interstage gain errors
- Together they drastically reduce analog circuit requirements required to achieve high performance
- They have been shown to be enabling components in a high-resolution pipelined ADC

Acknowledgements

- The authors are grateful to **Erica Poole** for digital schematic capture and verification, **Sudhakar Pamarti** and **Ashok Swaminathan** for digital layout and technical advice, **Eric Fogleman** for technical advice, and **Andrea Panigada** for test board design and technical advice.