Second and Third-Order Successive Requantizers for Spurious Tone Reduction in Low-Noise Fractional-*N* PLLs

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***Abstract*—This paper presents 2nd- and 3rd-order digital requantizers which can be used as drop-in replacements for digital delta-sigma modulators in analog fractional-*N* PLLs to reduce fractional spurs. The requantizers are demonstrated and compared to conventional delta-sigma modulators in a low-noise 3.35 GHz PLL IC and shown to offer significant reductions in worst-case spurious tones with similar phase noise relative to their delta-sigma modulator counterparts.**

Keywords—PLL, phase noise, quantization.

I. Introduction

Analog fractional-*N* phase-locked loops (PLLs) are widely used for RF local oscillator synthesis in high-performance wireless applications. For example, they are in most latest-generation mobile phone handsets. In such applications, fractional spur suppression is a major issue. This paper presents a low-noise PLL IC with best-of-class fractional spur performance enabled by new successive requantizers which replace the commonly-used 2nd- and 3rd-order digital delta-sigma (ΔΣ) modulators. More importantly, the IC demonstrates the successive requantizers and conventional ΔΣ modulators in a single PLL, thereby providing a controlled experimental comparison. The practical tradeoffs among the successive requantizers and ΔΣ modulators for PLL circuit designers are discussed as well.

II. New Digital Requantizers

Every analog fractional-*N* PLL has a digital requantizer, typically a ΔΣ modulator, whose quantization noise spectrum has at least one DC zero. The requantizer's quantization noise, $s[n]$, and its running sum, $t[n] = s[0] + s[1] + \ldots + s[n]$, inevitably are subjected to nonlinearity from the PLL's analog circuitry. This causes the PLL's phase noise to contain terms proportional to $s^p[n]$ and $t^p[n]$ for multiple integer values of p [1–3]. In practical circuits, the magnitudes of these terms decrease with increasing p, and can often be made insignificant for $p > 3$. Unfortunately, $s^p[n]$ and $t^p[n]$ for $p = 2$ and 3 contain spurious tones in ΔΣ modulator-based PLLs for most output frequencies.

This problem was avoided in [3] with a successive requantizer for which $s^p[n]$ and $t^p[n]$ are spur-free for $p = 1, 2, \ldots, 5$ and $p = 1, 2, 3$, respectively. Unfortunately, that successive requantizer has only 1st-order shaped quantization noise with higher power than even that of a 1st-order ΔΣ modulator, so the PLL required both quantization noise cancellation and cancellation path calibration, which incurred significant power and area consumption penalties.

In contrast, the successive requantizers described in this paper can be used as drop-in replacements for 2nd- and 3rd-order ΔΣ modulators in analog PLLs with or without quantization noise cancellation. They offer better spurious tone performance, comparable phase noise from quantization, elimination of low-frequency phase noise from dither, and reduction of short-term quantization noise spectral fluctuations relative to conventional ΔΣ modulators. In exchange for these benefits, they have larger output and $t[n]$ ranges, which increases phase noise from the PLL's charge pump, and higher digital complexity and power dissipation relative to ΔΣ modulators. These tradeoffs are quantified in Table 1 and further explained throughout the paper. The underlying mathematics are presented in [4], so this section focusses on the implementation, tradeoffs, and PLL circuit implications of the successive requantizers.

The new successive requantizers trade off some of the spur immunity achieved in [3] to increase the quantization noise shaping order and to further reduce quantization noise at low and mid frequencies where PLLs are most sensitive. In particular, $s^p[n]$ for the successive requantizers is only spur free for $p = 1$. As demonstrated by this work, this is not problematic because nonlinear distortion of $s[n]$ can be sufficiently mitigated by resynchronizing the frequency divider edges with voltage-controlled oscillator (VCO) edges to nearly eliminate modulus-dependent frequency divider delays.

The implemented PLL and its timing are shown in Figs. 1 and 2, and the successive requantizer details are shown in Fig. 3 and Table 2. Each successive requantizer has input $2^{16}\alpha$, where α is the fractional value to be quantized (restricted here to multiples of 2^{-16}), and quantized output $y[n] = \alpha + s[n]$. It consists of 16 serially-connected digital quantization blocks. The dth quantization block divides its input, $x_d[n]$, by 2 and quantizes the result by one bit. It does so by discarding the LSB of $x_d[n] + s_d[n]$, where $s_d[n]$ is internally generated with the constraint that $x_d[n] + s_d[n]$ is even. Thus, discarding the LSB

978-1-5090-5191-5/17/$31.00@2017 IEEE

TABLE I: SUCCESSIVE REQUANTIZER, ΔΣ MODULATOR COMPARISON TABLE

	2nd-order succ. req.	2nd-order ΔΣ mod.	3rd-order succ. req.	3rd-order ΔΣ mod.
Output range[a]	[–8, 7]	[–2, 1]	[–8, 7]	[–4, 3]
***t*[*n*] range**	[–4, 4)	[–1, 1)	[–4, 4)	[–2, 2)
Low-frequency phase noise from dither	None	$1/f^2$	none	$1/f^2$ or white[b]
Largest measured in-band spur (dBc)	–72	–58	–72	–67.5
Power (μW)	230	45	200	56
Gate count	1500	120	1350	180
Area (μm²)	11,000	1,700	9,700	2,250

a. For a requantizer input range of [–1, 0).

b. The noise is $1/f^2$ or white depending on whether the dither is applied to the ΔΣ modulator's first or second stage, respectively. Applying dither to the first stage results in better fractional spur suppression, but higher low-frequency noise. The prototype IC applies dither to the first stage to minimize fractional spurs.

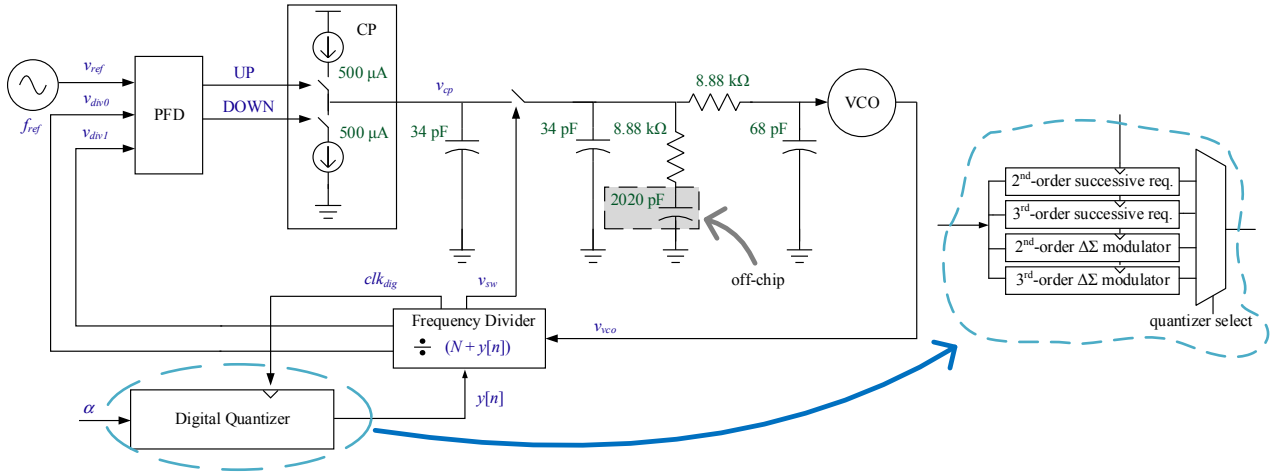

Fig. 1: Block diagram of the PLL.

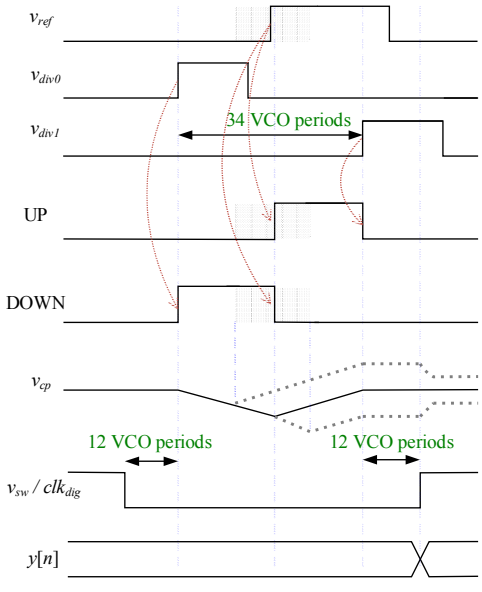

Fig. 2: Timing diagram of the PLL.

is equivalent to division by 2 without additional error, so $s_d[n]$ / 2 is the block's quantization noise. As $s[n]$ is a weighted sum of the $s_d[n]$ sequences, it inherits the $s_d[n]$ properties. The $s_d[n]$ sequence generators therefore determine the properties of the successive requantizer's quantization noise.

The 2nd-order version generates $s_d[n]$ by subjecting a bounded sequence, $u_d[n]$, to two $1 - z^{-1}$ operations. This ensures that $s_d[n]$ is 2nd-order highpass shaped. The combinatorial logic that generates $u_d[n]$ determines the remaining properties of $s_d[n]$. In the 2nd-order case, it is designed such that $t^p[n]$ is spur-free for p = 1, 2, 3. A rigorous mathematical treatment can be found in [4], but the main idea is to allow $t_d[n]$ to assume more levels than would otherwise be necessary and use the extra degrees of freedom to ensure that the mean of $t_d^p[n]$ is not periodic for p = 1, 2, 3. The extra levels increase quantization noise, but the combinatorial logic block was designed with a low-frequency minimization algorithm to push most of the extra quantization noise to high frequencies, where it is attenuated by the PLL loop filter.

The 3rd-order $s_d[n]$ sequence generator differs in that its combinatorial logic block's output is passed through three $1 - z^{-1}$ operations to achieve 3rd-order highpass shaping. While it is such that $t^p[n]$ is only spur-free for p = 1, it was found that $t^2[n]$ and $t^3[n]$ have only very low fractional spurs. Therefore, the emphasis of the design was to minimize quantization noise using a minimization algorithm similar to that of the 2nd-order case. Fig. 4 compares the quantization noise phase noise

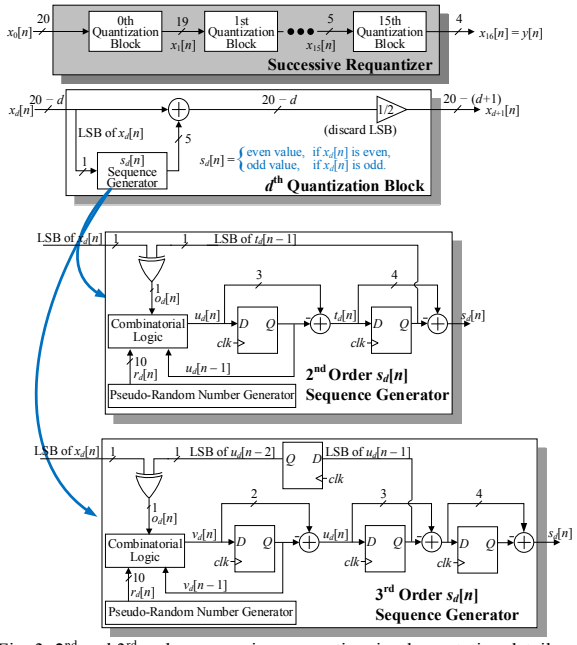

Fig. 3: 2nd and 3rd-order successive requantizer implementation details.

TABLE II: SEQUENCE GENERATOR COMBINATORIAL LOGIC TRUTH TABLES

2nd Order $s_d[n]$ Sequence Generator

$o_d[n] = 0$			$o_d[n] = 1$		
$u_d[n-1]$	$r_d[n]$	$u_d[n]$	$u_d[n-1]$	$r_d[n]$	$u_d[n]$
−2	≥ −512 and ≤ 153	0	−2	≥ 0 and ≤ 6	−1
−2	≥ 154	2	−2	≤ −1 or ≥ 7	1
−1	≥ 0 and ≤ 55	−1	−1	−512 or −511	−2
−1	≤ −1 or ≥ 56	1	−1	≥ −510 and ≤ 155	0
0	≥ 0 and ≤ 178	−2	0	≥ 156	2
0	≤ −1 or ≥ 358	0	0	≥ 0	−1
0	≥ 179 and ≤ 357	2	0	≤ −1	1
1	≤ −1 or ≥ 56	−1	1	≥ 156	−2
1	≥ 0 and ≤ 55	1	1	≥ −510 and ≤ 155	0
2	≥ 154	−2	2	−512 or −511	2
2	≥ −512 and ≤ 153	0	2	≤ −1 or ≥ 7	−1

3rd Order $s_d[n]$ Sequence Generator

$o_d[n] = 0$			$o_d[n] = 1$		
$u_d[n-1]$	$r_d[n]$	$u_d[n]$	$u_d[n-1]$	$r_d[n]$	$u_d[n]$
−1	= 0	−1	−1	X	0
−1	≠ 0	1	0	<0	−1
0	X	0	0	≥0	1
1	≠ 0	−1	1	X	0
1	= 0	1			

contribution of the successive requantizers with the ΔΣ modulators. LSB dither of weight 2^{-20} is used in the 2nd-order ΔΣ modulator. The dither in the 3rd-order ΔΣ modulator can be applied on the 1st or 2nd stage. In the figure, dither of weight 2^{-20} is used when applied on the 1st stage and weight 2^{-12} when applied on the 2nd stage. The IC applies dither on the 1st stage, as this results in better spurious tone performance.

The built-in randomization in both successive requantizers has the added benefit of avoiding the side effects of dither that occur in ΔΣ modulators. LSB 1-bit dither is used in ΔΣ modulators to cause the quantization noise prior to shaping to be asymptotically white. This ensures that $s^p[n]$ and $t^p[n]$ are spur-free for $p = 1$, but contributes significant low-frequency noise (Fig. 4). Reducing the dither power reduces this noise, but enhances short-term quantization noise spectral fluctuations resulting from the quantization noise being only asymptotically white. This is shown in Fig. 5, where LSB dither of weight 2^{-20} is used in the 2nd–order ΔΣ modulator. The PSD of the quantization noise phase noise contribution of the 2nd–order ΔΣ modulator is estimated with 100 averaged periodograms of length 256 to illustrate the short-term spectral fluctuations due to the ΔΣ modulator quantization error being only asymptotically white. The 2nd–order successive requantizer quantization noise phase noise contribution is estimated as well for comparison. PSDs capture spectral averages, so they potentially miss short-term fluctuations like those in the figure.

III. MEASUREMENTS

Measured phase noise and worst-case fractional spur sweeps (Fig. 6) and comparison to relevant prior papers that report worst-case (in-band) fractional spur sweeps (Table 3) verify the expected benefits of the successive requantizers relative to ΔΣ modulators. The worst-case fractional spurs for the two

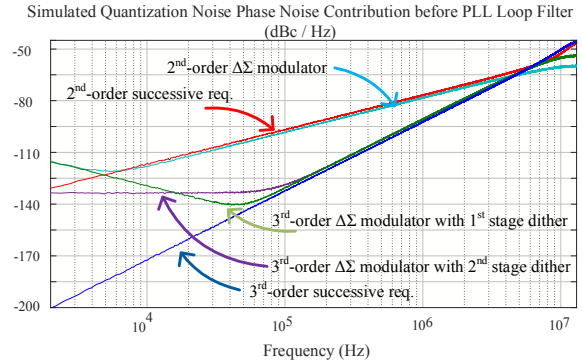

Fig. 4: Simulated quantization noise phase noise PSD contribution of the 2nd- and 3rd-order requantizers.

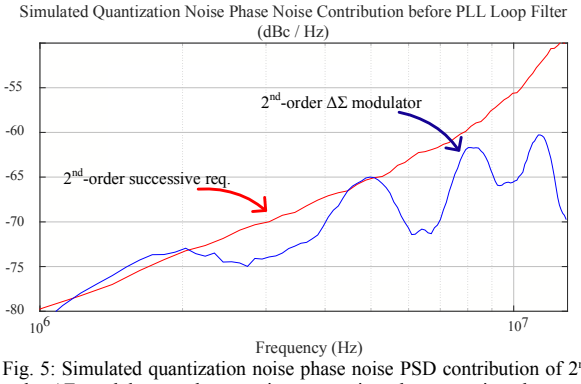

Fig. 5: Simulated quantization noise phase noise PSD contribution of 2nd-order ΔΣ modulator and successive requantizer demonstrating short-term quantization noise spectral fluctuations.

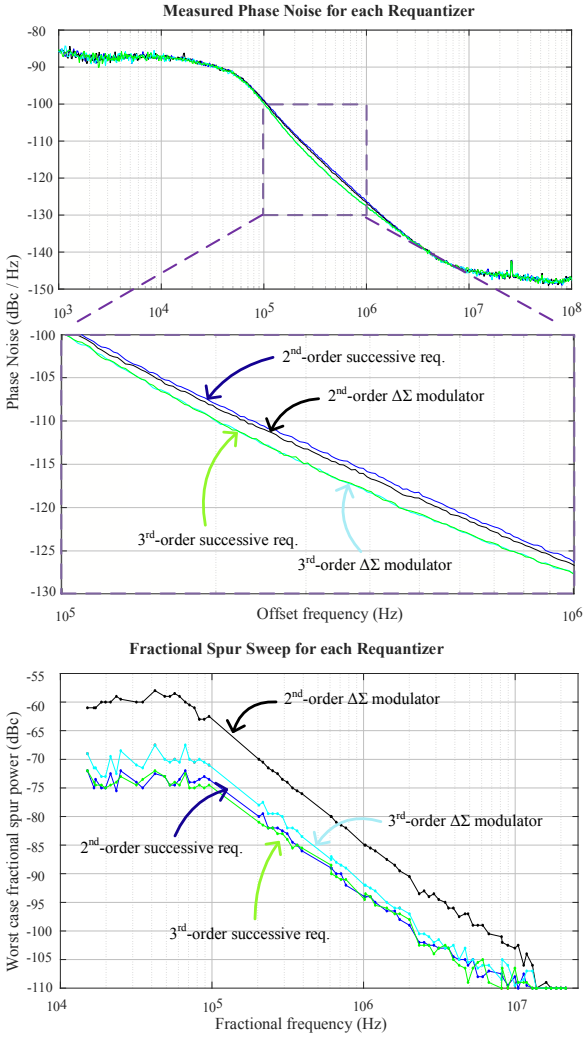

Fig. 6: Measured PLL phase noise and spur sweep. Due to a mistake in the IC serial port interface, most, but not all, of the desired fractional frequencies were able to be programmed.

successive requantizers are very similar and higher than predicted by simulation, e.g., by 8 dB for the 2nd-order successive requantizer case. This suggests that they are limited by a mechanism other than nonlinear distortion of $t[n]$, most likely parasitic coupling of signals aligned with reference and VCO edges. Hence, a design with less parasitic coupling would likely see even lower fractional spurs. The phase noise results are consistent with the simulated results of Fig. 4 and the expected noise performance of the PLL's analog blocks. Overall the best-of-class spurious tone results with low quantization noise demonstrate the viability of the successive requantizers as drop-in replacements for their conventional ΔΣ modulator counterparts in analog fractional-*N* PLLs.

ACKNOWLEDGMENTS

The authors are grateful to STMicroelectronics for IC fabrication and to Kevin Rivas, Julian Puscar, and Colin Weltin-Wu for design support and helpful discussions. The authors are also grateful for support of this work provided by the National Science Foundation under Award 1343389, by Analog Devices, and by corporate members of the UCSD Center for Wireless Communications.

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TABLE III: PERFORMANCE SUMMARY AND COMPARISON

	[3]	[5]	[6]	**This work**
Technology (nm)	180	180	40	65
Supply (V)	1.2	1.8	1.0 / 2.0	1.0 / 1.2
Power Consumption (mW)	66.42	46.8	9.1	19.52
Area (mm^2)	4.84	3.24	0.046	0.341
Reference Frequency (MHz)	12	38	26	26
PLL Frequency (GHz)	2.4	6.12	2.002	3.35
Bandwidth (kHz)	975	1000	1500	48[a]
In-band Phase Noise (dBc/Hz)	–98 @100kHz	–102 @300 kHz	–91 @5kHz	–87.5 @10kHz
Out-of-band Phase Noise (dBc/Hz)	- –121 @3MHz -	- –130 @3MHz -	- –105 @3MHz –115 @10MHz	–126 @1MHz –137 @3MHz –145 @10MHz
Largest Fractional Spur (dBc)	–64	–61	–70	–72
Reference Spur (dBc)	–70	–78	–87	–79

[a] This bandwidth was chosen to optimize phase noise for the 2nd-order ΔΣ modulator and was used for all measurements to facilitate a controlled comparison. The bandwidth could be widened considerably without a phase noise penalty for the 3rd-order requantizers and, if quantization noise cancellation is used as in [3], for the 2nd-order requantizers.