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Second and Third-Order Successive Requantizers for Spurious Tone Reduction in Low-Noise Fractional-*N* PLLs

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INTEGRATED SIGNAL PROCESSING GROUP

Outline

- Fractional-*N* PLL background
- ΔΣ modulator nonlinearity-induced fractional spurs
- A fundamental spur reduction limitation in digital quantizers
- Spur-mitigating 2nd and 3rd-order ΔΣ modulator replacements
- A technique to linearize charge pump response
- PLL implementation
- IC measurements

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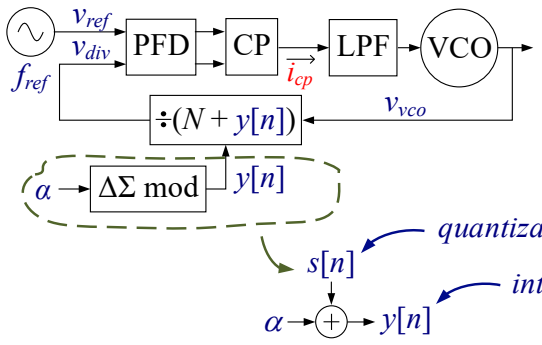
Conventional Fractional-*N* PLL



$f_{PLL} = (N+\alpha)f_{ref}$

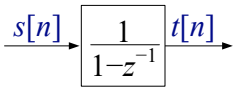
N: integer

$|\alpha| < 1$

- $v_{vco} = \sin(2\pi f_{PLL} t + \theta_{PLL}(t))$

  phase error

- Quantization noise and its *running sum* $t[n]$ contribute phase noise and spurs to $\theta_{PLL}(t)$



  - If frequency divider is resynchronized to VCO edges:
    only $t[n]$ contributes phase noise and spurs

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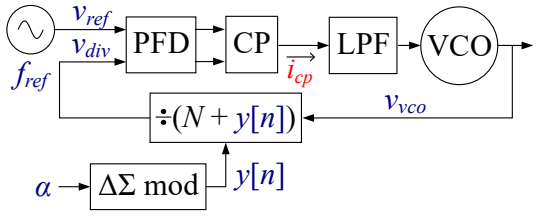
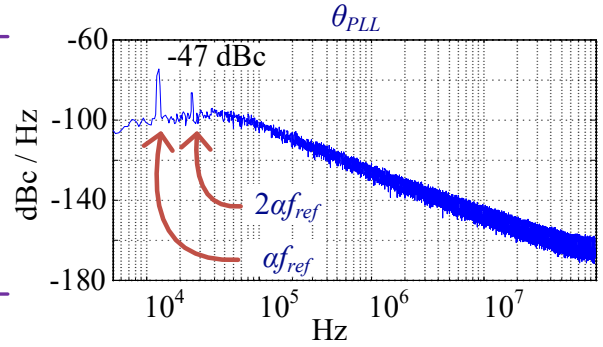
Fractional Spurs from PLL Nonlinearities



$\sin(2\pi f_{PLL} t + \theta_{PLL}(t))$

PLL nonlinearities
$\Rightarrow$ spurs

Example: PLL with
2nd-order $\Delta\Sigma$ mod,
1% CP mismatch



- Spurs arise from nonlinear distortion of $t[n]$:
  phase error contains terms with $t^2[n]$, $t^3[n]$, …

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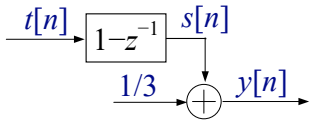
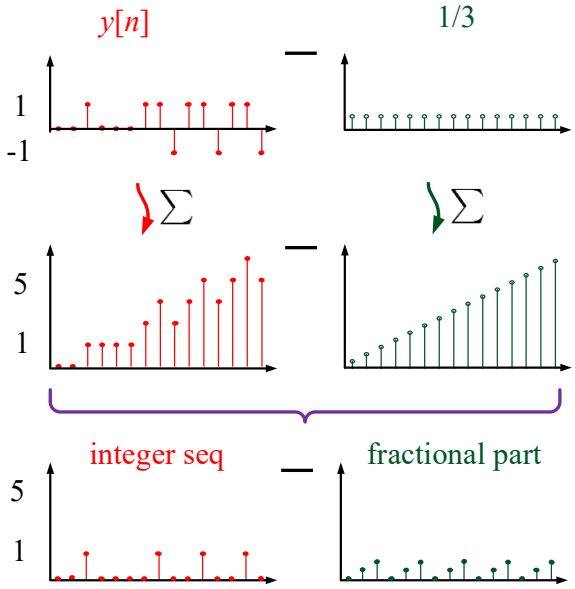
Building A Quantizer With Spur-Free $t[n]$, $t^2[n]$



$s[n]$ { DC-free
$= y[n] - 1/3$

$\Rightarrow$

$t[n]$ { Bounded
= integer seq – fractional part



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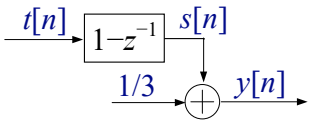
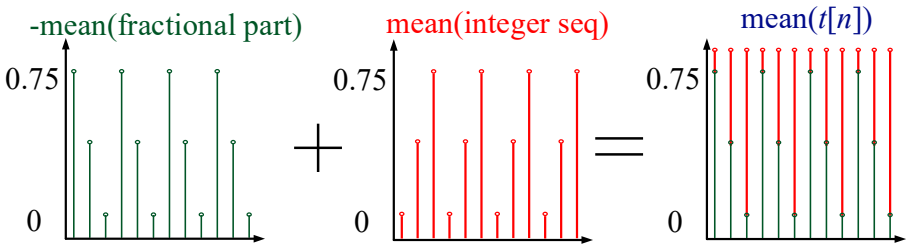
Making $t[n]$ Spur-Free



$s[n]$ { DC-free
$= y[n] - 1/3$
$\Rightarrow$ $t[n]$ { Bounded. Choose $|t[n]| \le 1$
= integer seq – fractional part

spur-free $t[n]$ $\Leftrightarrow$ *mean* of $t[n]$ is constant

Can come up with a probability distribution for $t[n]$ that makes the mean of $t[n]$ constant at each n



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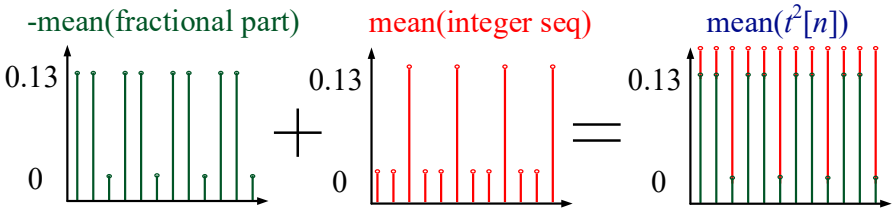
Making $t^2[n]$ Spur-Free

- We also want the probability distribution of $t[n]$ to make the mean of $t^2[n]$ constant at each n
  - $t^2[n]$ = integer seq – fractional part



- But with $|t[n]| \le 1$, there are not enough degrees of freedom to make the means of both $t[n]$ and $t^2[n]$ constant!
- Can get more flexibility if $t[n]$ is bounded by 2 instead of 1
  - Can make means of $t[n]$, $t^2[n]$ constant $\Rightarrow$ $t[n]$, $t^2[n]$ are spur-free
  - But quantization noise increases

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A Fundamental Limitation of Digital Quantizers

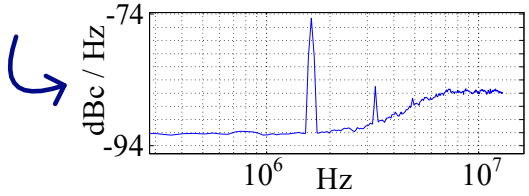
- Previous result is general:

  if $|t[n]|$ is always $\le K$ **at least one of $t[n]$, $t^2[n]$, … $t^{2K}[n]$ has spurs**

  - True for *any* digital quantizer

    [Familier, Galton, *IEEE Trans. Signal Processing*, May 2013]
- In dithered 2nd-order ΔΣ modulator $|t[n]| \le 1$

  $\Rightarrow$ $t^2[n]$ always has spurs!



- Can design a new digital quantizer with a larger $t[n]$ range to

  improve frac spur performance ☺

  but will get higher quant noise power ☹

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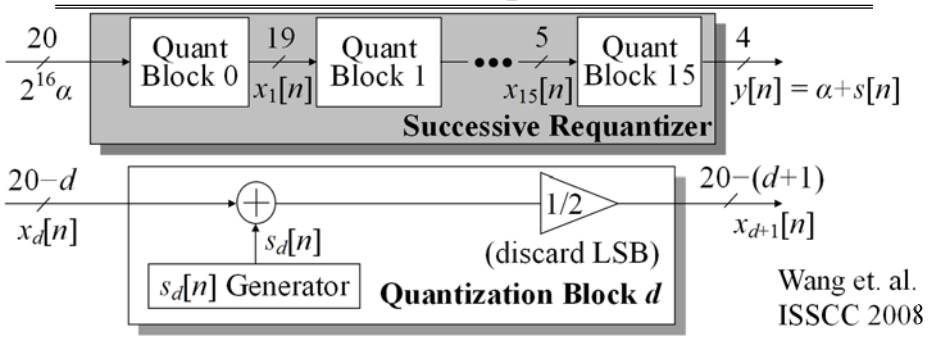
A ΔΣ Mod Replacement



- Successive requantizer (SR) quantizes input: $2^{16}\alpha$ one bit at a time
  - Quantization block adds $s_d[n]$ to input and divides result by 2
- Quant noise is a weighted sum of $s_d[n]$ seqs
- Quant noise running sum is a weighted sum of $t_d[n]$ seqs

$s_d[n] \rightarrow \boxed{\frac{1}{1-z^{-1}}} \rightarrow t_d[n]$

$s_d[n]$ seqs are *designed* to have desired quant noise properties

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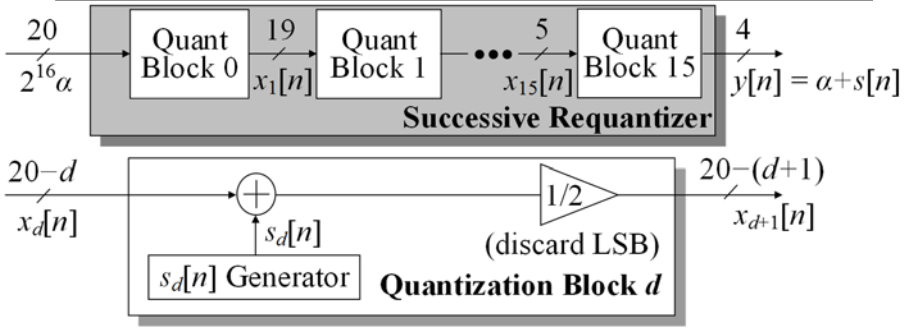
New Successive Requantizers



- Previously: $s[n]$, … $s^5[n]$ and $t[n]$, $t^2[n]$, $t^3[n]$ are spur-free
  - $s[n]$ is high-power 1st-order shaped noise
  - ⇒ PLL needs calibrated quant noise cancellation (QNC)
- This work: two successive requantizers with low-power $s[n]$
  - 2nd-order shaped $s[n]$ with spur-free $s[n]$, $t[n]$, $t^2[n]$ and $t^3[n]$
  - 3rd-order shaped $s[n]$ with spur-free $s[n]$ and $t[n]$
  - ⇒ great frac spur performance and no QNC needed

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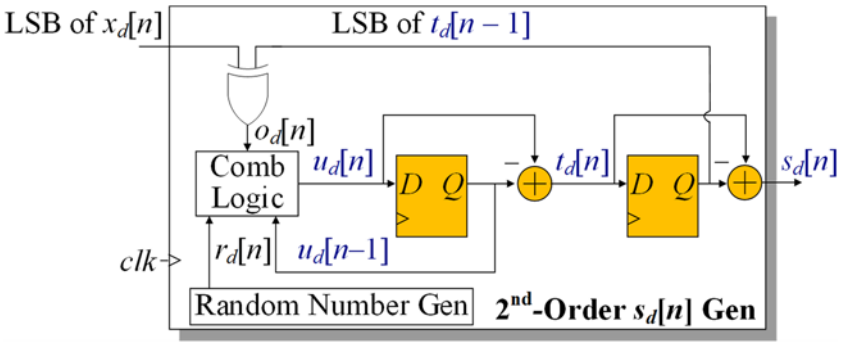
2nd-Order $s_d[n]$ Generator



- Combinatorial logic generates $u_d[n]$ $\quad |u_d[n]| \le 2$
- $u_d[n]$ goes through two $1-z^{-1}$ operations
  $\Rightarrow s_d[n]$ is 2nd-order shaped
- $u_d[n]$ generated so $x_d[n]+s_d[n]$ is even

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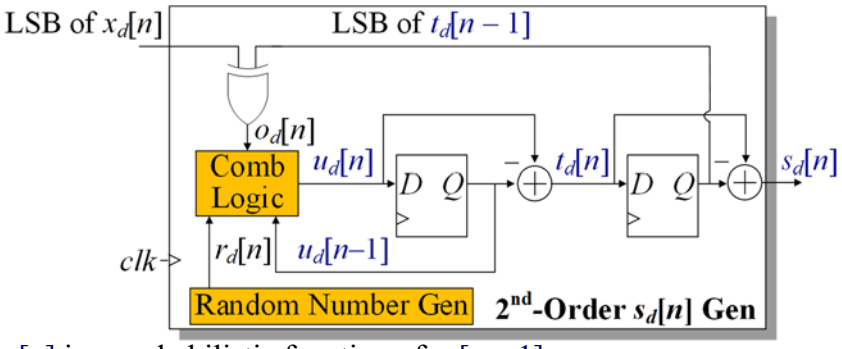
2nd-Order $s_d[n]$ Generator



- $u_d[n]$ is a probabilistic function of $u_d[n-1]$
- Probabilities encoded in combinatorial logic
  - Chosen so means of $t_d[n]$, $t_d^2[n]$, $t_d^3[n]$ are not periodic
    $\Rightarrow$ spur-free $t[n]$, $t^2[n]$, and $t^3[n]$
- Could have made $t^4[n]$ and $t^5[n]$ spur-free, but instead optimized to push quant noise to high frequencies
  $\Rightarrow$ quant phase noise contribution is similar to $\Delta\Sigma$ modulator

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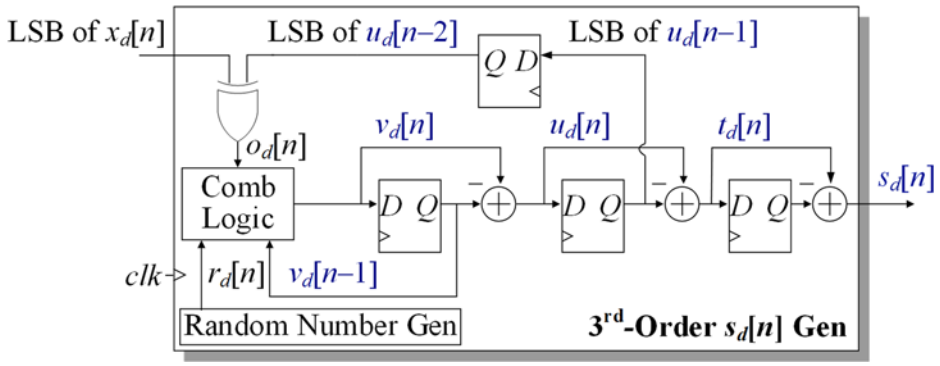
3rd-Order $s_d[n]$ Generator



- Combinatorial logic output $v_d[n]$ goes through three $1-z^{-1}$ operations
  $\Rightarrow s_d[n]$ is 3rd-order shaped
- Only $t[n]$ and $s[n]$ are spur-free
  but spurs in $t^2[n]$ and $t^3[n]$ are low
- Quant noise pushed to high frequencies like in 2nd-order case

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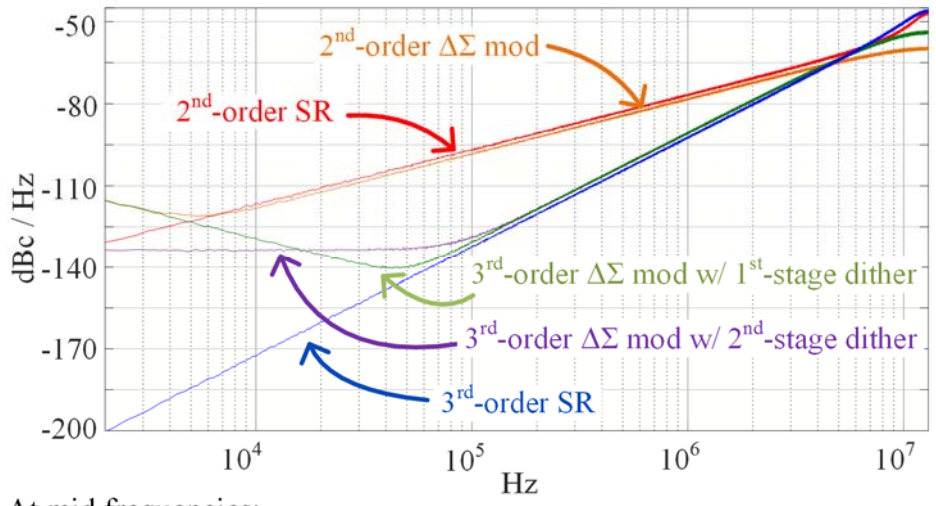
Quant Noise Phase Noise before LPF Attenuation



At mid frequencies:

2nd-order SR noise is 1.5 dB higher than 2nd-order ΔΣ mod

3rd-order SR noise is 1.5 dB lower than 3rd-order ΔΣ mod

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Successive Requantizer vs ΔΣ Modulator

- Better frac spur performance
  - 15 dB spur difference between 2nd-order ΔΣ mod and SRs
  - 3-5 dB spur difference between 3rd-order ΔΣ mod and SRs
- No dither

  ⇒ Improved low-frequency phase noise
- No short-term quant noise spectral fluctuations
- Higher phase noise at high frequencies
  - Not an issue if LPF attenuates noise
- Larger number of output and quant noise levels
  - Higher CP phase noise

- SR could be optimized for even better frac spur performance, but at the expense of quant noise power. Instead:

  improve frac spur performance by linearizing CP response

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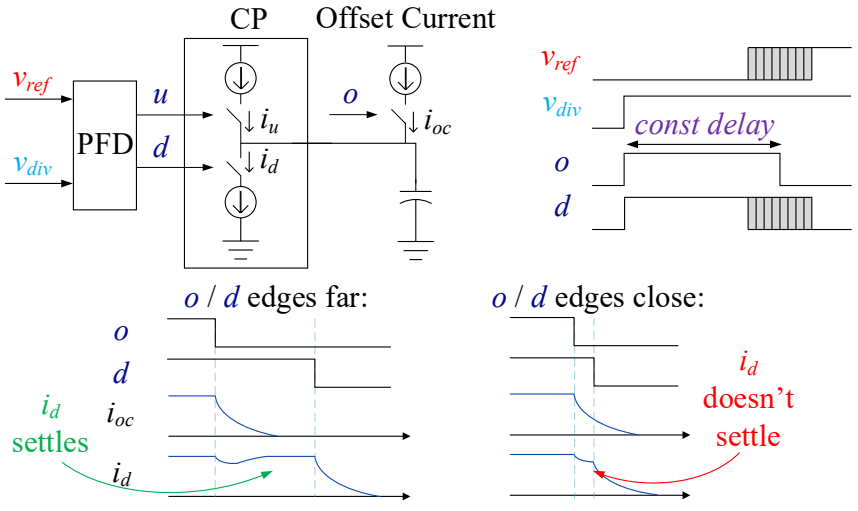
Charge Pump Nonlinearity

- Frac spurs can occur from mixing of ref and VCO-aligned signals
  - PLL should lock at a *phase offset* to let PFD disturbances settle

[Wang et. al. ISSCC 2008]:



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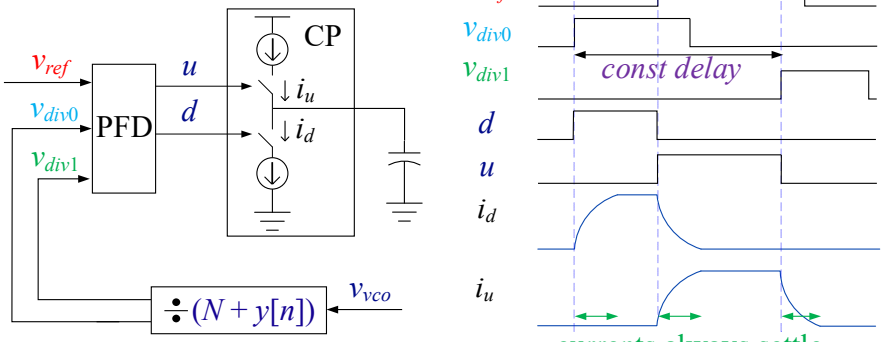
Charge Pump Linearization

- This work: PLL timing modified to let CP currents settle
  - Divider has 2 outputs separated by constant delay
  - PLL locked ⇒ v_{ref} edge falls between v_{div0} and v_{div1} edges
  - d is high from v_{div0} to v_{ref} edges
  - u is high from v_{ref} to v_{div1} edges



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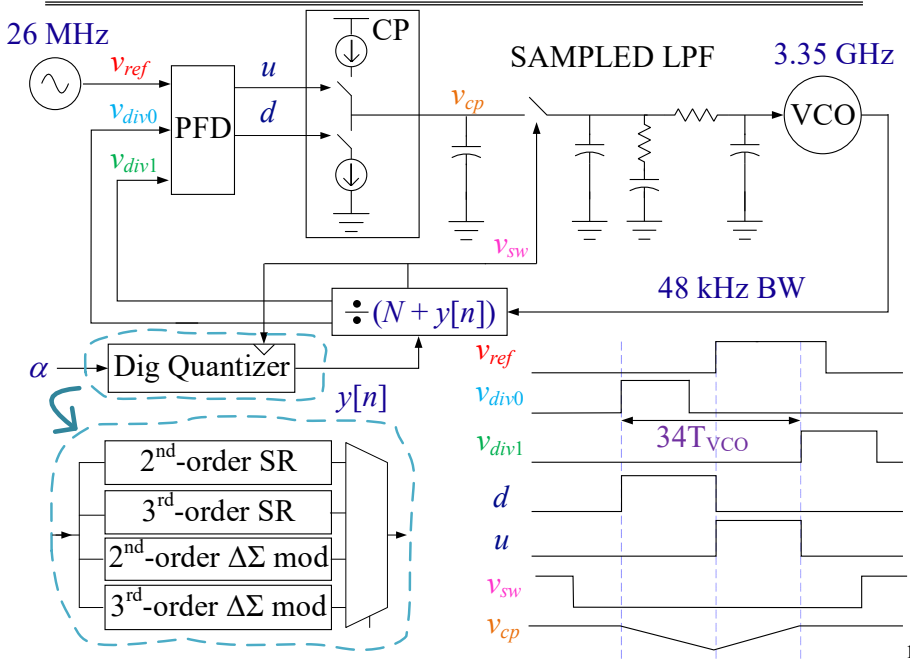
PLL Implementation



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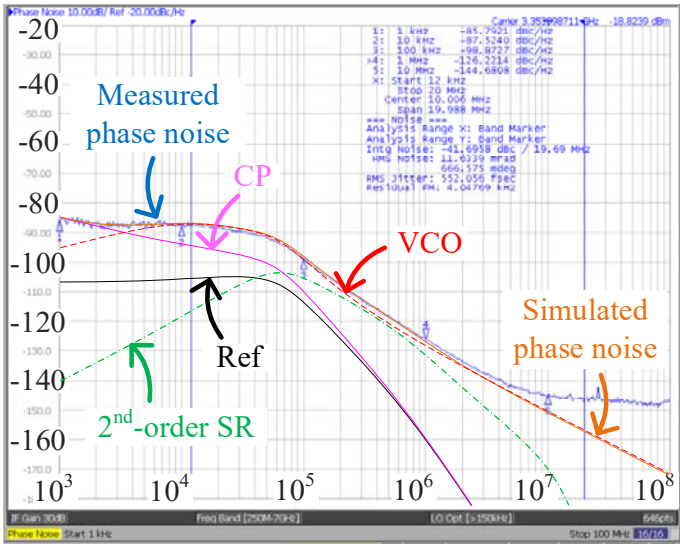
Measured Phase Noise With 2nd-Order SR



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Measured Phase Noise With Each Quantizer

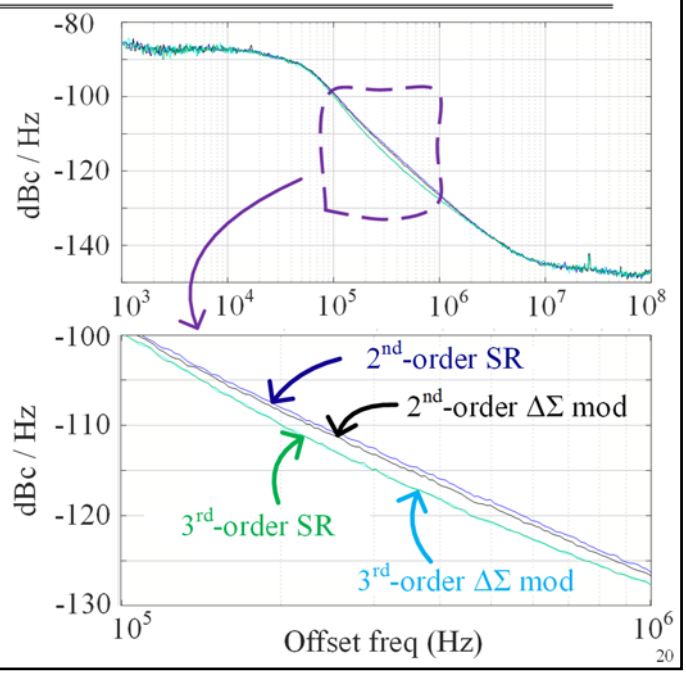
2nd-order SR

↕ 0.8 dB

2nd-order ΔΣ mod

↕ 2 dB

3rd-order quantizers



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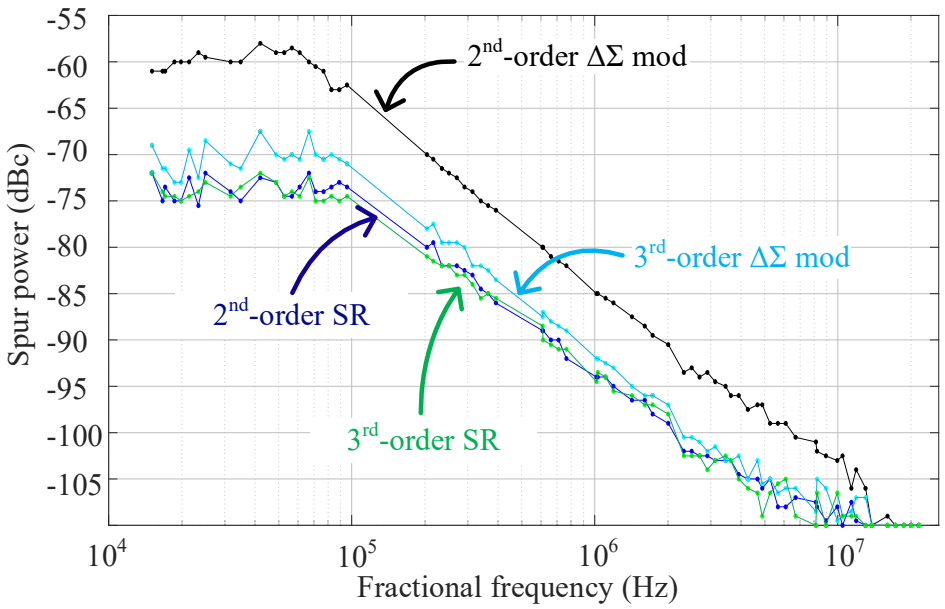
Measured Worst-Case Fractional Spur



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Performance Summary

	[3]	[5]	[6]	This work
Tech (nm)	180	180	40	65
Supply (V)	1.2	1.8	1.0 / 2.0	1.0 / 1.2
Power (mW)	66.42	46.8	9.1	19.52
Area (mm^2)	4.84	3.24	0.046	0.341
Ref freq (MHz)	12	38	26	26
PLL freq (GHz)	2.4	6.12	2.002	3.35
BW (kHz)	975	1000	1500	48[a]
In-band phase noise (dBc/Hz)	–98 @100kHz	–102 @300 kHz	–91 @5kHz	–87.5 @10kHz
Out-of-band phase noise (dBc/Hz)	- -121@3MHz -	- -130@3MHz -	- -105@3MHz -115@10MHz	-126@1MHz -137@3MHz -145@10MHz
Frac spur (dBc)	–64	–61	–70	–72
Ref spur (dBc)	–70	–78	–87	–79

[a] BW chosen to optimize phase noise for 2nd-order ΔΣ mod

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Conclusion

- Presented 2nd and 3rd-order successive requantizers as ΔΣ modulator replacements for fractional spur reduction in PLLs
- Demonstrated performance in an IC PLL
  - PLL linearizes charge pump response with timing technique
  - PLL has lowest in-band fractional spurs to date

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