UNIVERSITY OF CALIFORNIA, SAN DIEGO

Enabling Techniques for Low Power, High Performance Fractional-*N* Frequency Synthesizers

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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To Mom, Dad, and Deeps.

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ABSTRACT OF THE DISSERTATION

Enabling Techniques for Low Power, High Performance Fractional-*N* Frequency Synthesizers

by

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Delta-sigma fractional-*N* phase-locked loops are used to generate high quality radio-frequency signals for use in wireless applications. To reduce the phase noise inherent to these systems, a digital-to-analog converter is used to cancel the error introduced by the fractional division process, however matching between the digital-to-analog converter and the phase-locked loop circuitry place a limit on the amount of phase noise reduction that can be achieved. Furthermore, circuit non-linearity results

in the appearance of spurious tones in the phase-locked loop output.

This dissertation outlines a calibration technique, and a digital quantization technique that provide solutions to these two problems. The calibration technique results in improved phase noise performance by adjusting the digital-to-analog converter gain, and thus providing better matching between the phase-locked loop circuitry and digital-to-analog converter. The digital quantization technique results in no spurious tones when specified non-linearity is applied to the quantizer output sequence and error. The calibration technique was implemented in an integrated circuit, which achieves state-of-the-art performance when compared to currently published phase-locked loops and allows for all circuitry to be integrated onto a single chip. Chapter 1 presents the calibration technique, as well as a theoretical analysis of the stability. Chapter 2 presents details on the digital quantization technique, and a mathematical proof of the absence of spurious tones. In chapter 3, results from an implemented circuit are presented, which verify the behaviour of the technique presented in chapter 1.

Chapter 1 : A Calibration Technique for Phase Noise Canceling Fractional-N Phase-Locked Loops

ABSTRACT

Phase-noise canceling phase-locked loops (PLL) are sensitive to the matching between the phase noise canceling and PLL circuitry. Any mismatch places a limit on the quality of the phase noise cancellation, and as a result constrains the design of the PLL to accommodate the mismatch. This paper presents a calibration technique which estimates the mismatch, and adjusts the equivalent gain of the phase noise canceling circuitry to improve the degree of phase noise cancellation, thus allowing for more PLL design choices, such as widening the PLL loop bandwidth. The presented technique offers faster settling time over current solutions, which in turn enables its use in low power wireless systems.

I. INTRODUCTION

Delta-Sigma Fractional-*N* Phase-Locked Loops (PLL) are widely used in applications requiring the generation of a periodic signal with fine frequency tuning [1], however noise from the delta-sigma modulator degrades the phase noise performance of the PLL. This requires the bandwidth to be sufficiently narrow in order to attenuate the phase noise to acceptable limits dictated by the PLL requirements. A recent enhancement to delta-sigma fractional-*N* PLLs is the use of a Digital-to-Analog Converter (DAC) to reduce the phase noise induced by the fractional division process [2,3,4]. This technique facilitates the ability to widen the bandwidth of the PLL, the two main advantages of which are making it possible to integrate the passive loop fil-

ter on chip, and reducing the sensitivity of the voltage-controlled oscillator (VCO) to pulling [5].

In order to ensure ideal phase-noise cancellation, the DAC gain must be matched to an equivalent gain in the PLL circuitry. Any mismatch results in imperfect cancellation, leading to a limit on the phase noise performance that can be achieved for the PLL [6]. A calibration technique to reduce this gain mismatch has been presented in [7], and has been shown to result in phase noise cancellation of up to 30dB. However this calibration system has a low loop bandwidth, and therefore a long settling time, constraining its use due to the fact that wireless transceivers often power the fractional-N PLL down when not receiving or transmitting in order to reduce power dissipation.

This paper presents a calibration technique suitable for phase noise canceling fractional-N PLLs. The presented technique has three advantages over the scheme in [7]. There is no sampling of the loop filter voltage that can result in an increased spurious tone around the carrier at an offset of the reference frequency. Calibration signals are used which result in improved performance of the calibration loop when non-ideal factors are taken into account, such as DC offset. Finally, the architecture of the calibration technique inherently has reduced offsets, and no quantization noise which allows for a much faster settling time than attainable with currently implemented methods. The result is that the calibration technique presented is suitable for background calibration in wireless systems.

Section II outlines the phase noise canceling PLL matching problem, as well as discussing current methods of solving this. Section III presents the new calibration technique. Section IV presents a suitable signal-processing model, used to prove the stability of the calibration loop. Section V presents a design example as well as simulations that verify the normal operating behaviour.

II. Calibration in Phase noise Canceling Fractional-N PLL

A. The Problem

A phase noise canceling fractional-*N* PLL is shown in Figure 1a, which consists of a typical fractional-*N* PLL plus a feed-forward current DAC. The operation of a delta-sigma fractional-*N* PLL is discussed at length in [1], so only the salient points necessary for understanding the calibration technique are discussed. A fractional-*N* PLL is never locked every reference sample due to the integer nature of the divider, i.e. $V_{ref}(t)$ and $V_{div}(t)$ are never locked in phase. This results in the phase-frequency detector (PFD) and charge pump (CP) supplying an error charge each reference period into the loop filter. If the PLL is locked in frequency, this charge can be well modeled by [6]

$$Q_{CP}[n] = I_{CP} T_{VCO} \sum_{k=0}^{n-1} e_Q[k], \tag{1}$$

where I_{CP} is the nominal CP current, T_{VCO} is the period of the PLL output under steady-state conditions, and $e_Q[n]$ is the shaped quantization noise from the Delta-

Sigma (ΔΣ) modulator[1].

All phase noise canceling fractional-*N* PLL [2, 3, 4] operate on the principle that every reference period, the DAC supplies charge in the form of a pulse of current that nominally cancels the CP charge given by (1). This is shown in Figure 1b where the charge from the DAC and CP completely cancel every reference period. The DAC charge can be well modeled by [6]

$$Q_{DAC}[n] = I_{DAC}T_{DAC}\left(\sum_{k=0}^{n-1} e_Q[k] + e_{req}[n]\right), \tag{2}$$

where I_{DAC} is the DAC full-scale current, T_{DAC} is the duration of the DAC current pulse, and $e_{req}[n]$ is the noise added by the digital requantizer. The requantizer is dithered such that $e_{req}[n]$ is uncorrelated from the quantization noise of the ΔΣ modulator [8]. For ideal cancellation, $I_{CP}T_{VCO}$ is equal to $I_{DAC}T_{DAC}$, therefore subtracting (2) from (1) results only in charge related to the requantization noise appearing at the input to the VCO. However timing mismatches between T_{VCO} and T_{DAC} and current mismatches between I_{CP} and I_{DAC} result in a portion of the CP charge remains on the loop filter. Neglecting the requantization noise term, this charge is a scaled version of (1). The result is shown in Figure 1c, which imposes a limit on the degree of phase noise cancellation that can be achieved.

[1] $e_Q[n]$ is the integer valued ΔΣ modulator quantization noise scaled by the quantization step size, and for a 2nd order ΔΣ modulator is bounded by 2

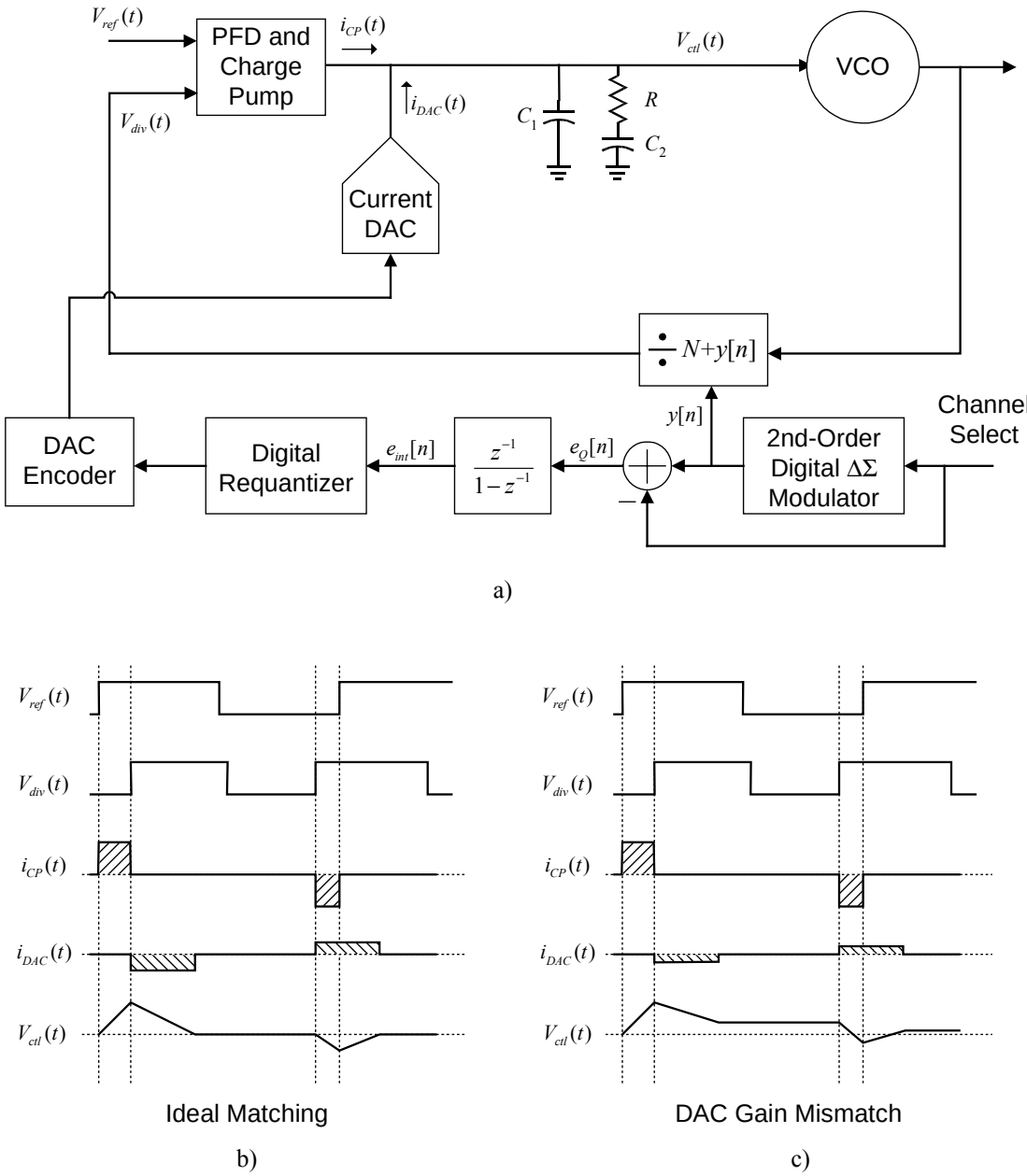

Figure 1: Phase Noise Canceling PLL; a) Block Diagram; b) Timing diagram, ideal matching; c) Timing diagram, DAC Gain mismatch

Since $e_Q[n]$ is a known quantity, the charge error on the loop filter can be sensed and I_{DAC} adjusted such that $I_{CP}T_{VCO}$ equals $I_{DAC}T_{DAC}$ and the charge due to $e_Q[n]$ is completely cancelled. A method of performing this is shown in Figure 2, equivalent

to the system presented in [7]. The loop filter voltage, $V_{ctl}(t)$ is buffered and then multiplied by a binary *correlation signal*, $c[n]$. This correlation signal must satisfy the following two requirements:

- The average of $c[n]$ must be zero
- $c[n]$ must be correlated with $e_Q[n]$ such that multiplying (1) by $c[n]$ results in a signal which has a non-zero average value

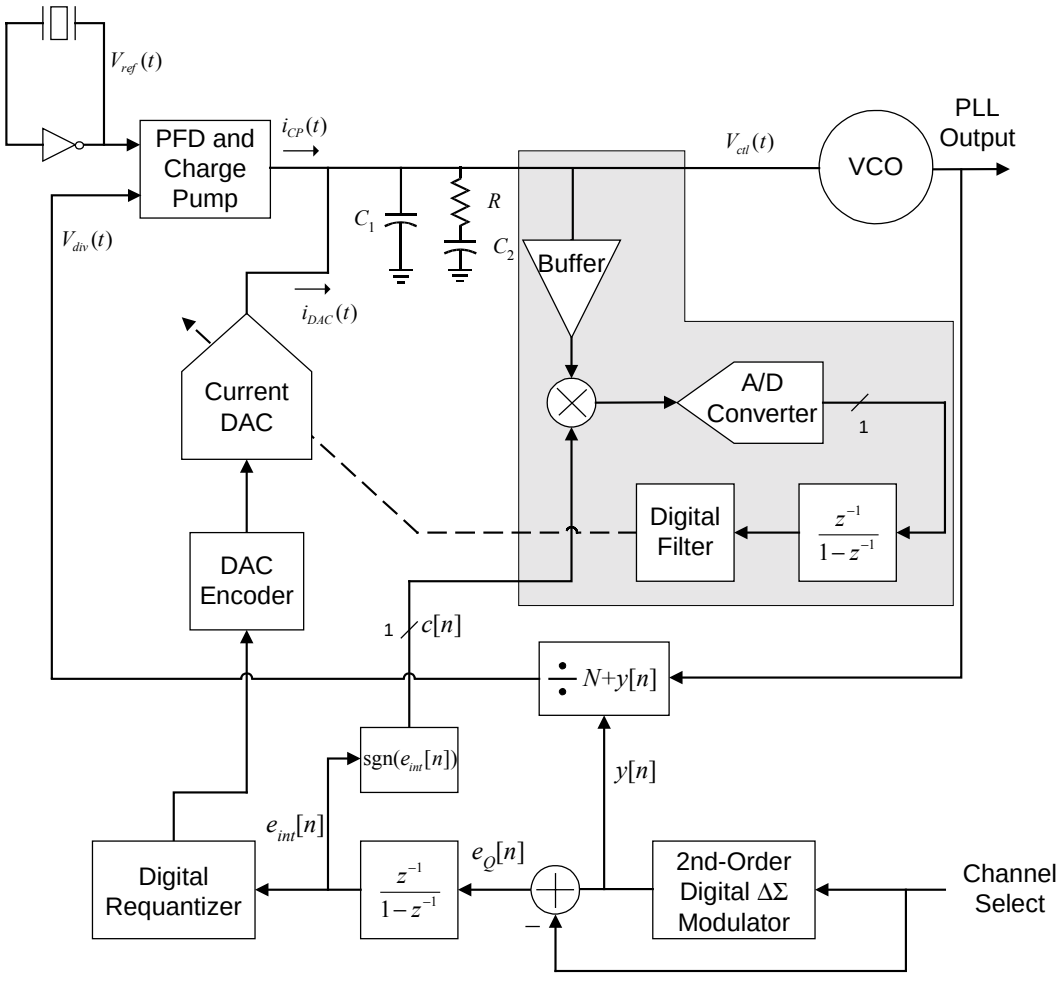

Figure 2: Previously Published Calibration Method for Phase Noise Canceling PLL

These requirements ensure that the dc component of $V_{ctl}(t)$ does not affect the calibration of I_{DAC}, and that the mismatch between the DAC and CP can be extracted and used in the calibration loop. The correlated signal is converted to a digital result, accumulated and filtered. The DAC bias is adjusted by switching weighted current sources. Since the correlated signal has a non-zero average value proportional to the CP and DAC mismatch, the calibration system adjusts I_{DAC} until the mismatch between $I_{CP}T_{VCO}$ and $I_{DAC}T_{DAC}$ is minimized and there is no dc remaining at the input to the accumulator.

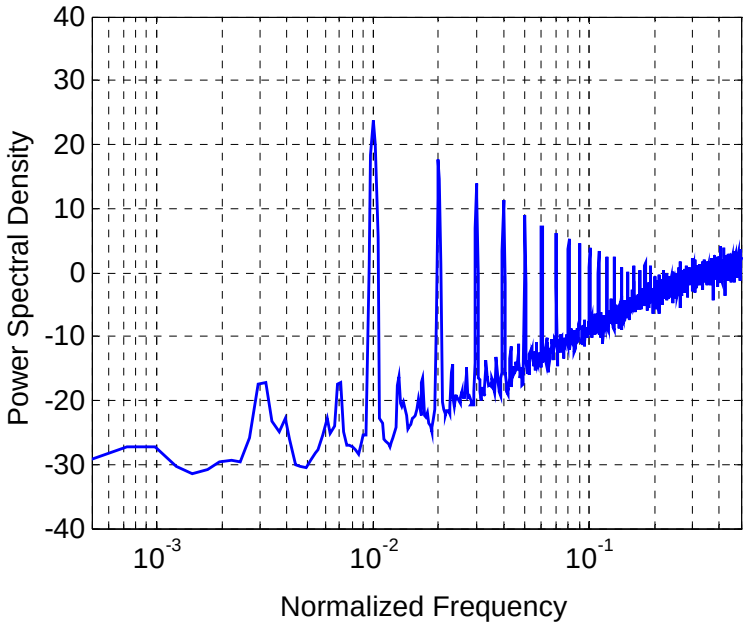

Figure 3: Sign of Integrated Quantization Error for a 2nd order ΔΣ Modulator

This particular calibration system suffers from restrictive filtering requirements; the correlation signal multiplied by the dc component of $V_{ctl}(t)$ results in a signal proportional to $c[n]$ modulating I_{DAC}. Moreover in the case where the correlation

signal is the sign of (1), spurious tones appear in $c[n]$. This is shown in Figure 3 for an input of 0.01 to the 2nd order ΔΣ modulator. It has been observed, but not proven in [2,9] that these spurs appear at multiples of the constant input times the reference frequency. Thus, any offsets present before correlation will result in periodic behaviour in the adjustment of I_{DAC}, which results in unwanted spurious tones at the output of the PLL.

B. Calibration Signal Generation

For the 2nd order ΔΣ modulator shown in Figure 1, the CP charge given in (1) can be expressed in terms of the quantizer error $e_{quant}[n]$[2]

$$Q_{CP}[n] = I_{CP} \cdot T_{VCO} \cdot \left(e_{quant}[n-1] - e_{quant}[n-2] \right), \tag{3}$$

Thus a correlation signal can be generated which is related with the individual $e_{quant}[n]$ terms in (3). In particular, with sgn(x) defined as 1 when $x \geq 0$ and –1 when $x<0$, two correlation signals are given by

$$\operatorname{sgn}\left(e_{quant}[n-1] \right), \qquad \text{and} \tag{4}$$

$$\frac{\operatorname{sgn}\left(e_{quant}[n-1] \right) - \operatorname{sgn}\left(e_{quant}[n-2] \right)}{2} + s[n], \tag{5}$$

where $s[n]$ is a zero-mean ergodic, 3-level, 1st order shaped random sequence uncorrelated with $e_{quant}[n-1]$ and $e_{quant}[n-2]$ that quantizes the three-level signal given by the first term in (5) into a binary signal [10]. If the ΔΣ modulator is properly dithered (e.g. according to the conditions in [11]), then $e_{quant}[n]$ has an asymptotically uniform

[2] The quantizer error is a digital number which has been normalized by the ΔΣ quantizer step size, and for a 2nd order ΔΣ modulator, $e_Q[n]=e_{quant}[n]-2\,e_{quant}[n-1]+e_{quant}[n-2]$

distribution, and both (4) and (5) will be asymptotically zero-mean signals. Multiplying (3) by either correlation signal results in a signal that has a non-zero mean, therefore (4) and (5) satisfy the necessary requirements for $c[n]$. Simulations shown in Figure 4 indicate that these choices of correlation signals have no spurious tones, hence the dc portion of $V_{ctl}(t)$ will not result in periodic modulation of I_{DAC}.

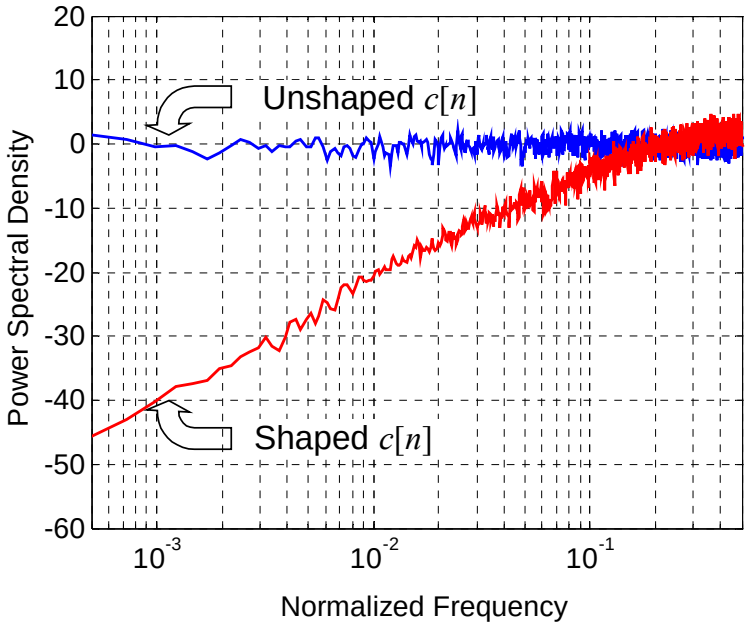

Figure 4: Correlation signals based on $e_{quant}[n]$

With this enhancement, there remain two problems in the calibration system from Figure 2. The analog-to-digital converter (ADC) samples the buffered loop filter voltage, so the buffer must provide sufficient isolation from the sampling process to avoid causing a spurious reference tone at the output of the PLL. Significant filtering is still required to filter the ADC quantization noise, as well as the noise introduced by multiplying the dc part of $V_{ctl}(t)$ with $c[n]$. This results in an effective reduction of the

bandwidth of the calibration loop, and hence longer settling time for calibration. For the design presented in [7], the settling time is on the order of one second [12].

III. Continuous-time Gain Calibration Technique

To overcome these problems, a calibration technique implemented in a phase-noise canceling fractional-*N* PLL is shown in Figure 5, with the calibration technique identified by the shaded parts in the figure. The VCO input, and loop filter are split into two equal parts, each of which have the same frequency response as in the PLL of Figure 2. The calibration circuitry consists of a continuous-time integrator and a voltage-to-current converter that controls I_{DAC}. To understand the system, consider the operation of the PLL from the CP and DAC to VCO as seen in Figure 6a. The calibration signal generator produces $c[n]$ given by (4) and (5), which switches the CP and DAC current, $i_{CP}(t)$ and $i_{DAC}(t)$, to either $i_p(t)$ or $i_n(t)$ each reference period.

Due to the equivalence of the VCO inputs, an equivalent change on either $V_p(t)$ or $V_n(t)$ will result in an identical VCO frequency change, and any differential change between $V_p(t)$ and $V_n(t)$ will result in no change. In this manner, the same current pulse in either $i_p(t)$ or $i_n(t)$ will result in the same VCO output change, therefore the correlation signal switching between $i_p(t)$ and $i_n(t)$ is transparent to the VCO. The effective loop filter voltage for controlling the VCO is the average of $V_p(t)$ and $V_n(t)$, given by $V_{ctl}(t)$ in Figure 6b. If the DAC and CP charges were perfectly matched, the net charge delivered to each loop filter would be zero each reference period, therefore $V_p(t)$ and $V_n(t)$ would settle to constant values and $V_{ctl}(t)$ would be at the correct value

required by the PLL. However, there are an unlimited number of possible choices for $V_p(t)$ and $V_n(t)$ that result in the correct value of $V_{ctl}(t)$ so it is impossible to predict the steady-state loop filter voltages by only considering the operation of the PLL.

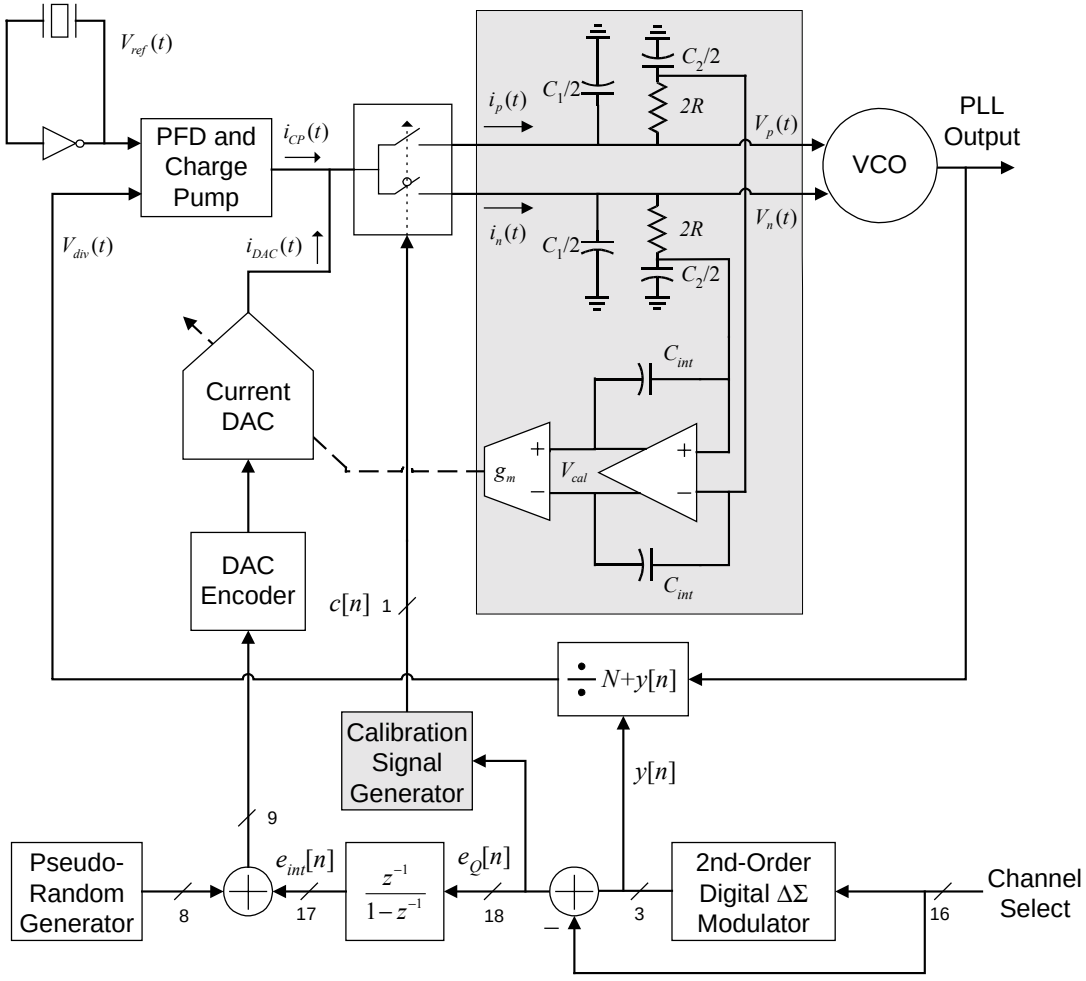

Figure 5: High-level Functional Diagram of Calibrated Fractional-*N* PLL

Next, consider the operation of the calibration loop. As an example, if the correlation signal is the sign of the accumulated quantization noise given in (1) [7], the result is the accumulation of positive CP charge on $V_p(t)$ and negative CP charge on $V_n(t)$. For the case where the DAC gain is smaller than the CP gain, $V_p(t)$ increases

and $V_n(t)$ decreases, causing the loop filter voltages to drift away from one another. The differential voltage change on $V_p(t)$ and $V_n(t)$ also results in a differential voltage between $V_{calp}(t)$ and $V_{caln}(t)$ which is accumulated through the continuous-time integrator, and used to adjust I_{DAC}. The DAC current is adjusted such that the average differential voltage between $V_{calp}(t)$ and $V_{caln}(t)$, and hence $V_p(t)$ and $V_n(t)$, is zero. Therefore the DAC and CP gains are matched. So, the calibration loop operating in conjunction with the PLL will cause $V_p(t)$ and $V_n(t)$ to each converge to unique values determined by the PLL output frequency and offsets within the PLL and calibration loops.

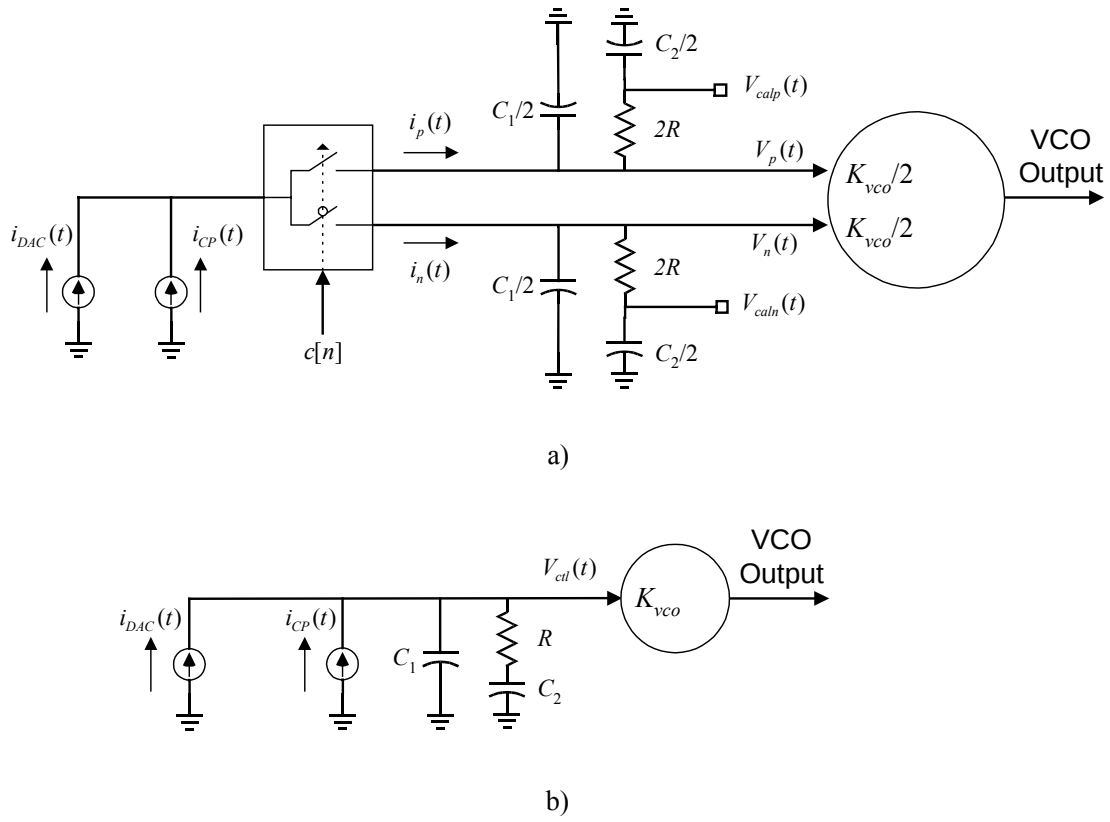

Figure 6: PLL Loop Modification for Calibration; a) Modified LF and VCO; b) Equivalent circuit for PLL

The PLL and calibration locking behaviour are shown in Figure 7 for a 10% mismatch between CP and DAC. Under ideal circuit behaviour, the operation of the loop is such that $V_p(t)$ and $V_n(t)$ converge to the same average voltage as the calibration loop converges. However, non-idealities in the circuit can result in incorrect settling or variation of the calibration loop output, as well as cause instability if the loop parameters are not chosen properly. The following section presents a signal processing model, and conditions that guarantee the stability of the system.

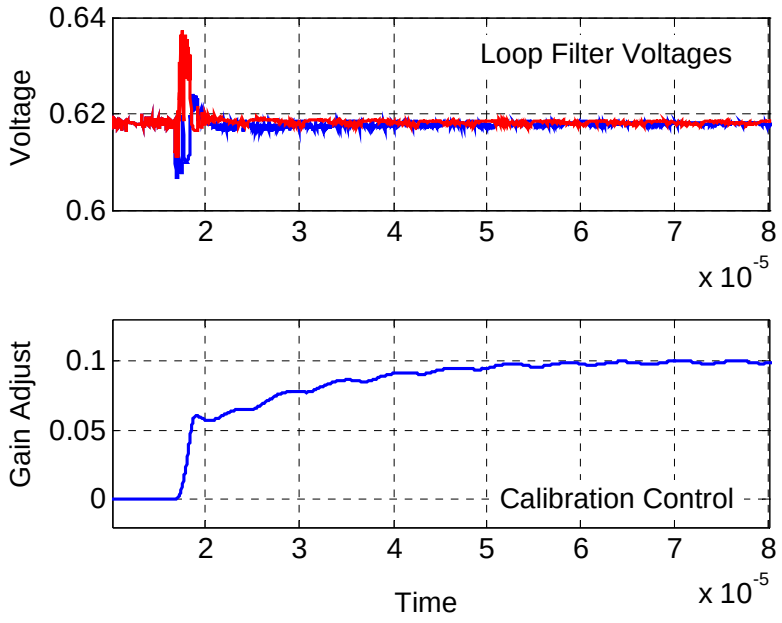

Figure 7: Loop Filter Voltages and Calibration Control Voltage

IV. Signal Processing Details

A. Signal Processing Model

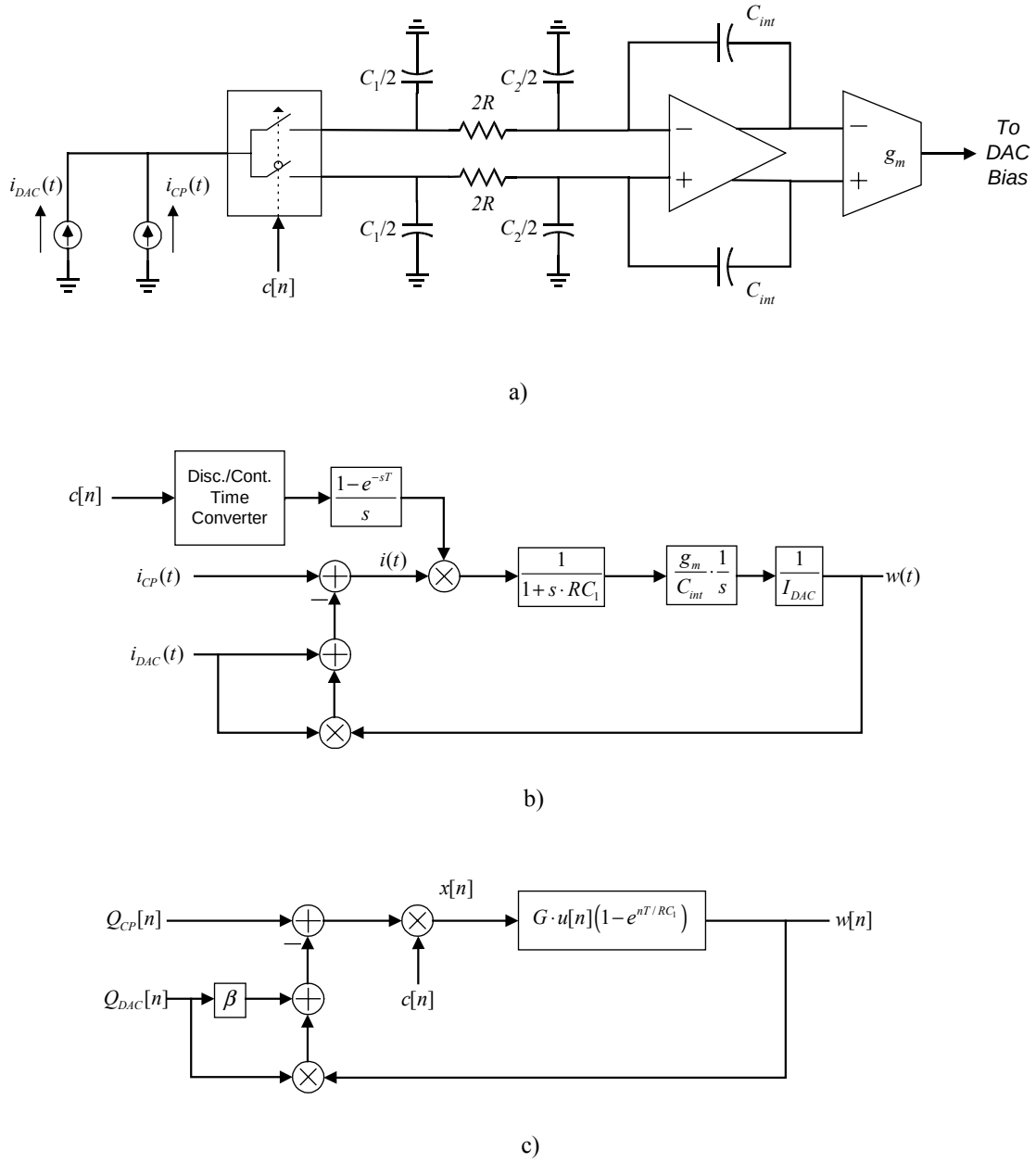

Figure 8: a) Calibration Loop Circuit; b) Continuous-time Model; c) Equivalent Discrete-time Signal Processing Model

The required continuous-time circuitry to implement the calibration technique

is shown in Figure 8a, consisting of a switch and passive filter followed by an ideal differential integrator[3] and voltage-to-current converter with a trans-conductance of g_m. The correlation signal $c[n]$ is held constant for the duration of $i_{CP}(t)$ and $i_{DAC}(t)$ and steers the currents to either the positive or negative input of the integrator each reference cycle. The equivalent continuous-time signal processing model of the calibration loop is shown in Figure 8b, where $c[n]$ is converted to a continuous-time signal, and the switch is replaced by a multiplication of the correlation signal with $i_{CP}(t)$ and $i_{DAC}(t)$, and $w(t)$ is the gain adjustment signal for the DAC.

Using (1) and (2), the CP and DAC current pulses can be well approximated by [6, 13]

$$i_{CP}(t) = \sum_{n=0}^{\infty} Q_{CP}[n]\delta(t - nT) \tag{6}$$

$$i_{DAC}(t) = \left(\sum_{n=0}^{\infty} \frac{Q_{DAC}[n]}{T_{DAC}} \delta(t - nT) \right) * p_{T_{DAC}}(t) \tag{7}$$

where T is the reference period, $\delta(t)$ is the impulse function, * is the convolution operator and $p_{T_{DAC}}(t)$ is a rectangular unit-amplitude pulse of width T_{DAC}. Taking the feedback signal $w(t)$ into account, the input to the calibration loop, $i(t)$ is

$$i(t) = \sum_{n=0}^{\infty} Q_{CP}[n] \cdot \delta(t - nT) - \left(\left(\sum_{n=0}^{\infty} \frac{Q_{DAC}[n]}{T_{DAC}} \cdot \delta(t - nT) \right) * p_{T_{DAC}}(t) \right) \cdot w(t) \tag{8}$$

Since the output of the calibration loop, $w(t)$ varies during the duration of a DAC pulse, it is impossible to maintain a constant $w(t)$ for all DAC pulses which re-

[3] A non-ideal integrator results in the addition of extra poles and zeros in the calibration loop, and with proper amplifier design, can be made negligible.

sults in perfect calibration of the DAC gain. However in all applications, a minimum level of gain matching performance, Δ, can be specified such that

$$(1-\Delta)I_{CP}T_{VCO} < \left|I_{DAC}T_{DAC}\right| < (1+\Delta)I_{CP}T_{VCO} \tag{9}$$

Appendix A outlines the necessary conditions on the calibration loop parameters to ensure that the variation in $w(t)$ is small with respect to Δ, which can be given as

$$\frac{I_{CP}T_{VCO}g_m}{C_{int}I_{DAC}}\frac{1-e^{-T_{DAC}/RC_1}}{1-e^{-T/RC_1}} < \Delta\,, \tag{10}$$

therefore $w(t)$ can be assumed to be constant for the duration of a DAC pulse.

Sampling $w(t)$ uniformly at intervals of T, the system can be modeled as a discrete-time system with charge inputs defined in (1) and (2), and the impulse response of the discrete-time filter is simply the continuous-time impulse response of the filter and integrator in Figure 8b sampled at $t = nT$. This model is shown in Figure 8c, where the mismatch between CP and DAC paths is explicitly represented by the parameter β, $I_{CP}T_{VCO} = I_{DAC}T_{DAC}$, and the corresponding discrete-time impulse responses are also shown. The parameter G can be readily derived from Figure 8b as

$$G = \frac{g_m}{C_{int}\cdot I_{DAC}}\,. \tag{11}$$

B. Calibration Loop Performance

The two equations used to describe the calibration loop are

$$x[n] = c[n]\cdot\left\{Q_{CP}[n] - (\beta + w[n])Q_{DAC}[n]\right\} \tag{12}$$

$$w[n] = G \cdot x[n] * \left\{ u[n]\left(1 - e^{-nT/RC_1}\right) \right\} \tag{13}$$

where $u[n]$ is the unit step function. Since (12) and (13) represent a non-linear feed-back system, a closed-form expression for $w[n]$ can be derived, and then used to evaluate the conditions under which bounded-input, bounded-output (BIBO) stability holds. Define

$$\begin{aligned} C_0 + C_{CP}[n] &\triangleq Q_{CP}[n] \cdot c[n], \quad \text{and} \\ C_R + C_{req}[n] &\triangleq I_{DAC} \cdot T_{DAC} \cdot e_{req}[n] \cdot c[n], \end{aligned} \tag{14}$$

where C_0 and C_R are the sample averages of $Q_{CP}[n] \cdot c[n]$ and $I_{DAC} \cdot T_{DAC} \cdot e_{req}[n] \cdot c[n]$ respectively. Claim 1 in Appendix B shows that for the choices of $c[n]$ given in (4) and (5), C_0 exists, and furthermore is given by

$$I_{CP} \cdot T_{VCO} \cdot \frac{2^{N-2} - 1}{2^N} \tag{15}$$

To prove the calibration loop is stable, the equations (12) and (13), and the result in (15) can be used in Claim 2 in Appendix B. The stability condition required is that

$$\left| G\left(1 - e^{-T/RC_1}\right) Q_{DAC}[n] \right| < 1 \tag{16}$$

for all DAC charge samples. From (11), (16) and the fact that $|Q_{DAC}[n]| \le I_{DAC} T_{DAC}$ reduces to

$$\left| \frac{g_m}{C_{int}} \left(1 - e^{-T/RC_1}\right) T_{DAC} \right| < 1 \tag{17}$$

The following section outlines a practical example which shows that for typical values

for calibration loop parameters, (17) is satisfied and the loop is stable.

V. Simulations and Limitations

Suppose that a calibration loop is to be designed for a Bluetooth compliant fractional-*N* PLL with a block diagram shown in Figure 5 and component values given in Table 1. The component requirements for the PLL and phase noise cancellation system are determined independently of the calibration technique, and will not be discussed as they are presented in [6]. The PLL parameters from Table 1 yield a PLL loop bandwidth of approximately 443kHz. In the absence of phase noise cancellation, the phase noise at a 3MHz offset can be calculated from [1] as –84dBc/Hz. To meet the Bluetooth specification of less than –120dBc/Hz at a 3MHz offset, the DAC gain matching must be accurate to 0.01. Furthermore, since transmission packets for Bluetooth are less than 625μs, the calibration loop must settle within a fraction of that time. For adequate noise performance, a settling time of 50μs to 0.01 accuracy is required.

Table 1: Parameters for Fractional-N PLL from Figure 2

PLL Parameters	
Reference Frequency, T	12 MHz
Output Frequency	2.4 – 2.5 GHz
ΔΣ Quantizer step, 2^N	2^{16}
Charge Pump Current, I_{CP}	2mA
Nominal DAC Current, I_{DAC}	1mA
VCO gain, K_{VCO}	120MHz/V
Loop Filter Resistor, R	2.5 kΩ
Loop Filter Capacitor, C_1	36 pF
Loop Filter Capacitor, C_2	564 pF
DAC resolution	9 bit
DAC pulse duration, T_{DAC}	$4T_{VCO}$
Required gain matching, Δ	0.01
Required settling performance	50μs

The validity of the discrete-time model, as well as the stability is verified by substituting the parameters in Table 1 into the left sides of (10) and (17), which results in respective bounds on the calibration loop parameters, g_m and C_{int} of

$$\frac{g_m}{C_{int}} < 4.0\times10^8, \qquad \text{and} \qquad \frac{g_m}{C_{int}} < 1.0\times10^9. \tag{18}$$

Clearly the most stringent requirement is satisfying the continuous-time to discrete-time model approximation. The appropriate choice of parameters to meet the settling time requirements can be found through simulations. Simulation results are shown in Figure 9 for a C_{int} of 10pF and a g_m of 0.2mS and 66µS. The simulator is similar to Hspice, and all blocks are implemented with ideal behavioral components. While both choices of parameters meet the bound given in (18), the settling time requirement is achieved when g_m is 200µS.

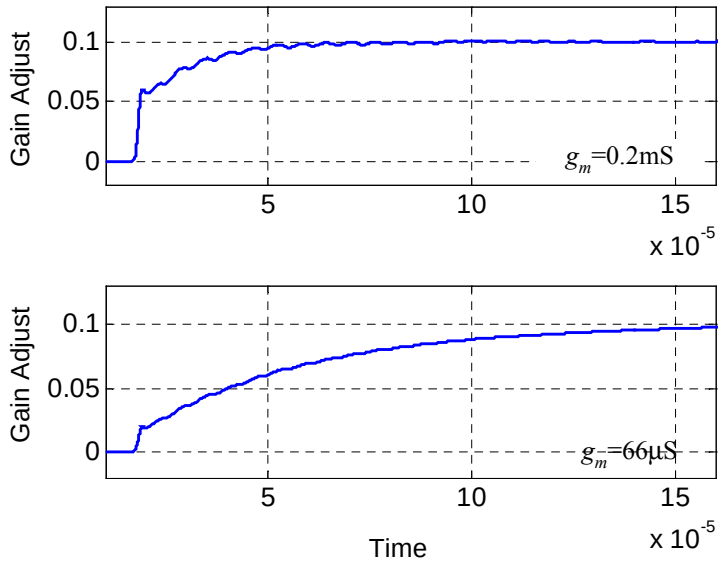

Figure 9: Settling Time for Calibration Technique

The phase noise of the calibrated fractional-*N* PLL is shown in Figure 10 and compared with that of an ideally matched PLL. As shown, the phase noise resulting from calibration is negligible compared to the case where there is no gain mismatch. The calibration technique results in a phase noise cancellation improvement of more than 20dB over the uncalibrated case with a 10% gain mismatch.

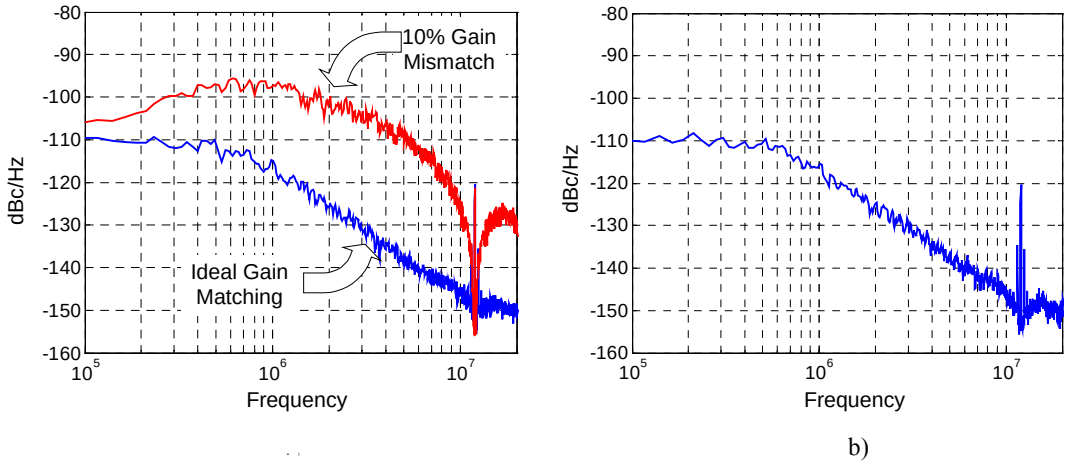

Figure 10: PLL Phase Noise; a) Without Calibration; b) Calibration enabled for β=0.9

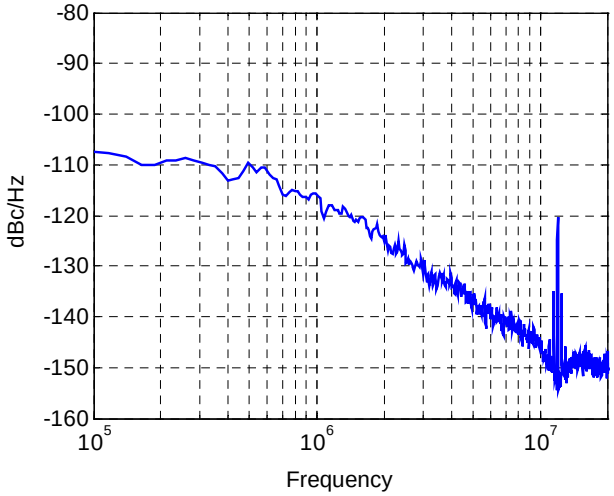

Figure 11: Calibration enabled for random mismatches in PLL loop

In practice, component mismatches could result in errors in the calibration technique. With mismatches in the component values of approximately 5%, the phase noise at the output of the PLL remains well behaved as shown in Figure 11, demonstrating the robustness of the calibration technique. It can be shown that component mismatches simply result in a replica of the CP and DAC charges appearing at the integrator input. Since these charges have zero dc content due to the PLL loop, this results in noise on the calibration signal, not misalignment. This demonstrates the viability of this calibration technique for phase-noise canceling delta-sigma fractional-*N* PLL.

VI. Conclusions

An analysis of a calibration technique applied to a phase-noise canceling fractional-*N* PLL has been presented. Conditions have been presented to ensure the stability of the technique, as well as an approximation for the settling time, which is also used to determine the calibration technique parameters. These results enable the customization of this calibration technique in response to target PLL specifications.

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APPENDIX A

Consider the continuous-time calibration loop model shown in Figure 8b. The impulse response, $g(t)$, from the input of the filter to $w(t)$ can be derived as

$$g(t) = \frac{g_m}{C_{int} I_{DAC}} u(t) \cdot \left\{1 - e^{-t/RC_1}\right\}. \tag{19}$$

The worst-case variation of (19) during a DAC pulse event occurs when the DAC gain is zero. Using (6) and (19), the deviation of $w(t)$ over a duration of T_{DAC} during the n^{th} DAC and CP event can be expressed as

$$\left|w(nT) - w(nT + T_{DAC})\right| = \frac{g_m}{C_{int} I_{DAC}} \left| \sum_{k=0}^{n} Q_{CP}[n] \left\{ e^{-(kT + T_{DAC})/RC_1} - e^{-kT/RC_1} \right\} \right| \tag{20}$$

Recalling from (3) that $|Q_{CP}[n]| \le I_{CP} T_{VCO}$, the right side of (20) can be bounded by

$$\begin{aligned} \frac{I_{CP} T_{VCO} g_m}{C_{int} I_{DAC}} \left\{1 - e^{-T_{DAC}/RC_1}\right\} \sum_{k=0}^{n} e^{-kT/RC_1} &= \frac{I_{CP} T_{VCO} g_m}{C_{int} I_{DAC}} \left\{1 - e^{-T_{DAC}/RC_1}\right\} \frac{1 - e^{-(n+1)T/RC_1}}{1 - e^{-T/RC_1}} \\ &< \frac{I_{CP} T_{VCO} g_m}{C_{int} I_{DAC}} \frac{1 - e^{-T_{DAC}/RC_1}}{1 - e^{-T/RC_1}} \end{aligned} \tag{21}$$

In order to ensure that $w(t)$ does not change over the duration of a DAC pulse, it is necessary to keep (21) small. This leads to

$$\frac{I_{CP} T_{VCO} g_m}{C_{int} I_{DAC}} \frac{1 - e^{-T_{DAC}/RC_1}}{1 - e^{-T/RC_1}} < \Delta \tag{22}$$

where Δ is the specified level of gain calibration required for $w(t)$.

APPENDIX B

This appendix provides the claims necessary to prove the convergence of the calibration loop. Consider the signal-processing model shown in Figure 8c. With $c[n]$ given by (5), Claim 1 proves that the charge supplied by the CP and DAC are ergodic, i.e. C_0 exists, and Claim 2 provides an intermediate claim to prove the stability of the calibration loop.

Definition: $E_{quant}[n]$ is an integer-valued sequence representing the quantizer noise from the ΔΣ modulator such that

$$e_{quant}[n] \triangleq \frac{E_{quant}[n]}{2^N},$$

where 2^N is the quantizer step size of the ΔΣ modulator. This definition is provided to ensure congruency with the theorems outlined in [14].

Claim 1: Suppose that the correlation signals given by (5) are generated in conjunction with a 2nd order ΔΣ modulator designed to satisfy the conditions of Theorem 3 in [14] with a quantizer step size of 2^N. Then C_0 is given by

$$C_0 = I_{CP} \cdot T_{VCO} \cdot \frac{2^{N-2}-1}{2^N}.$$

Proof: Consider the case where $c[n]$=sgn($e_{quant}[n-1]$)= sgn($E_{quant}[n-1]$). Then from (3),

$$C_0 + C_{CP}[n] = Q_{CP}[n] \cdot c[n] = \frac{I_{CP}T_{VCO}}{2^N} \cdot \left(\left| E_{quant}[n-1] \right| - \operatorname{sgn}\left(E_{quant}[n-1] \right) \cdot E_{quant}[n-2] \right). \quad (23)$$

From (14), C_0 is defined as the sample average of (23). First consider the sample average of $|E_{quant}[n]|$. Theorem 1 in [14] proves that $E_{quant}[n]$ asymptotically approaches a uniform random distribution as $n\to\infty$ given by

$$P_U(u) = 2^{-N}, \quad -2^{N-1}+1 \le u \le 2^{N-1}. \tag{24}$$

And therefore,

$$\lim_{n\to\infty} \mathrm{E}\left[\left|E_{quant}[n]\right|\right] = E\left[|u|\right] = 2^{N-2}. \tag{25}$$

For any postive number m, define

$$X_n = \left|E_{quant}[n+m]\right| - 2^{N-2}, \tag{26}$$

and Lemma 3 from [14] shows that $E[X_n]\to 0$ is sufficient to prove that the sample average of $|E_{quant}[n]|$ converges in probability to 2^{N-2}, or in other words

$$\lim_{n\to\infty} \frac{1}{n} \sum_{k=m}^{n+m-1} \left|e_{quant}[k]\right| = \frac{2^{N-2}}{2^N}. \tag{27}$$

Now consider the second term in (23). Theorem 2 in [14] also proves that the joint pmf of any two samples of the quantizer error converges in distribution to a jointly uniform random variable given by

$$P_{U,V}(u,v) = 2^{-2N}, \quad -2^{N-1}+1 \le u,v \le 2^{N-1}, \tag{28}$$

and therefore

$$\lim_{n\to\infty} \mathrm{E}\left[\operatorname{sgn}\left(E_{quant}[n]\right)\cdot E_{quant}[n-1]\right] = \mathrm{E}\left[\operatorname{sgn}(u)\cdot v\right] = 1. \tag{29}$$

For any positive number m, let

$$X_n = \mathrm{sgn}\left(E_{quant}[n+m]\right) E_{quant}[n+m-1] - 1, \tag{30}$$

and Lemma 3 from [14] shows that $E[X_n] \to 0$ is sufficient to prove that the sample average of $\mathrm{sgn}(E_{quant}[n]) \cdot E_{quant}[n-1]$ converges in probability to 1. Therefore due to the linearity of the sample mean operator,

$$\lim_{n\to\infty} \frac{1}{n} \sum_{k=m}^{n+m-1} \left\{ \left| e_{quant}[k] \right| - \mathrm{sgn}\left(e_{quant}[k]\right) \cdot e_{quant}[k-1] \right\} = \frac{2^{N-2}-1}{2^N}, \tag{31}$$

which proves Claim 1 for $c[n]=\mathrm{sgn}(e_{quant}[n])$, and the convergence is irrespective of the initial start index, m. Now consider the second correlation signal given by

$$c[n] = \frac{\mathrm{sgn}\left(e_{quant}[n]\right) - \mathrm{sgn}\left(e_{quant}[n-1]\right)}{2} + s[n],$$

where $s[n]$ is by definition a zero-mean ergodic sequence. For this correlation signal, (23) can be expressed as

$$\begin{aligned} C_0 + C_{CP}[n] = \frac{I_{CP} \cdot T_{VCO}}{2^N} \cdot \frac{1}{2} \Big\{ & \left| E_{quant}[n] \right| + \left| E_{quant}[n-1] \right| - \mathrm{sgn}\left(E_{quant}[n]\right) \cdot E_{quant}[n-1] \\ & - \mathrm{sgn}\left(E_{quant}[n-1]\right) \cdot E_{quant}[n] + 2 \cdot s[n] \cdot \left(E_{quant}[n] - E_{quant}[n-1]\right) \Big\} \end{aligned}. \tag{32}$$

The first 4 terms have already been shown to converge to (31), and since $s[n]$ is a zero-mean ergodic sequence uncorrelated from the quantization error, C_0 is given by

$$C_0 = I_{CP} \cdot T_{VCO} \cdot \frac{2^{N-2}-1}{2^N}$$

Therefore Claim 1 is proven for both correlation signals.

■

For the following stability claim, consider a system of non-linear difference equations defined by

$$x[n] = u_1[n] - w[n] \cdot u_2[n] \tag{33}$$
$$w[n] = x[n] * h[n] \tag{34}$$

where $u_1[n]$ and $u_2[n]$ are bounded inputs, and $h[n]$ is a filter with the following characteristics

$$h[n] = 0 \quad \text{for} \quad n \le 0, \qquad h[1] > 0, \qquad \text{and} \qquad h[n] - h[n-1] = Ke^{-(n-1)\alpha} \tag{35}$$

where K and α are positive constants. Without loss of generality, the system is assumed to start at $n = 0$ such that $u_1[n] = u_2[n] = 0$ for $n < 0$.

Claim 2: Suppose that

$$\left| h[1] \cdot u_2[n] \right| < 1 \tag{36}$$

Then the system of equations defined by (33) and (34) are BIBO stable if for any positive integer m,

$$\lim_{N \to \infty} \frac{1}{N} \sum_{n=m}^{N+m-1} u_2[n] = U > 0 \tag{37}$$

Proof: First, consider the product given by

$$\prod_{l=k+1}^{n} \left(1 - h[1] u_2[l]\right) \tag{38}$$

It follows from (36) and the fact that $|1 - x| \le e^{-x}$ that

$$\left|\prod_{l=k+1}^{n}\left(1-h[1]u_2[l]\right)\right| \le e^{-h[1]\sum_{l=k+1}^{n}u_2[l]} \tag{39}$$

(37) implies that for any index m, and positive number ε, there exists an $N_{\varepsilon,m}$ such that for all $N > N_{\varepsilon,m}$,

$$\sum_{n=m}^{N+m-1}\left(u_2[n]-U\right) < N\varepsilon \tag{40}$$

For all m and ε, $N_{\varepsilon,m}$ is finite. Therefore, for some $\varepsilon < U$, define

$$N' = \max\left\{N_{m,\varepsilon}\right\}_{m=0}^{\infty}, \tag{41}$$

and for $n - k > N$', the right side of (39) is bounded by

$$e^{-h[1](n-k)U}e^{-h[1]\left(\sum_{l=k+1}^{n}(u_2[l]-U)\right)} \le e^{-h[1](n-k)(U-\varepsilon)} \tag{42}$$

Therefore, there exists positive numbers D, and β such that for all n and k,

$$\left|\prod_{l=k+1}^{n}\left(1-h[1]u_2[l]\right)\right| \le De^{-(n-k)\beta}, \tag{43}$$

and therefore (38) is bounded by an exponentially decreasing function. The non-linear difference equations given by (33), (34) and (35) can be expressed as

$$\begin{aligned} w[n] &= \sum_{k=0}^{n}h[n-k]\left(u_1[k]-w[k]u_2[k]\right) \\ &= h[1]u_1[n-1]+\sum_{k=0}^{n-2}\left(h[n-k]-h[n-1-k]\right)u_1[k]+w[n-1]\left(1-h[1]u_2[n-1]\right) \\ &\quad -\sum_{k=0}^{n-2}\left(h[n-k]-h[n-1-k]\right)w[k]u_2[k]. \end{aligned} \tag{44}$$

Recursively substituting (44) into itself to eliminate $w[k]$, $k = 0, \ldots, n-1$ yields

$$w[n] = \sum_{k=0}^{n-1} \left\{ h[1]u_1[n-k-1] + \sum_{l=0}^{n-k-2} \left(h[n-l] - h[n-l-1] \right) u_1[l] \right\} \cdot \left\{ \prod_{m=1}^{k} \left(1 - h[1]u_2[n-m] \right) - u_2[n-k] \sum_{m=2}^{k} \left(h[m] - h[m-1] \right) \cdot \prod_{o=m}^{k-1} \left(1 - h[1]u_2[n-k+o] \right) \right\}. \tag{45}$$

The above equation consists of four separate terms. For a bounded input, there exists a B such that $u_1[n]$ and $u_2[n]$ are bounded by B in magnitude. From (43), the first term can be bounded by

$$\left| \sum_{k=0}^{n-1} h[1]u_1[n-k-1] \prod_{m=1}^{k} \left(1 - h[1]u_2[n-m] \right) \right| < h[1]B \sum_{k=0}^{n-1} De^{-k\beta} = h[1]B \cdot D \frac{1-e^{-n\beta}}{1-e^{-\beta}} < \frac{h[1]B \cdot D}{1-e^{-\beta}} \tag{46}$$

Using (35) the second term can be expressed and bounded by

$$\left| \sum_{k=0}^{n-1} \sum_{l=0}^{n-k-2} \left(h[n-l] - h[n-l-1] \right) u_1[l] \prod_{m=1}^{k} \left(1 - h[1]u_2[n-m] \right) \right| \le B \sum_{k=0}^{n-1} \sum_{l=0}^{n-k-2} Ke^{-(n-l-1)\alpha} \cdot De^{-k\beta} = KBD \sum_{k=0}^{n-1} e^{-k\beta} \cdot e^{-(k+1)\alpha} \sum_{l=0}^{n-k} e^{-l\alpha}. \tag{47}$$

The expression on the right side of (47) can be further reduced resulting in

$$B \sum_{k=0}^{n-1} De^{-k\beta} \cdot Ke^{-(k+1)\alpha} \frac{1-e^{-(n-k+1)\alpha}}{1-e^{-\alpha}} \le KBD \frac{e^{-\alpha}}{1-e^{-\alpha}} \frac{1-e^{-n(\alpha+\beta)}}{1-e^{-(\alpha+\beta)}} \le \frac{KBDe^{-\alpha}}{\left(1-e^{-\alpha}\right)\left(1-e^{-(\alpha+\beta)}\right)} \tag{48}$$

The third term from (45) can be expressed and bounded by

$$\left|\sum_{k=0}^{n-1} h[1]u_1[n-k-1]\cdot u_2[n-k]\sum_{m=2}^{k}\left(h[m]-h[m-1]\right)\cdot\prod_{o=m}^{k-1}\left(1-h[1]u_2[n-k+o]\right)\right| \le h[1]B^2\sum_{k=0}^{n-1}\sum_{m=2}^{k} Ke^{-(m-1)\alpha}\cdot De^{-(k-m)\beta} \tag{49}$$

The expression on the right side of (49) can be bounded by

$$\begin{aligned} h[1]B^2KD\sum_{k=0}^{n-1}e^{-k\beta}\sum_{m=2}^{k}e^{-(m-1)\alpha}\cdot e^{m\beta} &= h[1]B^2KDe^{\alpha}e^{-2(\alpha-\beta)}\sum_{k=0}^{n-1}e^{-k\beta}\frac{1-e^{-(k-1)(\alpha-\beta)}}{1-e^{-(\alpha-\beta)}} \\ &= h[1]B^2KDe^{\alpha}e^{-2(\alpha-\beta)}\frac{1}{1-e^{-(\alpha-\beta)}}\left[\frac{1-e^{-n\beta}}{1-e^{-\beta}}-e^{(\alpha-\beta)}\frac{1-e^{-n\alpha}}{1-e^{-\alpha}}\right] \\ &\le h[1]B^2KDe^{\alpha}e^{-2(\alpha-\beta)}\frac{1}{1-e^{-(\alpha-\beta)}}\left[\frac{1}{1-e^{-\beta}}-\frac{e^{(\alpha-\beta)}}{1-e^{-\alpha}}\right] \end{aligned} \tag{50}$$

Finally, the fourth term in (45) can be expressed and bounded by

$$\begin{aligned} &\left|\sum_{k=0}^{n-1}\sum_{l=0}^{n-k-2}\left(h[n-l]-h[n-l-1]\right)u_1[l]\,u_2[n-k]\right. \\ &\quad\left.\cdot\sum_{m=2}^{k}\left(h[m]-h[m-1]\right)\cdot\prod_{o=m}^{k-1}\left(1-h[1]u_2[n-k+o]\right)\right| \\ &\quad\le B^2\sum_{k=0}^{n-1}\sum_{l=0}^{n-k-2}e^{-(n-l-1)\alpha}\sum_{m=2}^{k}Ke^{-(m-1)\alpha}\cdot De^{-(k-m)\beta} \\ &\quad= KDB^2e^{\alpha}\sum_{k=0}^{n-1}e^{-k\beta}\cdot e^{-(k+1)\alpha}\sum_{l=0}^{n-k-2}e^{-l\alpha}\sum_{m=2}^{k}e^{m(\beta-\alpha)} \end{aligned} \tag{51}$$

Solving the right side of (51) yields

$$
\begin{aligned}
& KDB^2 e^{\alpha} \sum_{k=0}^{n-1} e^{-k\beta} \cdot e^{-(k+1)\alpha} \frac{\left(1-e^{-(n-k-1)\alpha}\right)}{1-e^{-\alpha}} \frac{e^{2(\beta-\alpha)}\left(1-e^{-(k-1)(\beta-\alpha)}\right)}{1-e^{-(\beta-\alpha)}} \\
& \le \frac{KDB^2 \cdot e^{2(\beta-\alpha)}}{\left(1-e^{-\alpha}\right)\left(1-e^{-(\beta-\alpha)}\right)} \sum_{k=0}^{n-1} e^{-k(\beta+\alpha)}\left(1-e^{-(k-1)(\beta-\alpha)}\right) \\
& = \frac{KDB^2 \cdot e^{2(\beta-\alpha)}}{\left(1-e^{-\alpha}\right)\left(1-e^{-(\beta-\alpha)}\right)} \left\{ \sum_{k=0}^{n-1} e^{-k(\beta+\alpha)} - e^{\beta-\alpha} \sum_{k=0}^{n-1} e^{-k(\beta+\alpha+\beta-\alpha)} \right\} \\
& = \frac{KDB^2 \cdot e^{2(\beta-\alpha)}}{\left(1-e^{-\alpha}\right)\left(1-e^{-(\beta-\alpha)}\right)} \frac{1-e^{-n(\beta+\alpha)}}{1-e^{-(\beta+\alpha)}} \frac{1-e^{-2n\beta}}{1-e^{-2\beta}} \\
& \le \frac{KDB^2 \cdot e^{2(\beta-\alpha)}}{\left(1-e^{-\alpha}\right)\left(1-e^{-(\beta-\alpha)}\right)\left(1-e^{-(\beta+\alpha)}\right)\left(1-e^{-2\beta}\right)}
\end{aligned}
\tag{52}
$$

which proves the BIBO stability of (33) and (34).

■

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Chapter 2 : A Digital Quantizer with Shaped Quantization Noise that Remains Well Behaved after Nonlinear Distortion

ABSTRACT

A major problem in oversampling digital-to-analog converters and fractional-*N* frequency synthesizers, which are ubiquitous in modern communication systems, is that the noise they introduce contains spurious tones. The spurious tones are the result of digitally generated, quantized signals passing through non-linear analog components. This paper presents a new method of digital quantization, called Segmented Quantization, special cases of which avoid the spurious tone generation problem. Sufficient conditions are derived that ensure certain statistical properties of the quantization noise, including the absence of spurious tones after non-linear distortion. A practical example is presented and shown to satisfy these conditions.

I. INTRODUCTION

Oversampling digital-to-analog converters (DACs) and fractional-*N* phase-locked loops (PLLs) are each enabling components in modern communication systems [15, 16, 17]. In both components a *digital delta-sigma* (ΔΣ) *modulator*, i.e., a ΔΣ modulator implemented with digital logic, is used to coarsely quantize a constant or slowly-varying digital sequence. The quantized sequence can be viewed as the sum of the original sequence plus spectrally shaped *quantization noise* that has most of its power outside of a given low-frequency *signal band*. Ultimately, the quantized sequence is converted to an analog signal and further processed by analog circuitry in-

cluding a lowpass filter to suppress quantization noise outside of the signal band.

In most communications applications it is critical that any spurious tones in the noise introduced by DACs and fractional-*N* PLLs have very low power [16, 18]. In principle, dither applied to a ΔΣ modulator can prevent the quantization noise from containing any spurious tones whatsoever [19, 20]. Nevertheless, in practice digital ΔΣ modulators are major sources of spurious tones in oversampling DACs and fractional-*N* PLLs [21, 22]. Regardless of how dither is applied, all ΔΣ modulator architectures known to the authors give rise to spurious tones when their quantization noise is subjected to non-linear distortion. This is particularly problematic in fractional-*N* PLLs wherein the input to the ΔΣ modulator usually is a constant and the output sequence from the ΔΣ modulator is converted to analog form and subjected to a various non-linear operations because of non-ideal circuit behavior. Heretofore, the only known solution was to make the analog circuitry very linear so that the spurious tones have sufficiently low power for the given application. Unfortunately, this limits design options and results in higher analog circuit power consumption than would be required if less linear analog circuits could be tolerated.

This paper presents a new type of digital quantizer, referred to as a *Segmented Quantizer* (SQ), that addresses this problem. The paper presents sufficient conditions on the segmented quantizer's design parameters to ensure certain statistical properties of the quantization noise and the running sum of the quantization noise. These properties include the absence of spurious tones under application of non-linear distortion. An example is presented that satisfies the conditions and is demonstrated via computer

simulation. The work borrows ideas from dc-free codes [23, 24] and dynamic element matching tree structured encoders [25, 26].

The paper consists of three main sections. Section II presents the principle of segmented quantization, as well as an example that illustrates the appearance of spurious tones when the quantized sequence is subjected to non-linear distortion. Section III presents the sufficient conditions mentioned above. Section IV presents an example segmented quantizer that satisfies the sufficient conditions.

II. Segmented Quantization

A. Spectral Properties of Interest

As outlined above, fractional-N PLLs and delta-sigma DACs ultimately generate analog waveforms. Each such waveform contains components corresponding to digitally generated quantization noise, $s[n]$, and, in the case of fractional-N PLLs, its running sum,

$$t[n] = \sum_{k=0}^{n} s[k]. \tag{53}$$

Moreover, inevitable non-ideal analog circuit behavior generally causes non-linear distortion. The distortion can be any non-linear function, but for almost all practical applications can be represented by a memory-less, truncated power series. This gives rise to components in the output waveform corresponding to $s^p[n]$ for p = 1, 2, 3, …, h_s, and $t^p[n]$ for p = 1, 2, 3, …, h_t, where h_s and h_t are the highest significant orders of distortion for the given application applied on $s[n]$ and $t[n]$ respectively.

Most communication system standards specify the required performance of such systems in terms of quantities that can be measured using spectrum analyzers, so the properties of the waveforms typically are quantified in the laboratory using spectrum analyzers. Although the waveforms themselves are considered to be random processes in most cases, spectrum analyzers can only average over time, not over ensemble. Therefore, in such applications the properties of the periodograms of $s^p[n]$ and $t^p[n]$ given by

$$I_{s^p,L}(\omega) = \frac{1}{L}\left|\sum_{n=0}^{L-1} s^p[n]e^{-j\omega n}\right|^2 \tag{54}$$

and

$$I_{t^p,L}(\omega) = \frac{1}{L}\left|\sum_{n=0}^{L-1} t^p[n]e^{-j\omega n}\right|^2 \tag{55}$$

are of particular interest, rather than traditional power spectral density (PSD) functions [27]. It is well known that in certain cases the expected values of the periodograms converge to the true PSD functions in the limit as $L\to\infty$, but in the applications mentioned above this is not a requirement, or even relevant to the measured performance. Hence, the results presented in this paper focus on the properties of the periodograms given by (54) and (55).

B. Signal Processing Model of the Segmented Quantizer

The proposed segmented quantizer architecture is shown in Figure 12a. Its input is a sequence of B-bit numbers, $x_0[n]$, and its output is a sequence of $B-K$-bit

numbers, $x_K[n]$, where n = 0, 1, 2, …, is the time index of the sequences. The segmented quantizer consists of *K quantization blocks*, each of which quantizes its input by one bit, so the segmented quantizer quantizes K bits overall.[4]

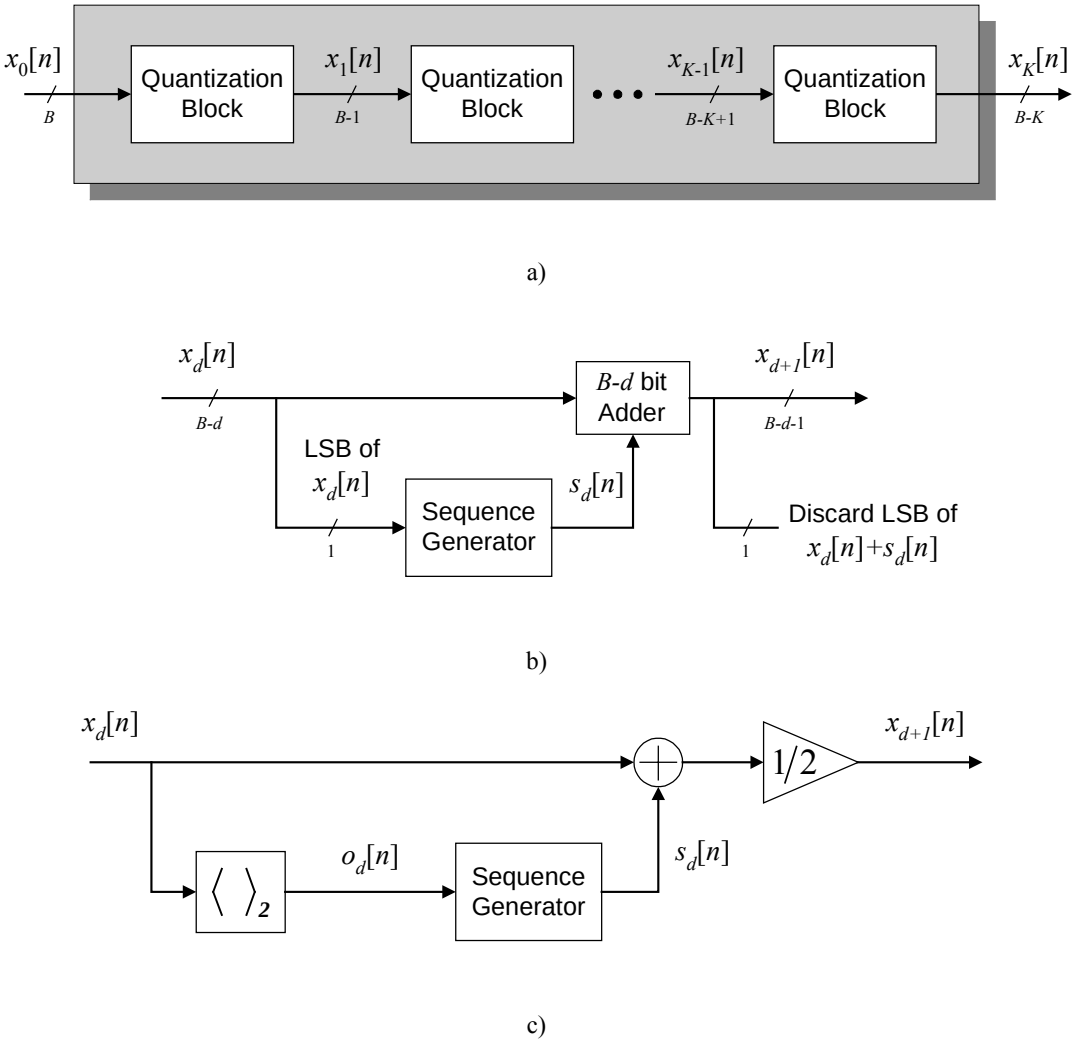


Figure 12: a) High-level block diagram of the segmented quantizer; b) quantization block details; c) signal processing model

The high-level details of each quantization block are shown in Figure 12b and

[4] Quantization blocks that quantize their input sequences by more than one bit could be used. However, it is straightforward to show that this is a trivial extension of the one bit-per-stage case.

the signal-processing model is shown in Figure 12c. Each quantization block generates a *quantization sequence*, $s_d[n]$, with the property that $x_d[n]+s_d[n]$ is an even number for each n, where $x_d[n]$ is the quantization block's input sequence. The quantization block adds $s_d[n]$ to $x_d[n]$ and discards the least significant bit (LSB) to implement the 1-bit quantization.[5] Since $x_d[n]+s_d[n]$ is an even number for each n, its LSB is zero, so discarding the LSB does not incur a truncation error. Hence, the quantization noise of the segmented quantizer is a weighted sum of the $s_d[n]$ sequences:

$$s[n] = \sum_{d=0}^{K-1} 2^d s_d[n]. \tag{56}$$

So far, the only restriction on the $s_d[n]$ sequences is that $x_d[n]+s_d[n]$ must be an even integer for each n and d. This leaves considerable flexibility in the design of the $s_d[n]$ sequences which is exploited in the remainder of the paper to achieve the desired quantization noise properties.

The versions of the segmented quantizer considered in this paper partially exploit this flexibility to have *first-order highpass shaped quantization noise*, i.e., they are designed such that the running sum of each $s_d[n]$ sequence,

$$t_d[n] = \sum_{k=0}^{n} s_d[k]. \tag{57}$$

is bounded over all n and that the estimated power spectrum of $s_d[n]$ has a highpass spectral shape. It follows from (56) that the overall quantization noise, $s[n]$, inherits

[5] Without loss of generality, numbers within the SQ are taken to be integers with a two's-compliment binary number representation.

the spectral shape of the $s_d[n]$ sequences, and similarly that the running sum of the quantization noise,

$$t[n] = \sum_{d=0}^{K-1} 2^d t_d[n], \tag{58}$$

is bounded.

The restriction to first-order highpass shaped quantization noise still leaves flexibility in the design of the $s_d[n]$ sequences. This flexibility is exploited in the remainder of the paper to ensure that $s^p[n]$ for $p = 1, 2, \ldots, h_s$, and $t^p[n]$ for $p = 1, 2, \ldots, h_t$ are free of spurious tones, where h_s and h_t are positive integers. By definition, if $s^p[n]$ and $t^p[n]$ contain spurious tones at a frequency ω_n, then (54) and (55), respectively, are expected to be unbounded in probability at $\omega = \omega_n$ as $L \to \infty$. Therefore, to establish that there are no spurious tones in either $s^p[n]$ or $t^p[n]$, it is sufficient to show that (54) and (55) are bounded in probability for all $|\omega| \leq \pi$ as $L \to \infty$. A spurious tone at $\omega = 0$ is just a dc offset, so this case is excluded from consideration. Theorems 1 and 2 in the next section present sufficient conditions on the $s_d[n]$ sequences for (54) and (55) to be bounded in probability for every $L \geq 1$ and $0 < |\omega| \leq \pi$, thereby ensuring the absence of spurious tones in $s^p[n]$ and $t^p[n]$.

C. Example Segmented Quantizer and Appearance of Spurious Tones

As shown in [28], first-order highpass quantization noise is achieved with quantization blocks that implement

$$s_d[n] = \begin{cases} 0, & x_d[n] = \text{even} \\ r_d[n], & x_d[n] = \text{odd}, \quad t_d[n-1] = 0 \\ 1, & x_d[n] = \text{odd}, \quad t_d[n-1] = -1 \\ -1, & x_d[n] = \text{odd}, \quad t_d[n-1] = 1 \end{cases} \tag{59}$$

where $r_d[n]$ is an independent random sequence that takes on the values 1 and –1 with equal probability. The results presented in [29] imply that neither $s_d[n]$ nor $t_d[n]$ contain spurious tones. Therefore, $s[n]$ and $t[n]$ inherit these properties provided the $r_d[n]$ sequences for $d = 0, \ldots, K-1$ are independent. This is demonstrated by the estimated power spectra shown in Figure 13 which correspond to a simulated segmented quantizer with $K = 16$, $x_0[n] = 2457$, and quantization blocks that implement (59).

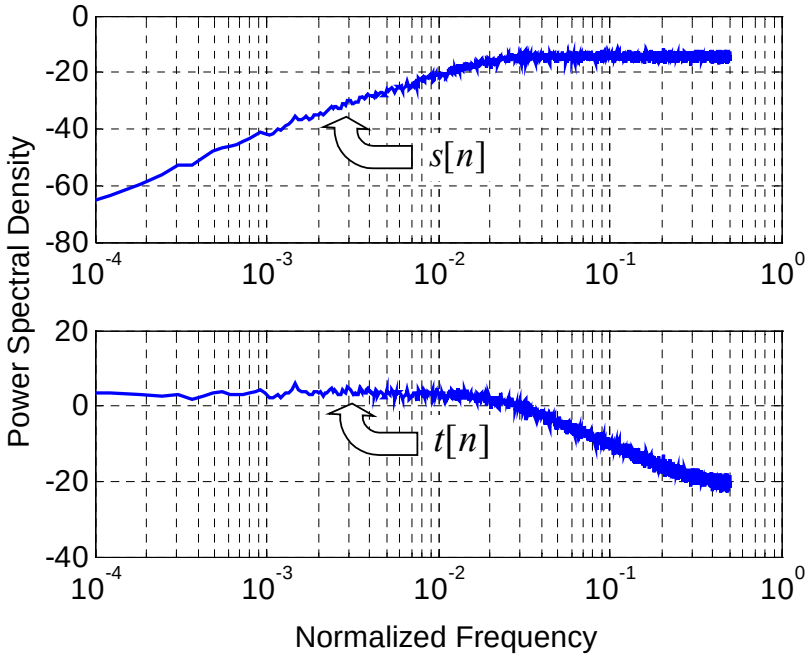


Figure 13: Estimated power spectra of the quantization noise and its running sum for the SQ presented in Section II.

However, if the quantization noise or its running sum is subjected to non-linear

distortion, spurious tones can be induced. For instance, Figure 14 shows the estimated power spectrum of $t^2[n]$ for the simulation example described above. Discrete spikes are evident in the plot, and it can be shown that the spikes grow without bound in proportion to the periodogram length. Therefore, the spikes represent spurious tones. The presence of spurious tones implies that subjecting $t[n]$ to second-order distortion is sufficient to induce spurious tones even though $t[n]$ is known to be free of spurious tones.

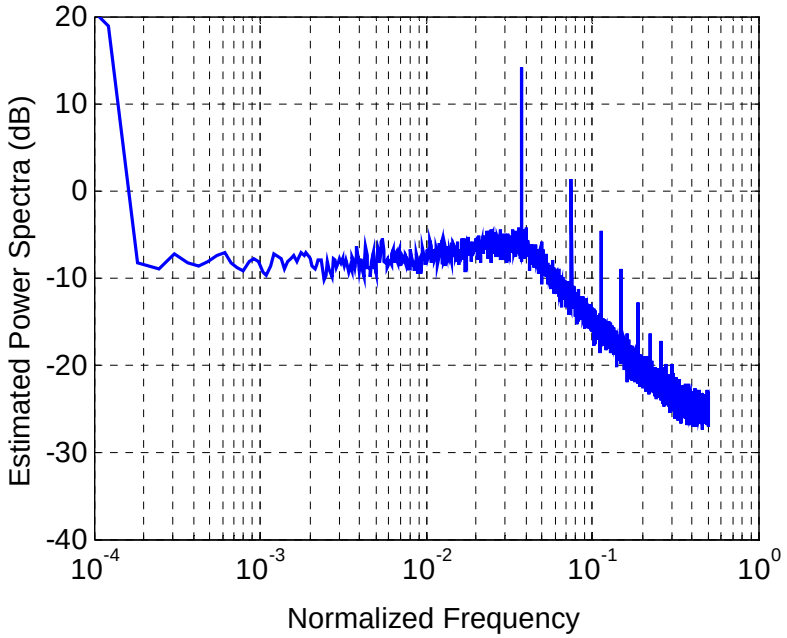


Figure 14: Estimated power spectra of the square of the running sum of the quantization noise for the SQ presented in Section II.

The spur generation mechanism can be understood by considering the first quantization block. Suppose the input to the segmented quantizer is an odd-valued constant and $t_0[n-1] = 0$ for some value of n. Then (59) implies that $(s_0[n], s_0[n+1])$ is either $(-1, 1)$ or $(1, -1)$ depending on the polarity of $r_0[n]$. It follows from (57) that

($t_0[n]$, $t_0[n+1]$) is either (−1, 0) or (1, 0), and, by induction, $t_0[n]$ has the form {…, 0, ±1, 0, ±1, 0, ±1, 0, …}. Therefore, $t_0^2[n]$ has the form {…, 0, 1, 0, 1, 0, 1, 0, …} which is periodic. A similar, but more involved analysis can be used to show that the $t_d^2[n]$ sequences for $d > 0$ also contain periodic components. These periodic components cause the spurious tones visible in Figure 3.

III. Theory for Tone-Free Quantization Sequences

It is assumed throughout the remainder of the paper that the input to the quantizer, $x_0[n]$, is integer-valued and deterministic sequence for $n = 0, 1, \ldots$, and that the segmented quantizer is designed such that the following properties are satisfied:

Property 1: $x_{d+1}[n] = (s_d[n] + x_d[n])/2$ is integer-valued for $n = 0, 1, \ldots$, and $d = 0, 1, \ldots, K - 1$.

Property 2: there exists a positive constant B such that $|t_d[n]| < B$, for $n = 0, 1, 2, \ldots$.

Property 3: $t_d[0] = 0$, and

$$t_d[n] = f\left(t_d[n-1], r_d[n], o_d[n]\right) \tag{60}$$

where f is a deterministic, memoryless function, $\{r_d[n]$, $d = 0, 1, \ldots, K-1$, $n = 1, 2, \ldots\}$ is a set of independent identically distributed (iid) random variables, and

$$o_d[n] = x_d[n] \mod 2 = \begin{cases} 1, & \text{if } x_d[n] \text{ is odd,} \\ 0, & \text{if } x_d[n] \text{ is even,} \end{cases} \tag{61}$$

is called the *parity sequence* of the d^{th} quantization block.

Property 1 and the assumption that $x_0[n]$ is integer-valued imply that $s_d[n]$ is an even integer when $x_d[n]$ is even, and an odd integer otherwise. Therefore, (57) implies that $t_d[n]$ is integer-valued, and Property 2 further implies that it is restricted to a finite set of values. Let $T_1, T_2, \ldots, T_N$ denote these values. Therefore, the function, f, in Property 3 takes on values restricted to the set $\{T_1, T_2, \ldots, T_N\}$.

It follows from Properties 1, 2, and 3 that $x_{d+1}[n]$, $s_d[n]$, and $t_d[n]$, for $d = 0, 1, \ldots, K-1$, and $n = 1, 2, \ldots$, depend only on the set of iid random variables $\{r_d[n], d = 0, 1, \ldots, K-1, n = 0, 1, 2, \ldots\}$ and the deterministic segmented quantizer input sequence, $\{x_0[n], n = 1, 2, \ldots,\}$. Therefore, the sample description space of the underlying probability space is the set of all possible values of the random variables $\{r_d[n], d = 0, 1, \ldots, K-1, \text{ and } n = 0, 1, 2, \ldots\}$.

Equation (57) implies that

$$s_d[n] = t_d[n] - t_d[n-1]. \tag{62}$$

Therefore, it follows from Property 1 that

$$x_d[n] = \left(t_{d-1}[n] - t_{d-1}[n-1] + x_{d-1}[n]\right)/2, \tag{63}$$

for $1 \le d < K$. Recursively substituting (63) into itself and applying (61) yields

$$o_d[n] = \frac{1}{2}\left[x_0[n] + \sum_{k=0}^{d-1} 2^{-k} \left(t_k[n] - t_k[n-1] \right) \right] \bmod 2 . \tag{64}$$

Recursively substituting (60) into itself implies that for any integer $n > 0$,

$$t_d[n] = g_n \left(r_d[n], r_d[n-1], \ldots, r_d[1], o_d[n], o_d[n-1], \ldots, o_d[1] \right) \tag{65}$$

where g_n is a deterministic, memoryless function. Similarly, for any pair of integers $n_2 > n_1 > 0$, recursively substituting (60) into itself $m = n_2 - n_1 - 1$ times implies that

$$t_d[n_2] = h_m \left(t_d[n_1], r_d[n_1+1], r_d[n_1+2], \ldots, r_d[n_2], o_d[n_1+1], o_d[n_1+2], \ldots, o_d[n_2] \right) \tag{66}$$

where h_m is a deterministic, memoryless function.

Repeatedly substituting (64) into (65) to eliminate the variables $\{o_d[n], \ldots, o_d[1]\}$ and then recursively substituting the result into itself to eliminate the variables $\{t_k[m], k = 0, \ldots, d-1, m = 1, \ldots, n\}$ shows that $t_d[n]$ is a random variable that depends only on $x_0[n]$ (which is deterministic), and the random variables $\{r_k[m], k = 0, 1, \ldots, d, m = 1, 2, \ldots, n\}$. This in conjunction with (64) implies that $o_d[n]$ is a random variable that depends only on $x_0[n]$, and the random variables $\{r_k[m], k = 0, 1, \ldots, d-1, m = 1, 2, \ldots, n\}$. In particular since the random sequence $\{o_d[n], n = 0, 1, 2, \ldots\}$ does not depend on the random sequence $\{r_d[n], n = 0, 1, 2, \ldots\}$ and since all the random variables $\{r_k[m] \; d = 0, 1, \ldots, K-1, n = 0, 1, 2, \ldots\}$ are statistically independent by Property 3, it follows that $\{o_d[n], n = 0, 1, 2, \ldots\}$ and $\{r_d[n], n = 0, 1, 2, \ldots\}$ are statistically independent random sequences. By similar reasoning, the random variable $t_d[n]$ is statistically independent of the random variables $\{r_d[m], m=n+1, n+2, \ldots\}$.

Hence, (66) implies that $t_d[n_2]$ conditioned on the random variables $t_d[n_1]$, $o_d[n_1+1]$, $o_d[n_1+2]$, …, $o_d[n_2]$ is a function only of the statistically independent random variables $r_d[n_1]$, $r_d[n_1+1]$, …, $r_d[n_2]$. By definition, for $i \neq j$ the random variables $\{r_i[n_1], r_i[n_1+1], \ldots, r_i[n_2]\}$ are statistically independent of the random variables $\{r_j[n_1], r_j[n_1+1], \ldots, r_j[n_2]\}$. Therefore, for $i \neq j$ the random variables $t_i[n_2]$ and $t_j[n_2]$ conditioned on $t_i[n_1]$, $t_j[n_1]$, $o_i[n_1+1]$, $o_i[n_1+2]$, …, $o_i[n_2]$, $o_j[n_1+1]$, $o_j[n_1+2]$, …, $o_j[n_2]$ are statistically independent. Consequently, for any positive real numbers $p_0, \ldots, p_{K-1}$,

$$\begin{aligned} & E\left[\prod_{j=0}^{K-1} t_j^{p_j}[n_2] \middle| t_d[n_1], o_d[n]; d = 0, \ldots, K-1, n = n_1+1, \ldots, n_2\right] \\ & = \prod_{j=0}^{K-1} E\left[t_j^{p_j}[n_2] \middle| t_d[n_1], o_d[n]; d = 0, \ldots, K-1, n = n_1+1, \ldots, n_2\right] \\ & = \prod_{j=0}^{K-1} E\left[t_j^{p_j}[n_2] \middle| t_j[n_1], o_j[n]; n = n_1+1, \ldots, n_2\right], \end{aligned} \tag{67}$$

where the second equality follows from (60) and the independence of the $\{r_d[n], n = 1, 2, \ldots,\}$ sequences for $d = 0, \ldots, K-1$. This implies that the pmf of the random variable $t_i[n_2]$ conditioned on $t_i[n_1]$, $o_i[n_1+1]$, $o_i[n_1+2]$, …, $o_i[n_2]$ is independent of any additional conditioning by $t_j[n_1]$, $o_j[n_1+1]$, $o_j[n_1+2]$, …, $o_j[n_2]$ for $i \neq j$.

The statistical independence of $o_d[n]$ and $r_d[n]$ together with (60) imply that $\{t_d[n], n = 0, 1, \ldots\}$ is a discrete-valued Markov random sequence conditioned on the sequence $\{o_d[n], n = 0, 1, \ldots\}$. Whenever $x_d[n]$ is odd the one-step state transition matrix for $t_d[n]$ is given by

$$\mathbf{A_o} = \left[P\left\{t_d[n] = T_j \mid t_d[n-1] = T_i, o_d[n] = 1\right\}\right]_{N \times N}. \tag{68}$$

Similarly, whenever $x_d[n]$ is even the one-step state transition matrix for $t_d[n]$ is given by

$$\mathbf{A}_{\mathbf{e}} = \left[P\left\{ t_d[n] = T_j \mid t_d[n-1] = T_i, o_d[n] = 0 \right\} \right]_{N \times N}. \tag{69}$$

The function f in Property 3 is independent of n and d, so neither matrix is a function of n and d.

Equation (62) implies that each possible value of $s_d[n]$ is given by $T_j - T_i$ for some pair of integers i and j, $1 \le i, j \le N$, so

$$P\left\{ s_d[n] = T_j - T_i \middle| t_d[n-1] = T_i, o_d[n] = 1 \right\} = P\left\{ t_d[n] = T_j \middle| t_d[n-1] = T_i, o_d[n] = 1 \right\}. \tag{70}$$

Given that $t_d[n]$ is restricted to N possible values, $s_d[n]$ is restricted to N' possible values where $N' \le N^2$. With identical reasoning to that used to proceed from (63) to (67), it follows that

$$\begin{aligned} &E\left[\prod_{j=0}^{K-1} s_j^{p_j}[n_2] \middle| t_0[n_1], \ldots, t_{K-1}[n_1], o_d[n]; d = 0, \ldots, K-1, n = n_1+1, \ldots, n_2 \right] \\ &= \prod_{j=0}^{K-1} E\left[s_j^{p_j}[n_2] \middle| t_j[n_1], o_j[n]; n = n_1+1, \ldots, n_2 \right]. \end{aligned} \tag{71}$$

Given that $\{t_d[n], n = 0, 1, \ldots\}$ is a discrete-valued Markov random sequence conditioned on the sequence $\{o_d[n], n = 0, 1, \ldots\}$, the conditional probability mass function (pmf) of $t_d[n_2]$ given $t_d[n_1]$ and $o_d[n]$ is equal to the conditional pmf of $t_d[n_2]$ given $t_d[n_1]$, $t_d[n_1-1]$ and $o_d[n]$. Therefore, (62) implies that (71) is equivalent to

$$E\left[\prod_{j=0}^{K-1} s_j^{p_j}[n_2] \middle| s_0[n_1],\ldots,s_{K-1}[n_1],t_0[n_1],\ldots,t_{K-1}[n_1],o_d[n];\right.$$
$$\left. d=0,\ldots,K-1, n=n_1+1,\ldots,n_2\right] = \prod_{j=0}^{K-1} E\left[s_j^{p_j}[n_2] \middle| t_j[n_1],o_j[n];n=n_1+1,\ldots,n_2\right] \tag{72}$$

The following definitions are used by the theorems presented below. In analogy to the matrices $\mathbf{A_o}$ and $\mathbf{A_e}$, let

$$\mathbf{S_o} = \left[P\left\{s_d[n]=S_j \mid t_d[n-1]=T_i, o_d[n]=1\right\}\right]_{N\times N'}, \tag{73}$$

and

$$\mathbf{S_e} = \left[P\left\{s_d[n]=S_j \mid t_d[n-1]=T_i, o_d[n]=0\right\}\right]_{N\times N'}, \tag{74}$$

where $\{S_i,\ 1 \le i \le N'\}$ is the set of all possible values of $s_d[n]$. Property 3 ensures that neither matrix is a function of n and d. It follows from (70) that each non-zero element of $\mathbf{S_o}$ or $\mathbf{S_e}$ is equal to an element in $\mathbf{A_o}$ or $\mathbf{A_e}$, respectively. For example, if $S_k = T_j - T_i$, then the element in the ith row and kth column of $\mathbf{S_o}$ is equal to the element in the ith row and jth column of $\mathbf{A_o}$. In this fashion, once $\mathbf{A_o}$ and $\mathbf{A_e}$ are known, $\mathbf{S_o}$ and $\mathbf{S_e}$ can be deduced.

Let

$$\mathbf{1} \triangleq \begin{bmatrix}1\\ \vdots \\ 1\end{bmatrix}, \qquad \mathbf{t}^{(p)} \triangleq \begin{bmatrix}(T_1)^p\\ \vdots \\ (T_N)^p\end{bmatrix}, \qquad \text{and} \qquad \mathbf{s}^{(p)} \triangleq \begin{bmatrix}(S_1)^p\\ \vdots \\ (S_{N'})^p\end{bmatrix}. \tag{75}$$

Suppose a sequence of vectors, $\mathbf{b}[n] = [b_1[n], \ldots, b_N[n]]^{\mathrm{T}}$ converges to a constant vector, $b\mathbf{1}$, as $n\to\infty$. Then the convergence is said to be *exponential* if there exist con-

stants $C \geq 0$ and $0 \leq \alpha < 1$ such that

$$\left| b_i[n] - b \right| \leq C\alpha^n \tag{76}$$

for all $1 \leq i \leq N$ and $n \geq 0$.

Theorem 1: Suppose that the state transition matrices $\mathbf{A_e}$ and $\mathbf{A_o}$ satisfy

$$\mathbf{A_e A_o} = \mathbf{A_o A_e}, \tag{77}$$

and there exists an integer $h_t \geq 1$ such that for each positive integer $p \leq h_t$

$$\lim_{n\to\infty} \mathbf{A_e}^n \mathbf{t}^{(p)} = b_p \mathbf{1}, \qquad \text{and} \qquad \lim_{n\to\infty} \mathbf{A_o}^n \mathbf{t}^{(p)} = b_p \mathbf{1} \tag{78}$$

where b_p is a constant and the convergence of both vectors is exponential. Then for every $L \geq 1$,

$$E[I_{t^p,L}(\omega)] \leq C(\omega) < \infty \tag{79}$$

for each $0 < |\omega| \leq \pi$. Moreover, the bound $C(\omega)$, which is independent of L, is uniform in ω for all $0 < \varepsilon < |\omega| \leq \pi$.

By Markov's Inequality [30], this immediately leads to,

Corollary 1: Under the assumptions of Theorem 1, $I_{t^p,L}(\omega)$ is bounded in probability for all $L \geq 1$ and for each ω satisfying $0 < |\omega| \leq \pi$.

Proof of Theorem 1: The expectation of $I_{t^p,L}(\omega)$ can be expressed as

$$
\begin{aligned}
E[I_{t^p,L}(\omega)] &= \frac{1}{L}\sum_{n_1=0}^{L-1}\sum_{n_2=0}^{L-1} E\left[t^p[n_1]t^p[n_2]\right]e^{-j\omega(n_1-n_2)} \\
&= \frac{1}{L}\sum_{n_1=0}^{L-1} E\left[t^{2p}[n]\right] + \frac{1}{L}\sum_{\substack{n_1=0 \\ n_1\neq n_2}}^{L-1}\sum_{n_2=0}^{L-1} E\left[t^p[n_1]t^p[n_2]\right]e^{-j\omega(n_1-n_2)} . \qquad (80) \\
&\triangleq J_1 + J_2
\end{aligned}
$$

The notation above means that J_1 and J_2 are defined as the first and second terms, respectively, to the left of the $\triangleq$ symbol. Property 2 states that $|t_d[n]| \leq B$, so it follows from (58) that $t[n] \leq B_1$ for some finite constant B_1. Therefore, $J_1 \leq {B_1}^{2p}$. The crux of the proof is showing that there exists a constant C_{t^p}, positive constants D_1, D_2, and a constant $0 < \alpha < 1$ such that for $n_1 \neq n_2$

$$
\left| E\left[t^p[n_1]t^p[n_2] - C_{t^p}\right]\right| \leq D_1\alpha^{|n_2-n_1|} + D_2\alpha^{n_1}, \qquad (81)
$$

The proof of (81), which is fairly lengthy, will be given later. Here (81) is used to complete the proof of the theorem. From (80), J_2 can be expressed as

$$
\begin{aligned}
J_2 &= \frac{1}{L}\sum_{\substack{n_1=0 \\ n_1\neq n_2}}^{L-1}\sum_{n_2=0}^{L-1}\left(E\left[t^p[n_1]t^p[n_2] - C_{t^p}\right]\right)e^{-j\omega(n_1-n_2)} + \frac{1}{L}\sum_{\substack{n_1=0 \\ n_1\neq n_2}}^{L-1}\sum_{n_2=0}^{L-1} C_{t^p}e^{-j\omega(n_1-n_2)} \\
&\triangleq J_{2,1} + J_{2,2}.
\end{aligned} \qquad (82)
$$

From (81) it is seen that

$$
\begin{aligned}
\left|J_{2,1}\right| &\leq \frac{1}{L}\sum_{\substack{n_1=0 \\ n_1\neq n_2}}^{L-1}\sum_{n_2=0}^{L-1}\left(D_1\alpha^{|n_1-n_2|} + D_2\alpha^{n_1}\right) \\
&\leq \frac{D_1}{L}\sum_{n_1=0}^{L-1}\sum_{n_2=0}^{L-1}\alpha^{|n_1-n_2|} + D_2\sum_{n_1=0}^{L-1}\alpha^{n_1} \qquad (83) \\
&\leq 2\left(D_1+D_2\right)\frac{1-\alpha^L}{1-\alpha} \leq 2\left(D_1+D_2\right)\frac{1}{1-\alpha}
\end{aligned}
$$

and the bound is independent of L. Similarly, $J_{2,2}$ can be bounded by

$$\begin{aligned}
\left|J_{2,2}\right| &\le \frac{\left|C_{t^p}\right|}{L}\left|\left|\sum_{n=0}^{L-1} e^{-j\omega n}\right|^2 - L\right| \\
&\le \frac{\left|C_{t^p}\right|}{L}\left|\left|\frac{1-e^{-j\omega L}}{1-e^{-j\omega}}\right|^2 - L\right| = \frac{\left|C_{t^p}\right|}{L}\left|\left|\frac{\sin(\omega L/2)}{\sin(\omega/2)}\right|^2 - L\right|. \\
&\le \left|C_{t^p}\right|\left(1+\frac{1}{\sin^2(\omega/2)}\right)
\end{aligned} \tag{84}$$

which is finite, independent of L, for each ω satisfying $0 < |\omega| \le \pi$; the bound is uniform for all ω satisfying $0 < \varepsilon < |\omega| \le \pi$ since $\sin(\omega/2) > \sin(\varepsilon/2)$. The result of the theorem then follows from (80) through (84).

To establish (81), it suffices to assume that $n_2 > n_1$. Using (58), $E[t^p[n_2]t^p[n_1]]$ can be expressed as

$$E\left[t^p[n_2]t^p[n_1]\right] = \sum_{c_1=0}^{K-1}\cdots\sum_{c_p=0}^{K-1}\sum_{d_1=0}^{K-1}\cdots\sum_{d_p=0}^{K-1} 2^{c_1+\cdots+c_p+d_1+\cdots+d_p}\, E\left[\prod_{i=1}^{p} t_{c_i}[n_2]\prod_{j=1}^{p} t_{d_j}[n_1]\right]. \tag{85}$$

It is seen that the above expression is a finite sum of terms of the form

$$Q(n_1,n_2) = E\left[\prod_{j=0}^{K-1}\left(t_j^{p_j}[n_2]t_j^{q_j}[n_1]\right)\right], \tag{86}$$

where p_j and q_j are positive integers less than or equal to p. It thus suffices to establish a bound for $Q(n_1, n_2)$ of the form

$$\left|Q(n_1,n_2) - C_3\right| \le C_1\alpha^{n_2-n_1} + C_2\alpha^{n_1}. \tag{87}$$

The right side of (86) is computed by conditional expectation as follows

$$Q(n_1,n_2) = E\left\{\prod_{i=0}^{K-1} t_i^{p_i}[n_1] E\left(\prod_{j=0}^{K-1} t_j^{q_j}[n_2] \middle| t_d[n_1], o_d[n], d=0,1,\ldots,K-1, n=n_1+1,\ldots,n_2\right)\right\}. \quad (88)$$

Substituting (67) into the inner conditional expectation of (88) yields

$$Q(n_1,n_2) = E\left\{\prod_{j=0}^{K-1}\left(t_j^{p_j}[n_1] E\left[t_j^{q_j}[n_2] \middle| t_j[n_1], o_j[n], n=n_1+1,\ldots,n_2\right]\right)\right\} \quad (89)$$

Since $\{t_d[n],\ n = 0,\ 1,\ \ldots\}$ is a Markov process for any given parity sequence, $\{o_d[n] = o_{d,n},\ n = 0,\ 1,\ \ldots\}$ where $o_{d,n} \in \{0,1\}$, it follows from (68) and (69) that the m-step state transition matrix corresponding to $t_d[n]$ from time n to time $n + m$ can be written as

$$\mathbf{A}_d[n,m] = \prod_{k=n+1}^{n+m}\left[\mathbf{A}_\mathbf{o} o_{d,k} + \mathbf{A}_\mathbf{e}\left(1-o_{d,k}\right)\right], \quad (90)$$

where $\mathbf{A}_d[n, m]$ is an $N \times N$ matrix with elements of the form

$$P\left\{t_d[n+m] = T_j \middle| t_d[n] = T_i, o_d[n+1] = o_{d,n+1}, o_d[n+2] = o_{d,n+2}, \ldots, o_d[n+m] = o_{d,n+m}\right\}. \quad (91)$$

Since $o_{d,n}$ is either 1 or 0 for each n, (77) can be used to write (90) as

$$\mathbf{A}_d[n,m] = \mathbf{A}_\mathbf{e}^{\,y_m}\mathbf{A}_\mathbf{o}^{\,m-y_m} = \mathbf{A}_\mathbf{o}^{\,m-y_m}\mathbf{A}_\mathbf{e}^{\,y_m}, \qquad \text{where} \quad y_m = \sum_{k=n+1}^{n+m} o_{d,k}. \quad (92)$$

By definition, $y_m \geq m/2$ or $m - y_m \geq m/2$ depending on the given parity sequence. It follows from the exponential convergence of (78) that there exists positive numbers $C_{p,e}$ and $C_{p,o}$ and positive numbers $\alpha_{p,e}$ and $\alpha_{p,o}$ less than unity such that each element of

$$\mathbf{A}_{\mathbf{e}}{}^{y_m}\mathbf{t}^{(p)} - b_p\mathbf{1} \tag{93}$$

is less than $C_{p,e}\alpha_{p,e}{}^{m/2}$ for $y_m \geq m/2$, and each element of

$$\mathbf{A}_{\mathbf{o}}{}^{m-y_m}\mathbf{t}^{(p)} - b_p\mathbf{1} \tag{94}$$

is less than $C_{p,o}\alpha_{p,o}{}^{m/2}$ for $m - y_m \geq m/2$.

The matrices $\mathbf{A}_{\mathbf{o}}^{m-y_m}$ and $\mathbf{A}_{\mathbf{e}}^{y_m}$ are stochastic matrices, so $\mathbf{A}_{\mathbf{o}}^{m-y_m}\mathbf{1} = \mathbf{1}$, $\mathbf{A}_{\mathbf{e}}^{y_m}\mathbf{1} = \mathbf{1}$ and

$$\mathbf{A}_{\mathbf{o}}{}^{m-y_m}\left(\mathbf{A}_{\mathbf{e}}{}^{y_m}\mathbf{t}^{(p)} - b_p\mathbf{1}\right) = \mathbf{A}_{\mathbf{o}}{}^{m-y_m}\mathbf{A}_{\mathbf{e}}{}^{y_m}\mathbf{t}^{(p)} - b_p\mathbf{1}, \tag{95}$$

$$\mathbf{A}_{\mathbf{e}}{}^{y_m}\left(\mathbf{A}_{\mathbf{o}}{}^{m-y_m}\mathbf{t}^{(p)} - b_p\mathbf{1}\right) = \mathbf{A}_{\mathbf{e}}{}^{y_m}\mathbf{A}_{\mathbf{o}}{}^{m-y_m}\mathbf{t}^{(p)} - b_p\mathbf{1}. \tag{96}$$

Since the elements of the vectors in (93) and (94) are exponentially bounded, the same must be true for the vectors in (95) and (96). From (92) it follows that the right side of either (95) or (96) is equal to

$$\mathbf{A}_d[n,m]\mathbf{t}^{(p)} - b_p\mathbf{1}. \tag{97}$$

Therefore, in general each element of (97) has a magnitude less than $C\alpha^{m/2}$ where C=max$\{C_{g,e}, C_{g,o}\}$ and α=max$\{\alpha_{g,e}, \alpha_{g,o}\}$, which implies that

$$E\left[t_d^p[n+m] \mid t_d[n], o_d[n+j] = o_{d,n+j}, j = 1,\ldots,m\right] \to b_p \tag{98}$$

as $m \to \infty$ uniformly in n where the convergence is also exponential. This result is independent of the given deterministic sequence $\{o_{d,n}, n = 0, 1, \ldots\}$, so it implies that

$$E\left[t_d^p[n+m] \mid t_d[n], o_d[n+j], j = 1,\ldots,m\right] \to b_p \tag{99}$$

almost surely as $m \to \infty$ uniformly in n where the convergence is also exponential.

Thus, the inner conditional expectation in (89) converges exponentially to b_{r_j} as $n_2 - n_1 \to \infty$ with probability one so that

$$Q(n_1, n_2) \to \prod_{j=0}^{K-1} b_{q_j} E\left\{\prod_{i=0}^{K-1} t_i^{p_i}[n_1]\right\}. \tag{100}$$

More precisely, the exponential convergence of (100) implies that for every $n_2 > n_1$

$$\left| E\left[t_j^{q_j}[n_2] \,|\, t_j[n_1], o_j[n], n = n_1 + 1, \ldots, n_2 \right] - b_{q_j} \right| \le C(q_j)\alpha^{n_2 - n_1}. \tag{101}$$

with probability one where $C(q_j)$ is a constant that depends on q_j. For every $n_2 > n_1$

$$\begin{aligned} &\left| Q(n_1, n_2) - \prod_{j=0}^{K-1} b_{q_j} E\left\{\prod_{i=0}^{K-1} t_i^{p_i}[n_1]\right\}\right| \\ &\quad \le E\left\{\prod_{j=0}^{K-1} \left| t_j[n_1] \right|^{p_j} \left| E\left[t_j^{q_j}[n_2] \,|\, t_j[n_1], o_j[n], n = n_1 + 1, \ldots, n_2 \right] - b_{q_j} \right|\right\}. \\ &\quad \le \prod_{j=0}^{K-1} C(q_j) B^{p_j} \alpha^{n_2 - n_1} \triangleq C_1 \alpha^{n_2 - n_1} \end{aligned} \tag{102}$$

where B is given from Property 2. By similar reasoning, it can be established that

$$\left| \mathrm{E}\left\{\prod_{j=0}^{K-1} t_j^{q_j}[n_1]\right\} - \prod_{j=0}^{K-1} b_{q_j} \right| \le C_2 \alpha^{n_1} \tag{103}$$

Hence, the above two bounds imply there exist positive constants C_1 and C_2 such that for all $n_2 > n_1$

$$\begin{aligned}
&\left| Q(n_1,n_2) - \prod_{i=0}^{K-1} b_{p_i} \prod_{j=0}^{K-1} b_{q_j} \right| \\
&\quad \le \left| Q(n_1,n_2) - E\left\{ \prod_{i=0}^{K-1} t_i^{p_i}[n_1] \right\} \prod_{j=0}^{K-1} b_{q_j} \right| + \left| E\left\{ \prod_{i=0}^{K-1} t_i^{p_i}[n_1] \right\} \prod_{j=0}^{K-1} b_{q_j} - \prod_{i=0}^{K-1} b_{p_i} \prod_{j=0}^{K-1} b_{q_j} \right|. \quad (104) \\
&\quad \le C_1 \alpha^{n_2 - n_1} + C_2 \alpha^{n_1}.
\end{aligned}$$

Consequently, there exists a constant C_3 such that

$$\left| Q(n_1,n_2) - C_3 \right| \le C_1 \alpha^{n_2 - n_1} + C_2 \alpha^{n_1} \quad (105)$$

which is of the required form.

■

Theorem 2: Suppose that the state transition matrices $\mathbf{A_e}$ and $\mathbf{A_o}$ satisfy

$$\mathbf{A_e A_o} = \mathbf{A_o A_e}, \quad (106)$$

and there exists an integer $h_s \ge 1$ such that for each positive integer $p \le h_s$, the sequence transition matrices $\mathbf{S_e}$ and $\mathbf{S_o}$ satisfy

$$\lim_{n\to\infty} \mathbf{A_e}^n \mathbf{S_e} \mathbf{s}^{(p)} = \lim_{n\to\infty} \mathbf{A_e}^n \mathbf{S_o} \mathbf{s}^{(p)} = \lim_{n\to\infty} \mathbf{A_o}^n \mathbf{S_e} \mathbf{s}^{(p)} = \lim_{n\to\infty} \mathbf{A_o}^n \mathbf{S_o} \mathbf{s}^{(p)} = c_p \mathbf{1}, \quad (107)$$

where c_p is a constant and the convergence of all vectors are exponential. Then for every $L \ge 1$,

$$E[I_{s^p,L}(\omega)] \le D(\omega) < \infty \quad (108)$$

for each $0 < |\omega| \le \pi$. Moreover, the bound $D(\omega)$, which is independent of L, is uniform in ω for all $0 < \varepsilon < |\omega| \le \pi$.

By Markov's Inequality, this immediately leads to,

Corollary 2: Under the assumptions of Theorem 2, $I_{s^p,L}(\omega)$ is bounded in probability for all $L \geq 1$ and for each ω satisfying $0 < |\omega| \leq \pi$.

Proof of Theorem 2: The proof is similar to that of Theorem 1, so only the non-trivial differences with respect to the proof of Theorem 1 are presented.

Similarly to the proof of Theorem 1, it is necessary to show that

$$E\left[s_d^p[n+m] \,|\, t_d[n], o_d[n+j], j = 1, \ldots, m \right] \rightarrow c_p \tag{109}$$

almost surely as $m \rightarrow \infty$ uniformly in n where the convergence is also exponential. With this result and $s_d[n]$, c_p, and (72) playing the roles of $t_d[n]$, b_p, and (67) in the proof of Theorem 1, respectively, the proof of Theorem 2 is almost identical that of Theorem 1. Therefore, it is sufficient to prove (109).

Since the random variables $t_d[n-1]$ and $o_d[n]$ are statistically independent, for any given parity sequence, $\{o_d[n] = o_{d,n},\ n = 0, 1, \ldots\}$ where $o_{d,n} \in \{0,1\}$, it follows from (73), (74), and (91) that

$$\mathbf{S}_d[n, m+1] = \mathbf{A}_d[n, m]\left[\mathbf{S}_\mathbf{o} o_{d,n+m+1} + \mathbf{S}_\mathbf{e} \left(1 - o_{d,n+m+1} \right) \right], \tag{110}$$

where $\mathbf{S}_d[n, m+1]$ is an $N \times N'$ matrix with elements of the form

$$P\left\{ s_d[n+m+1] = S_j \,\middle|\, t_d[n] = T_i, o_d[n+1] = o_{d,n+1}, \ldots, o_d[n+m+1] = o_{d,n+m+1} \right\}, \tag{111}$$

where i is the row index and j is the column index. By similar reasoning to that used

in the proof of Theorem 1, (106) and (107) together imply that there exists a positive number D and a positive number β less than unity such that each element of the vector

$$\mathbf{S}_d[n, m+1]\mathbf{s}^{(p)} - c_p\mathbf{1}, \tag{112}$$

has a magnitude less than $D\cdot\beta^{m/2}$. Thus, (112) implies that

$$E\left[s_d^p[n+m] \,|\, t_d[n], o_d[n+j] = o_{d,n+j}, j = 1,\ldots,m \right] \to c_p \tag{113}$$

as $m \to \infty$ uniformly in n where the convergence is also exponential. This result is independent of the given deterministic sequence $\{o_{d,n}, n = 0, 1, \ldots\}$, so it implies that (109) holds almost surely as $m \to \infty$ uniformly in n where the convergence is also exponential.

■

IV. A Segmented Quantizer that Satisfies Theorems 1 and 2

A. Verification of Example Matrices

Matrices $\mathbf{A_e}$, $\mathbf{A_o}$, $\mathbf{S_e}$, and $\mathbf{S_o}$ which can be used with the segmented quantizer to generate quantized sequences and satisfy the conditions of Theorems 1 and 2 for $h_t = 3$ and $h_s = 5$ are presented in this section.

For a state $t_d[n]$ whose possible values are $\{-2, -1, 0, 1, 2\}$, define

$$\mathbf{t}^{(p)} = \left[(-2)^p \quad (-1)^p \quad 0 \quad 1^p \quad 2^p \right]^T, \tag{114}$$

and the proposed state transition matrices as

$$\mathbf{A}_\mathbf{o} = \begin{bmatrix} 0 & 3/4 & 0 & 1/4 & 0 \\ 3/16 & 0 & 3/4 & 0 & 1/16 \\ 0 & 1/2 & 0 & 1/2 & 0 \\ 1/16 & 0 & 3/4 & 0 & 3/16 \\ 0 & 1/4 & 0 & 3/4 & 0 \end{bmatrix}, \quad \text{and} \quad \mathbf{A}_\mathbf{e} = \begin{bmatrix} 1/4 & 0 & 3/4 & 0 & 0 \\ 0 & 5/8 & 0 & 3/8 & 0 \\ 1/8 & 0 & 3/4 & 0 & 1/8 \\ 0 & 3/8 & 0 & 5/8 & 0 \\ 0 & 0 & 3/4 & 0 & 1/4 \end{bmatrix}. \quad (115)$$

From (62) all possible $s_d[n]$ values are $\{-4, -3, -2, -1, 0, 1, 2, 3, 4\}$, and further define

$$\mathbf{s}^{(p)} = \begin{bmatrix} (-4)^p & (-3)^p & (-2)^p & (-1)^p & 0 & 1^p & 2^p & 3^p & 4^p \end{bmatrix}^T. \quad (116)$$

Applying (70) yields

$$\mathbf{S}_\mathbf{o} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 3/4 & 0 & 1/4 & 0 \\ 0 & 0 & 0 & 3/16 & 0 & 3/4 & 0 & 1/16 & 0 \\ 0 & 0 & 0 & 1/2 & 0 & 1/2 & 0 & 0 & 0 \\ 0 & 1/16 & 0 & 3/4 & 0 & 3/16 & 0 & 0 & 0 \\ 0 & 1/4 & 0 & 3/4 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad \text{and}$$

$$\mathbf{S}_\mathbf{e} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1/4 & 0 & 3/4 & 0 & 0 \\ 0 & 0 & 0 & 0 & 5/8 & 0 & 3/8 & 0 & 0 \\ 0 & 0 & 1/8 & 0 & 3/4 & 0 & 1/8 & 0 & 0 \\ 0 & 0 & 3/8 & 0 & 5/8 & 0 & 0 & 0 & 0 \\ 0 & 0 & 3/4 & 0 & 1/4 & 0 & 0 & 0 & 0 \end{bmatrix}. \quad (117)$$

Multiplying the matrices in either order yields

$$\mathbf{A}_\mathbf{e}\mathbf{A}_\mathbf{o} = \mathbf{A}_\mathbf{o}\mathbf{A}_\mathbf{e} = \begin{bmatrix} 0 & 9/16 & 0 & 7/16 & 0 \\ 9/64 & 0 & 3/4 & 0 & 7/64 \\ 0 & 1/2 & 0 & 1/2 & 0 \\ 7/64 & 0 & 3/4 & 0 & 9/64 \\ 0 & 7/16 & 0 & 9/16 & 0 \end{bmatrix}, \quad (118)$$

so the matrices commute. Direct computation reveals that the eigenvectors of both $\mathbf{A}_\mathbf{e}$

and $\mathbf{A_o}$ are linearly independent, and therefore $\mathbf{A_e}$ and $\mathbf{A_o}$ are diagonalizable [31]. Specifically, $\mathbf{A_e}^n = \mathbf{V_e}\mathbf{\Lambda_e}^n\mathbf{V_e}^{-1}$, where

$$\mathbf{\Lambda_e}^n = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1/4^n & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1/4^n \end{bmatrix}, \quad \mathbf{V_e} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 \\ 1 & 0 & -1/3 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 \\ 1 & -1 & 1 & 0 & 0 \end{bmatrix},$$
$$\text{and} \quad \mathbf{V_e}^{-1} = \begin{bmatrix} 1/8 & 0 & 3/4 & 0 & 1/8 \\ 1/2 & 0 & 0 & 0 & -1/2 \\ 3/8 & 0 & -3/4 & 0 & 3/8 \\ 0 & 1/2 & 0 & 1/2 & 0 \\ 0 & -1/2 & 0 & 1/2 & 0 \end{bmatrix}, \tag{119}$$

and $\mathbf{A_o}^n = \mathbf{V_o}\mathbf{\Lambda_o}^n\mathbf{V_o}^{-1}$, where

$$\mathbf{\Lambda_o}^n = \begin{bmatrix} (-1)^n & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & (-1/4)^n & 0 & 0 \\ 0 & 0 & 0 & 1/4^n & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{V_o} = \begin{bmatrix} 1 & 1 & 1 & -1 & 1 \\ -1 & 1 & -1/2 & -1/2 & 0 \\ 1 & 1 & 0 & 0 & -1/3 \\ -1 & 1 & 1/2 & 1/2 & 0 \\ 1 & 1 & -1 & 1 & 1 \end{bmatrix},$$
$$\text{and} \quad \mathbf{V_o}^{-1} = \begin{bmatrix} 1/16 & -1/4 & 3/8 & -1/4 & 1/16 \\ 1/16 & 1/4 & 3/8 & 1/4 & 1/16 \\ 1/4 & -1/2 & 0 & 1/2 & -1/4 \\ -1/4 & -1/2 & 0 & 1/2 & 1/4 \\ 3/8 & 0 & -3/4 & 0 & 3/8 \end{bmatrix}. \tag{120}$$

By inspection of (119), $\mathbf{\Lambda_e}^n$ converges to

$$\mathbf{\Lambda}_{\mathbf{e},1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{121}$$

The vector given by $\mathbf{V}_\mathbf{e}\mathbf{\Lambda}_{\mathbf{e},1}^n\mathbf{V}_\mathbf{e}^{-1}\mathbf{t}^{(p)}$ is equal to $b_p\mathbf{1}$, where b_p = 0, 1 and 0 for p = 1, 2 and 3 respectively, which is of the form required by Theorem 1. To show exponential convergence, consider

$$\begin{aligned} \left\|\mathbf{A}_\mathbf{e}^n\mathbf{t}^{(p)} - b_p\mathbf{1}\right\| &= \left\|\left(\mathbf{A}_\mathbf{e}^n - \mathbf{V}_\mathbf{e}\mathbf{\Lambda}_{\mathbf{e},1}\mathbf{V}_\mathbf{e}^{-1}\right)\mathbf{t}^{(p)}\right\| \\ &\le \left\|\mathbf{A}_\mathbf{e}^n - \mathbf{V}_\mathbf{e}\mathbf{\Lambda}_{\mathbf{e},1}\mathbf{V}_\mathbf{e}^{-1}\right\|\left\|\mathbf{t}^{(p)}\right\| \end{aligned}, \tag{122}$$

where $\|\ \|$ is the l_2 norm, and p = 1, 2 or 3. Evaluating $\|\mathbf{t}^{(p)}\|$ for p = 3, and $\|\mathbf{A}_\mathbf{e}^n - \mathbf{V}_\mathbf{e}\mathbf{\Lambda}_{\mathbf{e},1}\mathbf{V}_\mathbf{e}^{-1}\|$ yields $\sqrt{130}$ and $\sqrt{2}\left(1/4\right)^n$ respectively therefore the right side of (122) is equal to

$$\sqrt{260}\left(1/4\right)^n \tag{123}$$

and therefore each element of the vector given by $\mathbf{A}_\mathbf{e}^n\mathbf{t}^{(p)} - b_p\mathbf{1}$ converges exponentially to zero.

By inspection of (120), $\mathbf{\Lambda}_\mathbf{o}^n$ does not converge, however it is sufficient to show that the vector $\mathbf{V}_\mathbf{o}\mathbf{\Lambda}_\mathbf{o}^n\mathbf{V}_\mathbf{o}^{-1}\mathbf{t}^{(p)}$ converges. Consider $\mathbf{A}_\mathbf{o}^n = \mathbf{V}_\mathbf{o}\mathbf{\Lambda}_{\mathbf{o},1}^n\mathbf{V}_\mathbf{o}^{-1} + \mathbf{V}_\mathbf{o}\mathbf{\Lambda}_{\mathbf{o},2}^n\mathbf{V}_\mathbf{o}^{-1}$ where

$$\boldsymbol{\Lambda}_{\mathbf{o},1}^{n} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & (-1/4)^n & 0 & 0 \\ 0 & 0 & 0 & 1/4^n & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad \text{and} \quad \boldsymbol{\Lambda}_{\mathbf{o},2}^{n} = \begin{bmatrix} (-1)^n & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (124)$$

Multiplying $\mathbf{V}_\mathbf{o}\boldsymbol{\Lambda}_{\mathbf{o},2}^{n}\mathbf{V}_\mathbf{o}^{-1}$ by $\mathbf{t}^{(p)}$ for p = 1, 2 or 3 results in a vector with all zero elements for all $n \geq 1$. Therefore, for all $n \geq 1$ and p = 1, 2 or 3, $\mathbf{A}_\mathbf{o}^{n}\mathbf{t}^{(p)} = \mathbf{V}_\mathbf{o}\boldsymbol{\Lambda}_{\mathbf{o},1}^{n}\mathbf{V}_\mathbf{o}^{-1}\mathbf{t}^{(p)}$. By inspection, $\boldsymbol{\Lambda}_{\mathbf{o},1}^{n}$ converges to

$$\boldsymbol{\Lambda}_{\mathbf{o},3} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (125)$$

The vector given by $\mathbf{V}_\mathbf{o}\boldsymbol{\Lambda}_{\mathbf{o},3}\mathbf{V}_\mathbf{o}^{-1}\mathbf{t}^{(p)}$ is equal to $b_p\mathbf{1}$, where b_p = 0, 1 and 0 for p = 1, 2 and 3 respectively. Replacing $\mathbf{A}_\mathbf{e}^{n}, \mathbf{V}_\mathbf{e}, \boldsymbol{\Lambda}_{\mathbf{e},1}$, and $\mathbf{V}_\mathbf{e}^{-1}$ in (122) with $\mathbf{A}_\mathbf{o}^{n}, \mathbf{V}_\mathbf{o}, \boldsymbol{\Lambda}_{\mathbf{o},3}$, and $\mathbf{V}_\mathbf{o}^{-1}$ respectively shows that $\|\mathbf{A}_\mathbf{o}{}^{n}\mathbf{t}^{(p)} - b_p\mathbf{1}\|$ converges exponentially to $b_p\mathbf{1}$. Therefore the state transition matrices given by (115) satisfy the conditions of Theorem 1 for h_t = 3.

Using the decomposition in (119) and (120) and the sequence transition matrices given by (117), it can be shown by direct computation that $\mathbf{A}_\mathbf{o}^{n}\mathbf{S}_\mathbf{e}\mathbf{s}^{(p)}, \mathbf{A}_\mathbf{o}^{n}\mathbf{S}_\mathbf{o}\mathbf{s}^{(p)}, \mathbf{A}_\mathbf{e}^{n}\mathbf{S}_\mathbf{e}\mathbf{s}^{(p)}$ and $\mathbf{A}_\mathbf{e}^{n}\mathbf{S}_\mathbf{o}\mathbf{s}^{(p)}$ converges to $c_p\mathbf{1}$, where c_p = 0, 1.5, 0, 6, and 0 for p = 1, 2, 3, 4 and 5 respectively. Furthermore, the convergence of each vector at index n can be bounded using (122), replacing $\|\mathbf{t}^{(p)}\|$ alternately with $\|\mathbf{S}_\mathbf{e}\mathbf{s}^{(p)}\|$ and

$\|\mathbf{S_o s}^{(p)}\|$, which implies that the convergence of $\mathbf{A}_\mathbf{o}^n\mathbf{S_e s}^{(p)}, \mathbf{A}_\mathbf{o}^n\mathbf{S_o s}^{(p)}, \mathbf{A}_\mathbf{e}^n\mathbf{S_e s}^{(p)}$ and $\mathbf{A}_\mathbf{e}^n\mathbf{S_o s}^{(p)}$ are exponential. Therefore, the matrices $\mathbf{A_e}$, $\mathbf{A_o}$, $\mathbf{S_e}$, and $\mathbf{S_o}$ given in (115) and (117) also satisfy the conditions of Theorem 2 for $h_s = 5$.

B. Simulation Results and Comparison to a ΔΣ Modulator

The segmented quantizer presented above performs first-order quantization noise shaping. Therefore, it is reasonable to compare its quantization noise characteristics to those of a first-order ΔΣ modulator of the type shown in Figure 15. The ΔΣ modulator consists of a discrete-time integrator and a mid-tread quantizer enclosed in a negative feedback loop. A random independent, identically distributed (iid) dither sequence, $d[n]$, is added to the output of the discrete-time integrator prior to the quantizer to ensure that the quantization noise sequence introduced by the quantizer is white (and therefore free of spurious tones) [32]. The quantizer implements

$$x_k[n] = \left\lfloor \frac{u[n]}{2^K} + \frac{1}{2} \right\rfloor,$$

where $\lfloor\ \rfloor$ is the floor function, and the dither sequence has a triangular pmf with support on $\{0, 2^{K+1} - 2\}$.

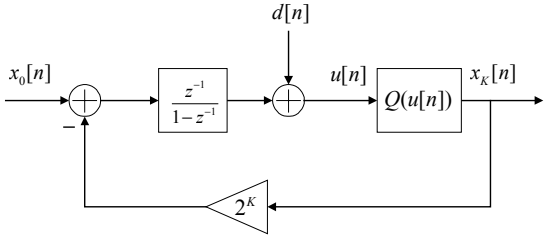
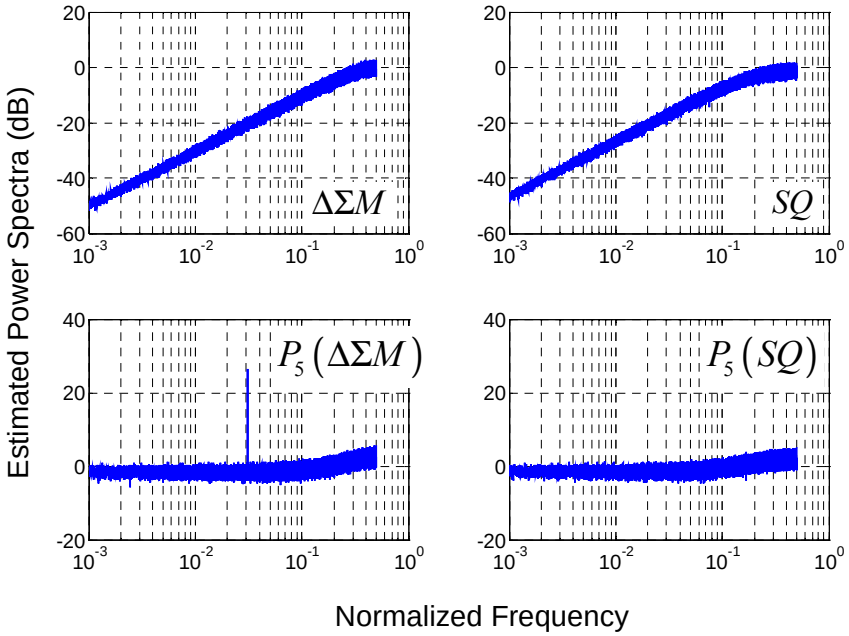
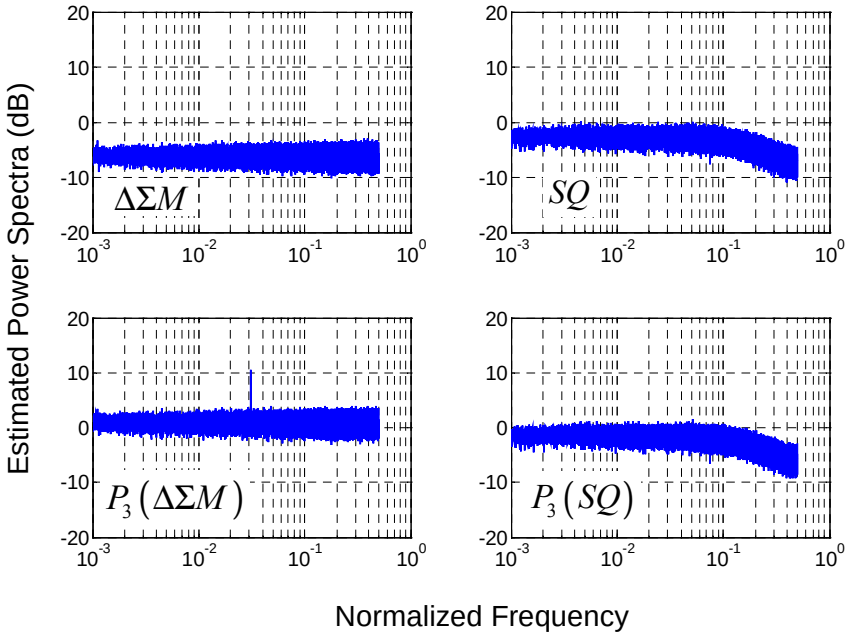


Figure 15: A first-order ΔΣ modulator.



a)



b)

Figure 16: Estimated power spectra of a) the quantization noise sequences, and b) the running sums of the quantization noise sequences of the first-order ΔΣ modulator and the segmented quantizer presented in Section IV before and after application of non-linear distortion.

Simulation results for the segmented quantizer presented above and the ΔΣ modulator with $K = 16$ and a constant input of $x_0[n] = 2048$ are shown in Figure 16. The quantization noise, as well as its running sum for both the segmented quantizer and the ΔΣ modulator are subjected to the following distortion polynomials,

$$\begin{aligned} P_3\left(t[n]\right) &= 0.15\left(t[n]\right)^3 + 0.32\left(t[n]\right)^2 + 0.99\left(t[n]\right) - 0.23 \\ P_5\left(s[n]\right) &= 0.32\left(s[n]\right)^5 - 0.27\left(s[n]\right)^4 - 0.64\left(s[n]\right)^3 + 0.12\left(s[n]\right)^2 + 1.03\left(s[n]\right) + 0.13. \end{aligned} \tag{126}$$

Figure 16 shows the estimated power spectra of the quantization noise and integrated quantization noise before and after application of the distortion polynomials. The estimated power spectra of the sequences, $t^p[n]$ or $s^p[n]$, are taken to be the average of the periodograms of the *M windowed* sequences, $t^p[n - kL]w[n - kL]$ and $s^p[n - kL]w[n - kL]$, for $k = 1, 2, \ldots, M$, where $w[n]$ is a Hanning window of length L. As expected from the theoretical results presented above, no spurious tones are apparent in the figures for the segmented quantizer before or after application of the distortion polynomials. In contrast, spikes, which imply the presence of spurious tones, are evident in the estimated power spectra of the quantization noise from the ΔΣ modulator after application of the distortion polynomials.

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which forms the basis of this paper. Andrea Panigada contributed to the theorem statements, and Elias Masry contributed to the structure of the proofs.

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Chapter 3 : A Wideband 2.4GHz Delta-Sigma Fractional-*N* PLL with Calibrated Phase Noise Cancellation

ABSTRACT

A calibration technique applied to a phase noise canceling fractional-*N* phase-locked loop (PLL) is presented and demonstrated as an enabling component in a wideband, low power CMOS delta-sigma fractional-*N* PLL. The prototype has a measured bandwidth of greater than 730kHz with a 12MHz reference frequency. The PLL is demonstrated with the technique enabled over all Bluetooth channels from 2.402GHz to 2.480GHz and is found to have a worst-case phase noise of –101dBc/Hz and –124dBc/Hz at 100kHz and 3MHz frequency offset from the carrier respectively. With the exception of the reference spur, the spurious tones are less than –57dBc at 2MHz offset, and –62dBc at 3MHz or greater offset. The calibration loop settles in less than 35μs, enabling its use as a background technique for any wireless application. The core PLL circuitry consumes 20.9mA from a 1.8V supply. The IC is fabricated in a 0.18μm mixed-signal CMOS technology, and has a die size of 2.2mm × 2.2mm.

I. INTRODUCTION

This paper presents a calibration technique applicable for use in phase noise canceling Fractional-*N* Phase-locked Loops (PLL) that improves the quality of phase noise cancellation and has fast transient performance. This, along with low-power circuit architectures, makes it practical to implement a low power, fully integrated fractional-*N* PLL. This enhancement is demonstrated in a CMOS Delta-Sigma (ΔΣ) frac-

tional-*N* PLL for operation in the 2.4GHz ISM band. The technique enables the fractional-*N* PLL to achieve the required phase noise for Bluetooth with a bandwidth of 730kHz and a reference of 12MHz without incurring either increased phase noise or power consumption that results from the design of wide bandwidth PLLs. The wide bandwidth makes it possible to integrate a passive 2^{nd} order loop filter on chip [33], which does not suffer from the increased noise inherent to an integrated active loop filter [34]. Moreover, the wide bandwidth also reduces the sensitivity of the voltage-controlled oscillator (VCO) to pulling [35], and attenuates the $1/f^2$ and $1/f^3$ phase noise from the VCO within the PLL loop bandwidth.

The presented calibration technique differs from current techniques in that the existing PLL loop is modified so that minimal extra circuitry is required for calibration. In addition, the calibration circuitry is an analog, continuous-time technique, and avoids many of the problems of existing techniques, such as reference clock feedthrough from sampling the loop filter voltage, and the low calibration loop bandwidth required to filter quantization noise added during the calibration process [36]. The calibration technique demonstrated in this paper has a wide bandwidth and thus fast settling time. The resulting improvement in the quality of phase noise cancellation allows for enhancements to be made, such as reducing the reference frequency, which lowers the power consumption of the digital logic at the cost of increased phase noise. A dynamic bias technique allows the charge pump to operate with significantly high output current to meet circuit noise requirements without dissipating constant power in the bias network.

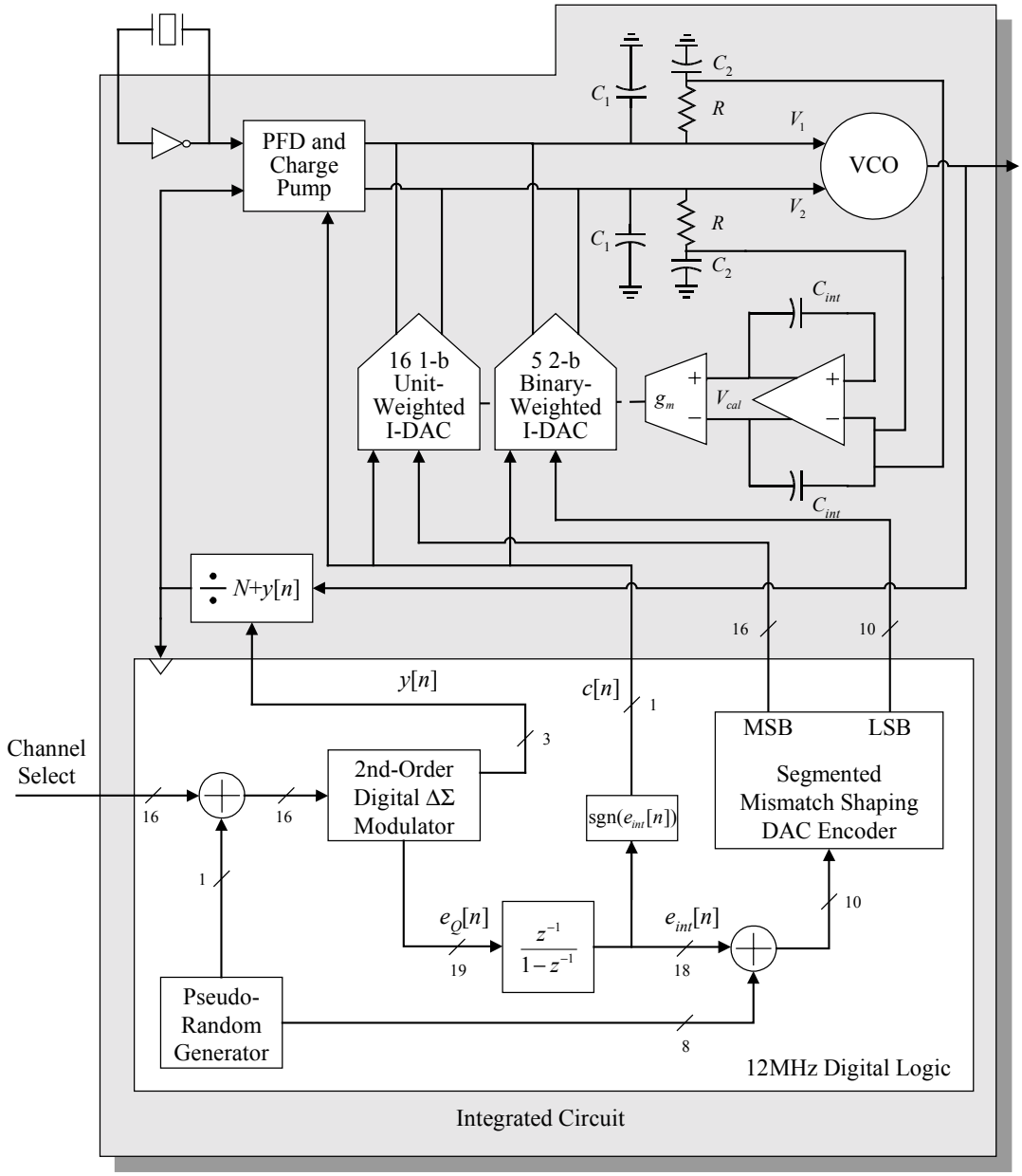


Figure 17: High-level functional diagram of the implemented PLL

A high-level block diagram of the implemented fractional-*N* PLL is shown in Figure 17. It differs from a typical phase noise canceling fractional-*N* PLL in that the charge pump, digital-to-analog converter (DAC), loop filter and VCO have been modified to implement the calibration technique. The additional circuitry required to

implement the calibration technique is an analog integrator and voltage-to-current converter connected between the modified loop filter and the DAC current bias. The details of the fractional-*N* PLL are presented throughout this paper; Section II presents the calibration technique. Section III discusses circuit issues involved in the implementation, and Section IV presents measured results from the prototype.

II. Calibrated Phase Noise Canceling Technique

A. The Problem with Phase-Noise Canceling PLLs

The core of a phase-noise canceling PLL is shown in Figure 18a [37, 38, 39]. It consists of a Phase/Frequency Detector (PFD), charge pump (CP), voltage-controlled oscillator (VCO), divider, DAC, and digital logic required to generate the divider input, $y[n]$, as well as the DAC input. The operation of a delta-sigma fractional-*N* PLL is discussed at some length in [40], but will be summarized in order to present the salient points necessary to understand the operation of the calibration technique. The divider output, $V_{div}(t)$, is a two level signal, where the n^{th} and $(n+1)^{th}$ rising edges are separated by $N + y[n]$ VCO cycles. The PFD compares the rising edges of $V_{div}(t)$ with the rising edges of a reference signal, $V_{ref}(t)$, and then generates control signals for the CP, resulting in a pulse of current, $i_{cp}(t)$, which deposits charge proportional to the time difference between $V_{div}(t)$ and $V_{ref}(t)$ onto the loop filter. This serves to either increase, or decrease the loop filter voltage, $V_{ctl}(t)$, and hence increase or decrease the frequency of the VCO. In this way, the PLL attempts to lock the phase of the divider output with the reference signal.

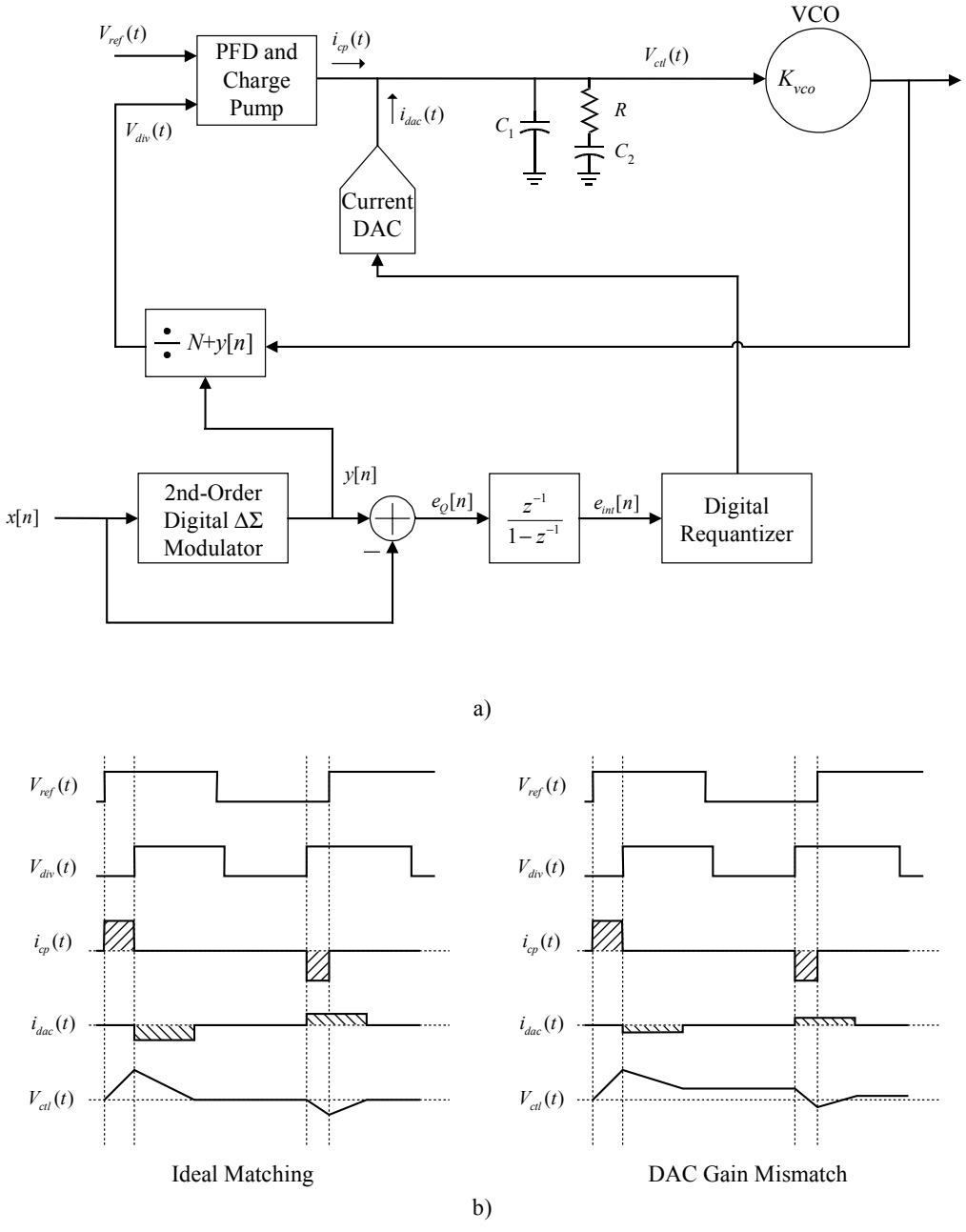


Figure 18: Phase Noise Canceling PLL; a) Block Diagram; b) Timing Diagram

If $y[n]$ is a constant, then the VCO frequency is $N + y[n]$ times the reference frequency. The VCO can be locked to a fractional multiple of the reference frequency by maintaining a fractional average value on $y[n]$. This is done by quantizing a frac-

tional number, $x[n]$ to an integer $y[n]$ with a delta-sigma modulator [41] such that the quantization noise, $e_Q[n]$ is high-pass spectrally shaped. Since it is only possible for the divider edge to occur after an integer multiple of the VCO period, instantaneously the divider output will never be phase-locked to the reference. At the output of the CP, this results in current pulses always adding or subtracting charge from the loop filter and, on average, the net charge added to the loop filter is zero. This CP charge deposited each reference period can be well modeled by the following expression [37]

$$Q_{cp}[n] = I_{CP}T_{VCO}\sum_{k=0}^{n-1} e_Q[k] = I_{CP}T_{VCO}e_{int}[n], \tag{127}$$

where T_{VCO} is the period of the VCO output under steady-state conditions, I_{CP} is the magnitude of the charge pump current, and $e_{int}[n]$ is the integrated quantization noise. Since the noise introduced by $e_{int}[n]$ is generated by the digital logic, the phase noise cancellation technique uses this information to subtract the error charge given by (127).

The DAC converts $e_{int}[n]$ into current pulses which have a charge nominally equal in magnitude and opposite in sign to the CP charge. Thus with ideal cancellation, the net voltage change on $V_{ctl}(t)$ over a period of the reference clock is zero, and is shown in Figure 18b. The DAC pulses can be mismatched from the CP pulses due to static current mismatch or pulse width mismatches [42]. This results in a residual charge error remaining on the loop filter, thereby limiting the achievable phase noise cancellation, also shown in Figure 18b.

The DAC circuitry is often simply a scaled copy of the CP circuitry in order to

maintain good matching between them. However the matching between DAC unit elements necessitates increased device sizes, and the speed of the CP circuitry necessitates reduced device lengths, which impose opposing constraints on the design of the DAC and CP circuitry. To date, intrinsic matching of CP and DAC circuitry has resulted in 16dB, 15dB and 29dB of phase noise cancellation for [37], [38], and [39] respectively.

B. Calibration for Phase-Noise Canceling PLLs

DAC gain mismatch results in a fraction of the original CP charge given by (127) being deposited into the loop filter each reference period. To a first order, after the CP and DAC pulses occur the loop filter voltage settles to a constant value related to this charge. The mismatch is estimated by multiplying this loop filter voltage with a binary *correlation signal*, $c[n]$, equal to $\mathrm{sgn}(e_{int}[n])$, each reference period. The average value of $c[n]$ is zero, and multiplying (127) by $c[n]$ results in a discrete-time signal which is always positive. Therefore if the DAC gain is greater or less than the CP gain, the correlated loop filter voltage will have a net positive or negative dc value respectively. This dc value is accumulated, and used to modify the DAC gain by adjusting the DAC bias current. The feedback of the calibration loop adjusts the DAC gain to minimize the dc component of the correlated loop filter voltage. An example of this is given in [36] where a source-follower isolates the loop filter from a sampling analog-to-digital converter (ADC). In this particular system, swapping the input sampling capacitor between the positive and negative inputs of the ADC performs the correlation operation. Two problems exist with this scheme. First, noise arising from the

multiplication of the correlation signal with the dc loop filter voltage, and quantization noise from the ADC must be filtered prior to adjusting the DAC bias current. This results in a long transient response of the calibration circuit, which settles in approximately 1 second [43]. Second, the buffer needs to provide isolation for the loop filter and thus requires a significant amount of power consumption.

To overcome these problems, a continuous-time calibration technique is utilized to reduce the noise from quantization and correlation of the dc loop filter voltage, and eliminate the sampling of the loop filter voltage. The method is shown conceptually in Figure 19a, from the DAC and CP to the VCO output. Two signal paths are necessary; one for PLL operation containing the required VCO input voltage to maintain the correct output frequency, and one for calibration loop operation, containing the correlated residual charge due to mismatch between the CP and DAC. The two signal paths are given by common-mode (CM) voltage, $\{V_p(t) + V_n(t)\} / 2$, and the differential-mode (DM) voltage, $V_{calp}(t) - V_{caln}(t)$.

The VCO in Figure 19a has two equal half-sized inputs, each of which is connected to a filter with identical component values. If both input terminals of the VCO were connected together, the VCO would behave identically to the VCO shown in Figure 18. To a first order, the output frequency is proportional to the sum of the two input voltages. Thus, to a first order, the VCO shown in Figure 19a is insensitive to $V_p(t) - V_n(t)$, and is only dependent on. The correlation signal, $c[n]$, is constant over the duration of a DAC and CP pulse and switches the DAC and CP currents, $i_{dac}(t)$ and $i_{cp}(t)$, between two equivalent loop filters, each of which is connected to an equally

sized VCO input. Since the VCO is only sensitive to the CM voltage, $\{V_p(t) + V_n(t)\}$ / 2, the switching due to $c[n]$ is transparent to the operation of the PLL, and to a first order results in the equivalent circuit shown in Figure 19b, where $V_{ctl}(t)$ is equal to $\{V_p(t) + V_n(t)\}$ / 2.

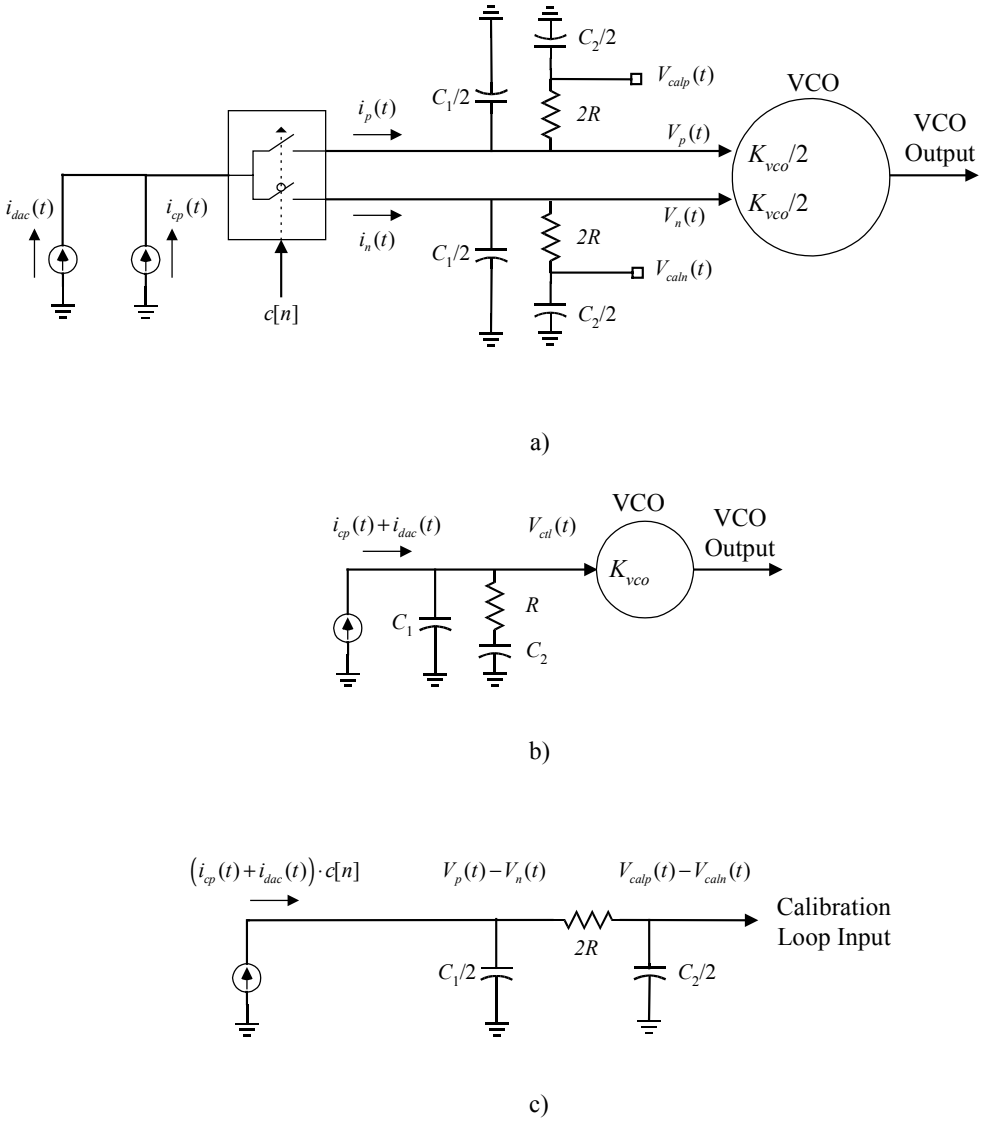


Figure 19: PLL Loop Modification for Calibration; a) Modified LF and VCO; b) Equivalent circuit for PLL; c) Equivalent single-ended half circuit for Calibration system

However since $c[n]$ is related to the CP and DAC charge, the switching of the CP and DAC current is equivalent in DM to multiplying $i_{dac}(t)$ and $i_{cp}(t)$ by $c[n]$, and results in a change in the DM voltage, $V_p(t) - V_n(t)$, when gain mismatch exists between the CP and DAC. In practice, $i_{dac}(t)$ and $i_{cp}(t)$ are large pulses of current occurring over a short duration, so $V_p(t)$ and $V_n(t)$ have large changes over the duration of the CP and DAC pulses. This causes a significant change at the input of the calibration loop during the DAC pulse, which results in a significant change in the DAC bias current during the duration of a DAC pulse. The voltages $V_{calp}(t)$ and $V_{caln}(t)$, which are filtered versions of $V_p(t)$ and $V_n(t)$ respectively are used in the calibration loop to reduce the variation in the DAC bias current for the duration of a DAC pulse. With matched loop filter components, $V_{calp}(t) - V_{caln}(t)$ is a filtered version of $V_p(t) - V_n(t)$, and therefore contains the correlated signal information necessary for calibration loop operation. The equivalent half-circuit for the calibration loop is shown in Figure 19c. Similar to PLL operation, the calibration loop is a differential circuit, and can be designed to have very low sensitivity to common-mode signals. In this manner, the common-mode voltage is used by the PLL, and the differential-mode voltage is used by the calibration loop.

Mismatches in the two paths will result in a CM to DM conversion in the calibration loop, and a DM to CM conversion in the PLL. The DM to CM conversion results in a scaled copy of $i_{dac}(t)$ and $i_{cp}(t)$ multiplied by $c[n]$ appearing at the CM input of the PLL. The dc present in this signal is compensated for by the PLL, and does not result in instability. The CM to DM conversion results in a scaled copy of $i_{dac}(t)$ and

$i_{cp}(t)$ appearing at the input to the calibration loop. Since this does not contain dc due to the steady-state operation of the PLL, the calibration loop settles to the correct value.

To illustrate the operation of the calibration technique, suppose that the PLL is in steady state, and the DAC gain is less than the CP gain. In this case, $V_p(t)$ would accumulate positive charge from $i_{cp}(t)$ and $i_{dac}(t)$, and $V_n(t)$ would accumulate negative charge from $i_{cp}(t)$ and $i_{dac}(t)$. Thus a mismatch would cause $V_p(t)$ to increase and $V_n(t)$ to decrease. Since the PLL is only sensitive to the common-mode voltage across the two loop filters, this has no effect on the PLL steady-state output frequency.

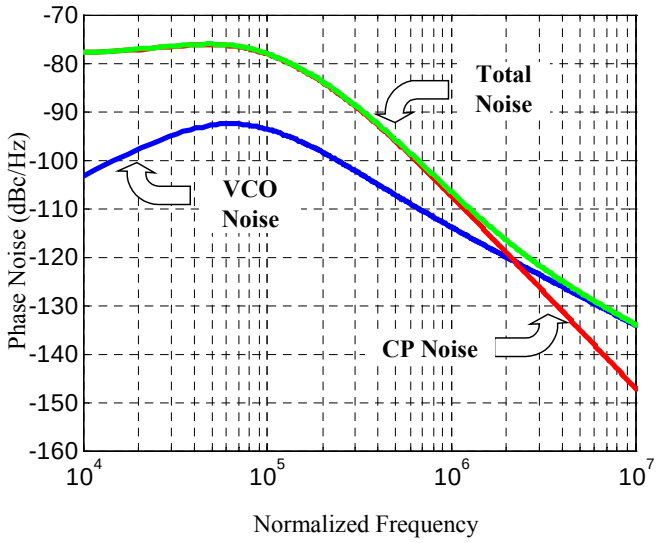
The DM voltage, $V_{calp}(t) - V_{caln}(t)$, is a filtered version of the DM loop filter voltage $V_p(t) - V_n(t)$, so from the preceding example $V_{calp}(t)$ will also increase and $V_{caln}(t)$ will also decrease. This DM voltage is then accumulated and used to adjust the DAC gain through the voltage-to-current converter such that the DM voltage, $V_{calp}(t) - V_{caln}(t)$, settles to zero. This also results in the DM voltage $V_p(t) - V_n(t)$ settling to zero.

III. Circuit Issues

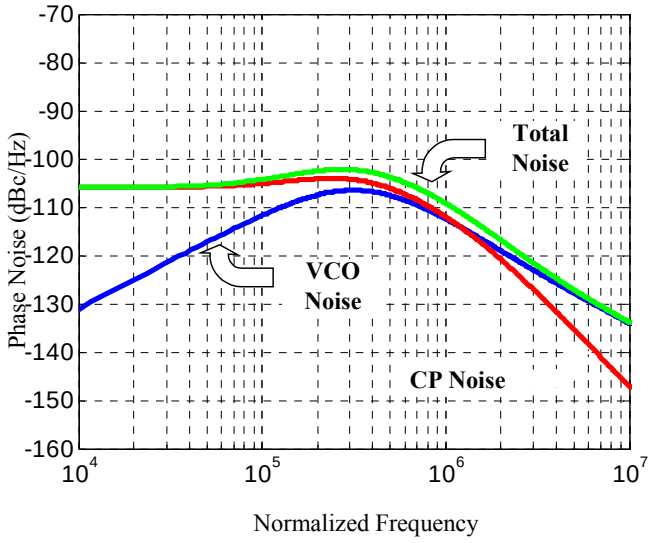
A. Overview

The circuit is implemented in the TSMC 0.18μm CMOS process, with single poly and six metal layers, Metal-insulator-metal capacitors and packaged in a 5mm 32 pin TQFN, with electro-static discharge (ESD) protection devices included on all pads. The circuits are all operated with a 1.8V supply, and the VCO, CP, PFD, DAC, digital

and loop filter are integrated on chip. Separate deep n-wells under the digital logic and critical analog circuitry and separate supply domains were used to help prevent interference from each circuit block.



a)



b)

Figure 20: Effect of PLL Bandwidth on component noise requirements; a) 100kHz bandwidth; b) 500kHz bandwidth

B. Power Consumption Issues

Widening the bandwidth of a PLL helps reduce in-band VCO phase noise and improve acquisition time, however, the attenuation of spot noise outside the PLL bandwidth is reduced. Consequently, to maintain a given level of phase noise performance outside the PLL bandwidth, the noise contributions of the reference, divider, PFD and CP circuits must be reduced. This effect is shown in Figure 20 for an out of band phase noise specification of –120dBc/Hz at 3MHz offset from the carrier. In order to meet this specification, the thermal noise requirements for the CP are significantly reduced from –77dBc/Hz to –103dBc/Hz (inband noise referred to the PLL output) when the PLL loop bandwidth is increased from 100kHz to 500kHz respectively. In this design, the CP had the largest power consumption due to the noise requirements.

In a delta-sigma fractional-*N* PLL, the transfer function of the CP noise to the output of the PLL is given by

$$H_{cp}(f) = \left(\frac{\pi N}{I_{CP}}\right) G(f) \tag{128}$$

where N is the divider value, and $G(f)$ is the closed-loop PLL transfer function from the divider input to the PLL output where, for frequencies within the PLL bandwidth, $|G(f)| \cong 1$ [44]. Since thermal noise in a MOSFET transistor is proportional to $\sqrt{I_{CP}}$, it can be seen from (128) the only mechanisms for decreasing the CP inband noise is to increase I_{CP} or decrease N. Decreasing N constrains the PLL design to having an

increased reference frequency for a fixed output frequency, which increases digital power consumption and reduces the choices for the reference frequency, while increasing I_{CP} results in increased power consumption in the CP. In the presented design, the choice was made to increase I_{CP} rather than increase the reference frequency.

C. Dynamic Bias Technique

The CP bias circuit is shown in Figure 21 where the transmission gates are CMOS transistors with dimensions of 10μm by 0.18μm. The enable clocks *en*, $\overline{en}$, and *en2* are generated such that the gate of each bias transistor is disconnected before removal of the current paths through each bias line. This is done in order to avoid disturbing the voltage on the gates of the bias transistors. To further reduce variation on the gate voltage of each bias, 24pF on-chip decoupling capacitors are used for each bias signal.

The CP bias circuitry only needs to be active during a CP pulse. Since the CP is on for a fraction of the reference period, the current through the bias circuitry is disabled in the manner described above whenever the CP is off. To ensure proper operation of the CP, the current is disabled such that *en* and *en2* are high for the duration of a CP pulse. The reduction in current dissipation is limited by the duty cycle of the enable signal. In the presented design, the optimum duration of *en* was found to be approximately 10ns, occurring 4.4ns before the divider edge. A similar technique is demonstrated in [45] for a PLL with 10kHz reference frequency and 500Hz bandwidth, however no circuit details are given on the implementation of the dynamic bias technique.

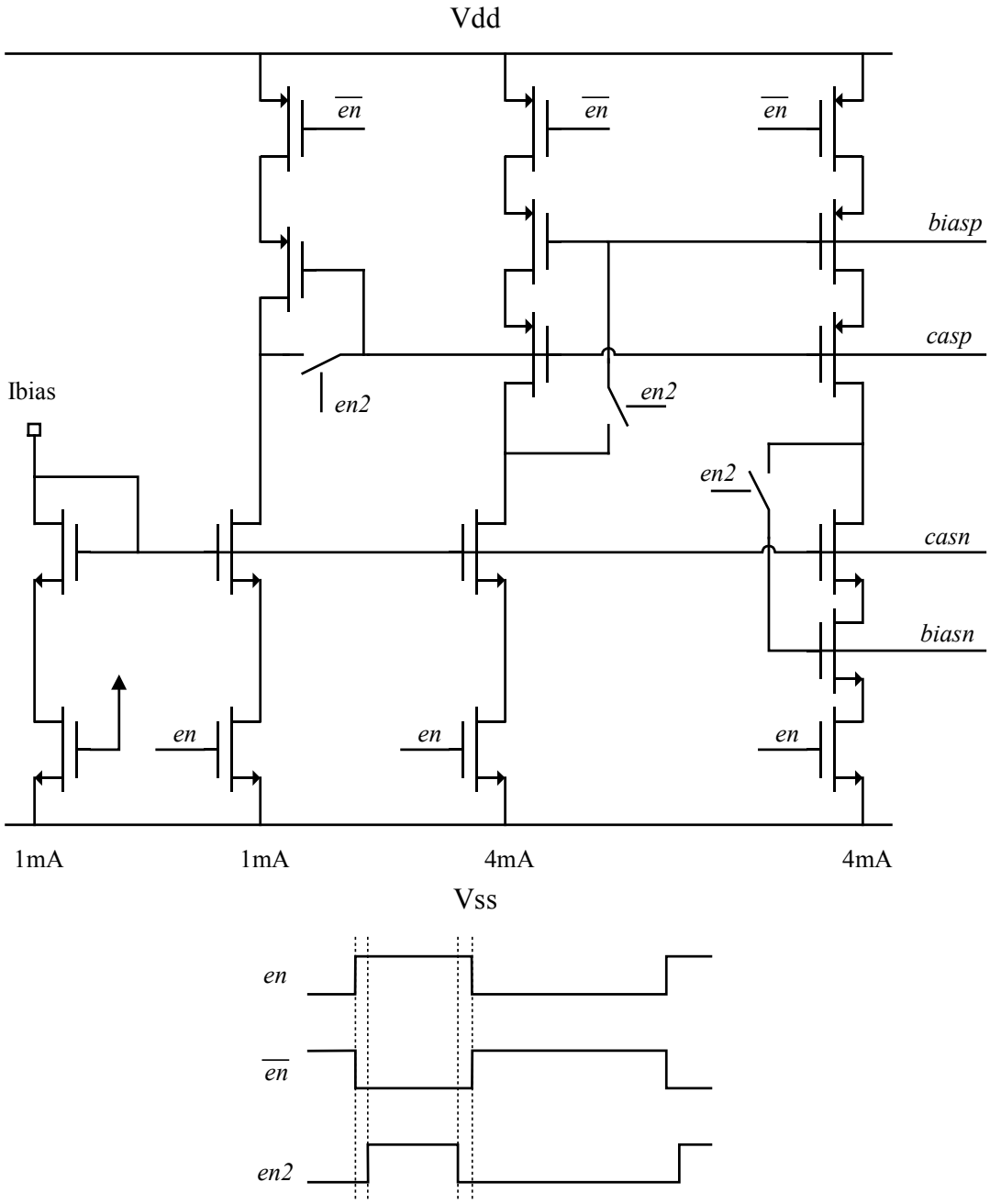


Figure 21: CP dynamic bias technique

D. Phase/Frequency Detector and CP

The PFD compares the rising edges of the divider and reference signals, and generates control pulses for the CP. To generate the proper polarity signals for the CP

and to provide the necessary drive, buffers are used between the PFD and CP. The PFD and buffers are shown in Figure 22, with the details of the PFD given in [37]. The up and down signals enable the CP positive and negative currents respectively. The up_{ped} and $down_{ped}$ signals are used to convert the mismatch between the positive and negative currents into a constant current offset each reference period which reduces non-linearity in the CP [37].

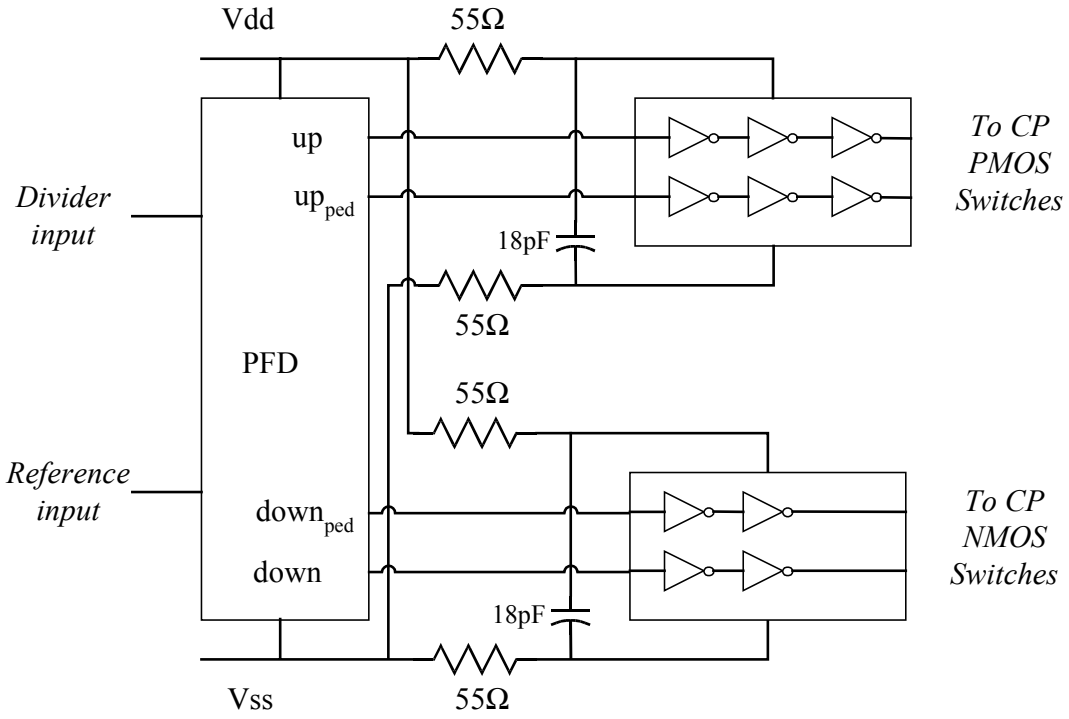


Figure 22: PFD and Buffer schematic

To reduce the supply coupling between up & down pulses, the buffer supplies are resistively drawn from PFD supply, with 18pF decoupling for each up and down buffer. The buffers draw a significant amount of current from the supply during the up and down transitions. The disturbance on the supply during transitions results in inter-

ference between the buffers. For example, if the up and up_{ped} signal transitions occurs first, the supply voltage is temporarily reduced, and the delay in the buffers for the down and $down_{ped}$ signal are increased. In this way, the difference between the rising edges of the up, up_{ped} and down, $down_{ped}$ pulses is subjected to a non-linearity when the two edges occur close to each other. This was found in simulation to provide sufficient isolation between the buffers.

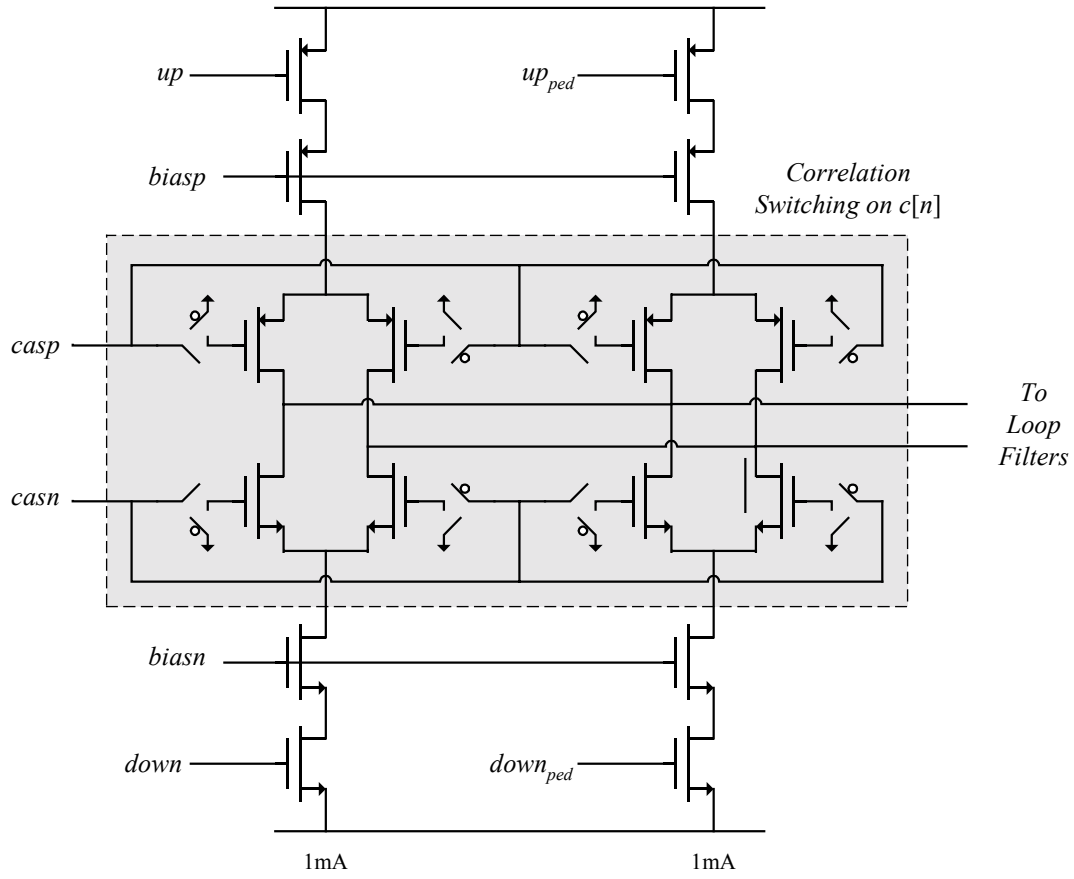


Figure 23: CP schematic

The CP schematic is shown in Figure 23. The correlation switching required for the calibration loop is implemented through the switching of the cascode devices

between each loop filter. The switching is synchronized to be 12 VCO periods before the divider edge in order to ensure that the CP current has the maximum time to deposit charge into the loop filters.

E. VCO and Divider

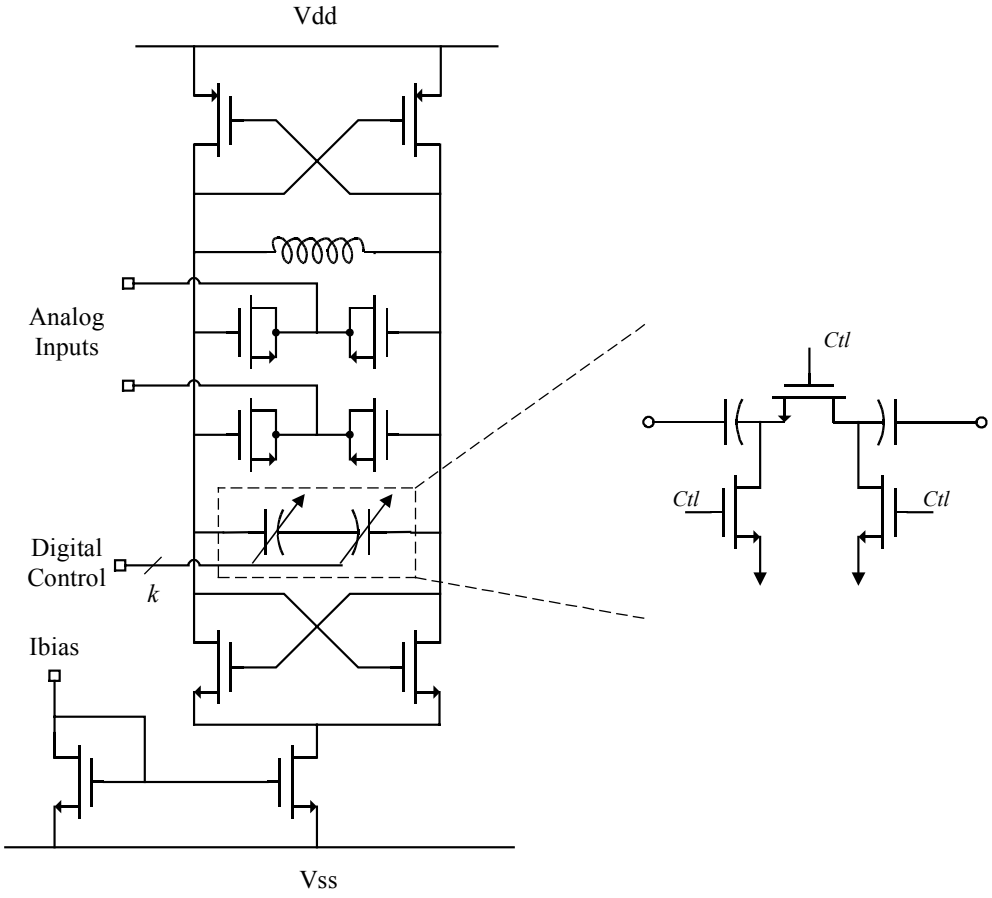


Figure 24: VCO schematic

The VCO is a negative-g_m CMOS LC oscillator, as shown in Figure 24. The differential inductor is a stacked M5 & M6 spiral, with a Q of approximately 8 at 2GHz. Two equal MOS varactors provide tuning over a 0.6V-1.2V range, with a nominal tuning gain of 60MHz/V at each input. Coarse digital tuning is performed by

switching MIM capacitors of 20fF & 80fF sizes into the tank circuit [46]. This is sufficient for the VCO to cover a range from 2.35GHz to 2.65GHz, which encompasses the entire 2.4 GHZ ISM band.

The divider is a 7-stage pulse-swallowing divider similar to that used in [37] and [47]. CML logic is used in the first two stages, and CMOS logic is used for the remaining stages. The divider output is resynchronized to the output of the first CML stage in order to reduce divider jitter noise and modulus dependent delays.

F. Digital

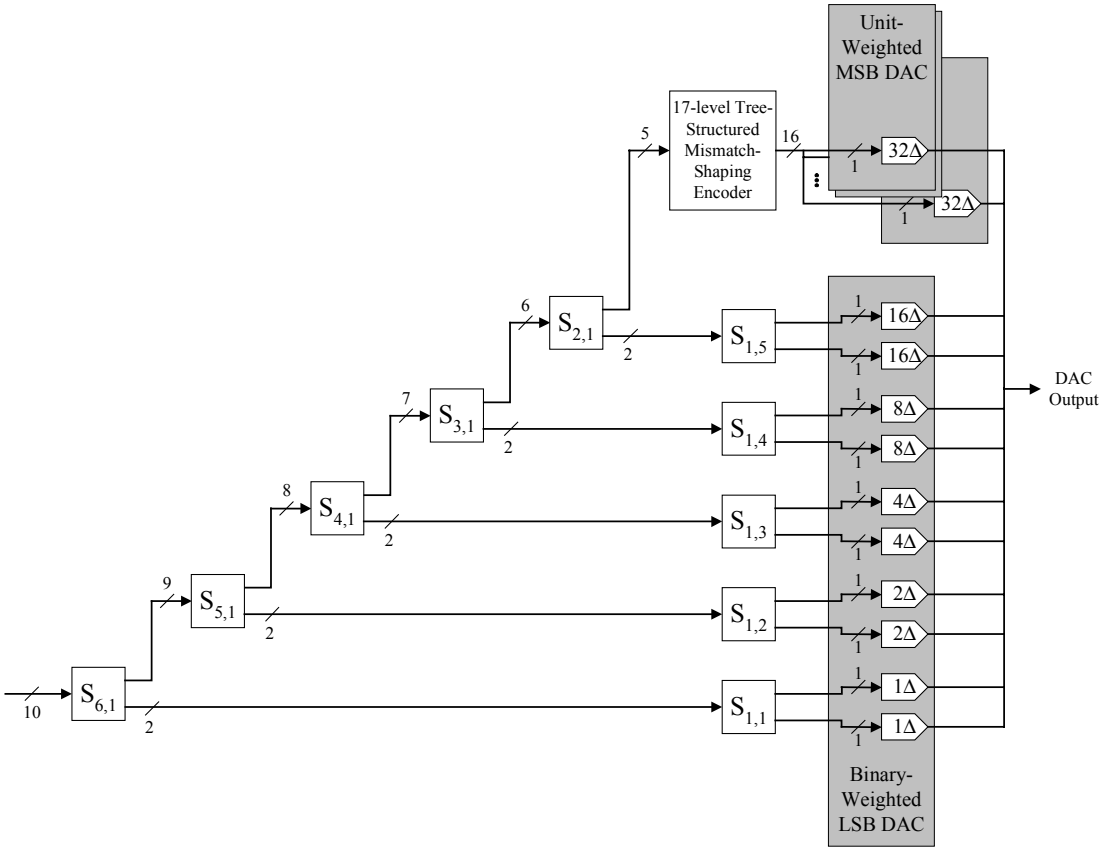


Figure 25: Details of the mismatch-shaping digital encoder

The digital logic was implemented using a standard cell library with transistor gate lengths of 0.18μm. The requantizer adds an 8 lsb-bit pseudo-random number to the input then truncates the result to 10 bits to ensure that the requantization noise is uncorrelated from the delta-sigma quantization noise [48]. The mismatch scrambling encoder was implemented as a partially segmented tree-structured encoder, and is shown in Figure 25. Each switching block, shown as $S_{k,r}$, uses a random sequence to ensure that the digital input exercises all DAC elements in a random fashion to scramble DAC element mismatches. More details on the switching blocks are given in [49].

G. Loop Filter and DAC

The loop filter is fully integrated, with values for R, C_1, and C_2 in Figure 17 of 5kΩ (polysilicon resistor), 18pF (MIM capacitor), and 282pF (PMOS capacitor) respectively. Coarse tuning is provided to account for process variations. Each DAC element is a resistively degenerated charge pump cell and shown in Figure 26, with a DAC lsb current of 1μA. The transistor sizes are large to reduce the mismatch of the DAC, which in turn results in channel charge in the gates of the transistors to be of the order of the charge delivered by the DAC unit elements. Since this can lead to a significant DAC gain error, a fast turn off scheme is used with a reset switch is connected between bias transistor source and gate. When the DAC is enabled, the reset switch is off, and either M1 or M2 supplies current into the loop filter. When the DAC is disabled, the gate & source of M1 and M2 are shorted together and channel charge from the bias and switch transistors are shunted to the DAC bias signal. This results in a significant disturbance on the DAC bias, however this occurs after the DAC pulse

event and the reference period is sufficient for settling of the DAC bias to the proper voltage before the next DAC pulse. Previously published reset schemes involve shorting the source of the bias transistor to the supplies [50], however this was not done in order to minimize charge injection through the shorting switch into the loop filter. The correlation switching for the DAC is implemented by using two identical DACs, enabled by $c[n]$, and connected between the DAC encoder and both loop filters. The gain mismatch between each DAC was found to be negligible and did not affect the calibration loop operation.

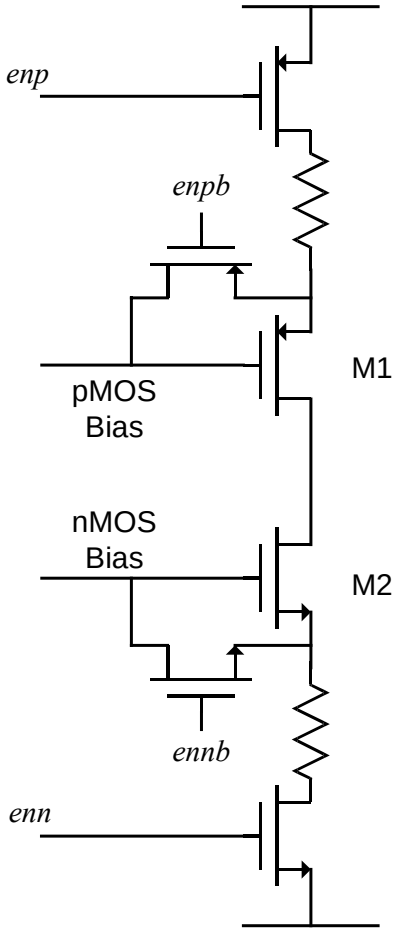


Figure 26: DAC schematic

Comparing Figure 23 and Figure 26, it can be seen that the DAC and CP circuits have different architectures since the DAC was designed in order to improve matching between elements, and the CP was designed in order to ensure fast turn-on. This results in poor DAC gain matching, which the calibration loop corrects for.

H. Calibration Circuitry

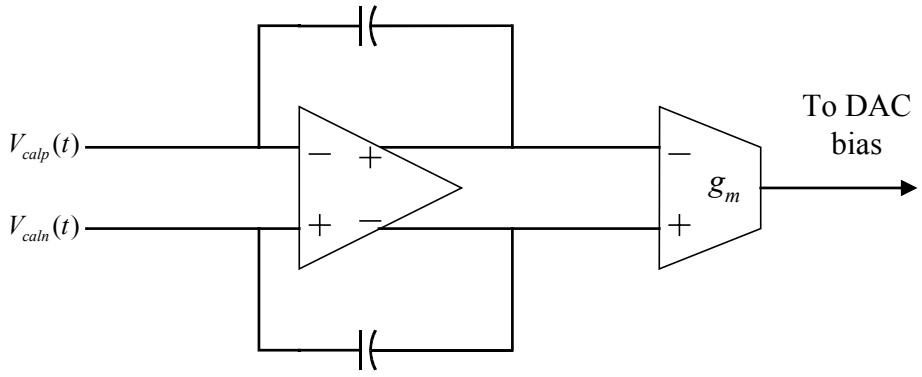


Figure 27: Calibration circuit

The calibration system is shown in Figure 27, with $V_{calp}(t)$ and $V_{caln}(t)$ defined in Figure 19. The OTA integrator accumulates the correlated signal information containing the DAC mismatch signal. The DAC gain is adjusted by applying the output of the voltage-to-current converter into the DAC bias current. The OTA is a folded-cascode, single stage amplifier with a wide input CM range to account for the variation of the loop filter voltage over the PLL frequency range. The OTA is designed with sufficiently low offset voltage that the settled voltages on $V_p(t)$ and $V_n(t)$ do not result in current mismatch in the CP and DAC when switched between the two calibration path. In normal operation, the simulated current consumption of the calibration circuit is 1.3mA.

IV. Measurement Results

The performance of the IC was tested over all 79 Bluetooth channels. The results, presented in Table 2, are compared between the calibration technique and DAC enabled and disabled. With the DAC and calibration technique enabled, the phase noise performance at a 3MHz offset was found to improve by 27dB to 33dB. The worst-case phase noise with the techniques enabled was –101dBc/Hz and –124dBc/Hz at a 100kHz and 3MHz offset respectively. A representative plot of the phase noise with the DAC disabled and enabled, and with the calibration technique enabled is shown in Figure 28. Similar results are seen on all tested Bluetooth channels. For each channel, the settling time of the calibration loop was found to be approximately 35μs, which makes this calibration technique suitable for the numerous wireless applications where the PLL is powered down when not in use. The settling performance is shown in Figure 29.

The worst-case spurious tones are also given in Table 2. With the calibration technique enabled, the fractional spurs were found to be within the required Bluetooth specifications. The fractional spurs can be seen to be significantly higher when the DAC is disabled. Simulations indicate that this is due to K_{vco} non-linearity in the MOS varactors used in the VCO. K_{vco} can vary by up to 30% over the output voltage range of the CP, so when the DAC and calibration technique are enabled, the net voltage change on the loop filter each reference period is greatly reduced, resulting in improved K_{vco} linearity. The calibration technique was found to have an insignificant impact on the fractional spur performance of the PLL versus manually calibrating the

DAC gain and disabling the calibration technique. The fractional and reference spur performance at a center frequency of 2.403 GHz is seen in Figure 30.

Table 2: Performance Parameters

Design Details		
Technology	TSMC 0.18 μm 1P6M CMOS	
Package and Die Area	32 pin TQFN, 2.2×2.2 mm^2	
Reference Frequency	12 MHz	
Output Frequency	2.4 – 2.5 GHz	
Loop Bandwidth	> 730kHz	
Measured Current Consumption (at 1.8V)		
VCO and Divider Buffer	6.9 mA	20.9 mA
Divider	5.8 mA	
CP (with dynamic biasing)	2.7 mA	
Digital	0.5 mA	
DAC	3.6 mA	
Calibration	1.4 mA	
Xtal Buffer	4.1 mA	9.4 mA
External Buffer	5.3 mA	
Measured Worst Case Integer-*N* Performance		
Phase Noise @ 100 kHz	-104 dBc/Hz	
Phase Noise @ 3 MHz	-126 dBc/Hz	
Measured Worst Case Performance, DAC and Calibration Technique Disabled		
Phase Noise @ 3 MHz	-91 dBc/Hz	
Fractional Spur @ 1 MHz	-40 dBc	
Fractional Spur @ 2 MHz	-42 dBc	
Fractional Spur @ ≥3 MHz	-45 dBc	
Measured Worst Case Performance, DAC and Calibration Technique Enabled		
Phase Noise @ 100 kHz	-101 dBc/Hz	
Phase Noise @ 3 MHz	-124 dBc/Hz	
Fractional Spur @ 1 MHz	-47 dBc	
Fractional Spur @ 2 MHz	-57 dBc	
Fractional Spur @ ≥3 MHz	-62 dBc	
Reference Spur	-53 dBc	

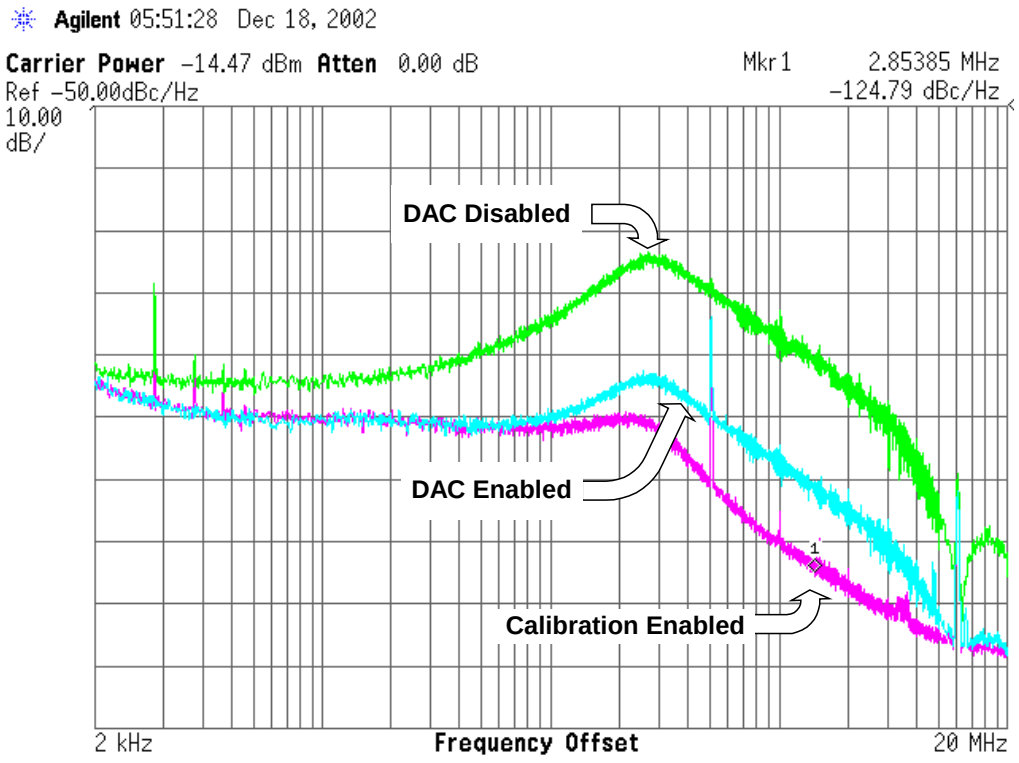


Figure 28: Phase Noise Performance

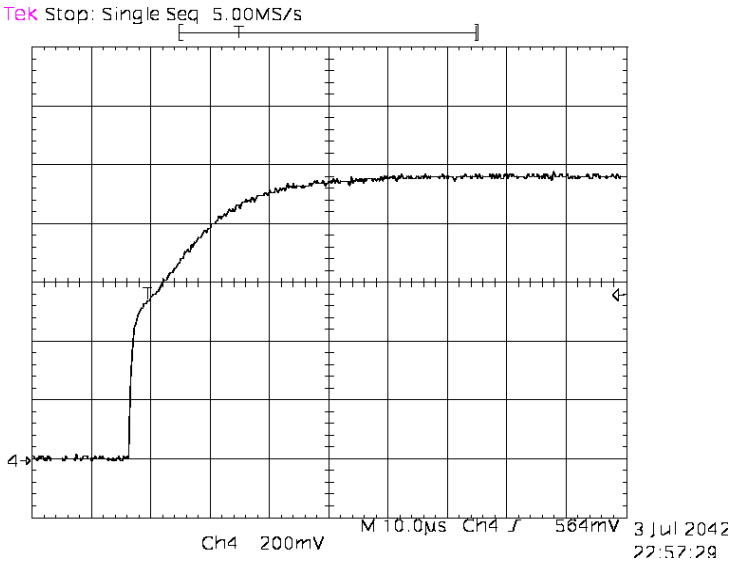


Figure 29: Calibration Loop Settling Performance

The worst-case reference spur was found to be –53dBc. Measurements of the

IC indicated that the P/N mismatch in the CP was 2%. While the CP linearization technique from [37] improves the linearity due to P/N mismatch, it does so at the expense of transforming the non-linearity into a constant charge offset each reference period, which results in the increased spur. To improve the matching even further, replica biasing techniques could have been used [38, 51]. The chip photograph is shown in Figure 31.

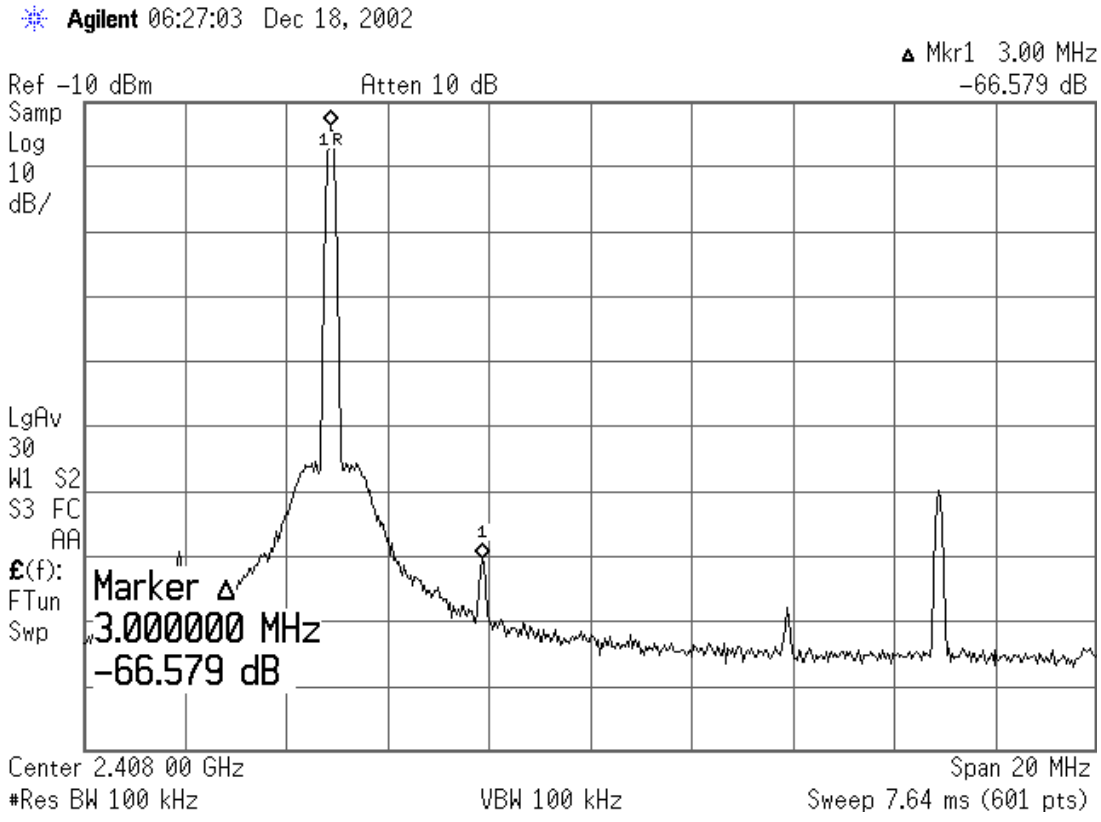


Figure 30: PLL Output Spectrum

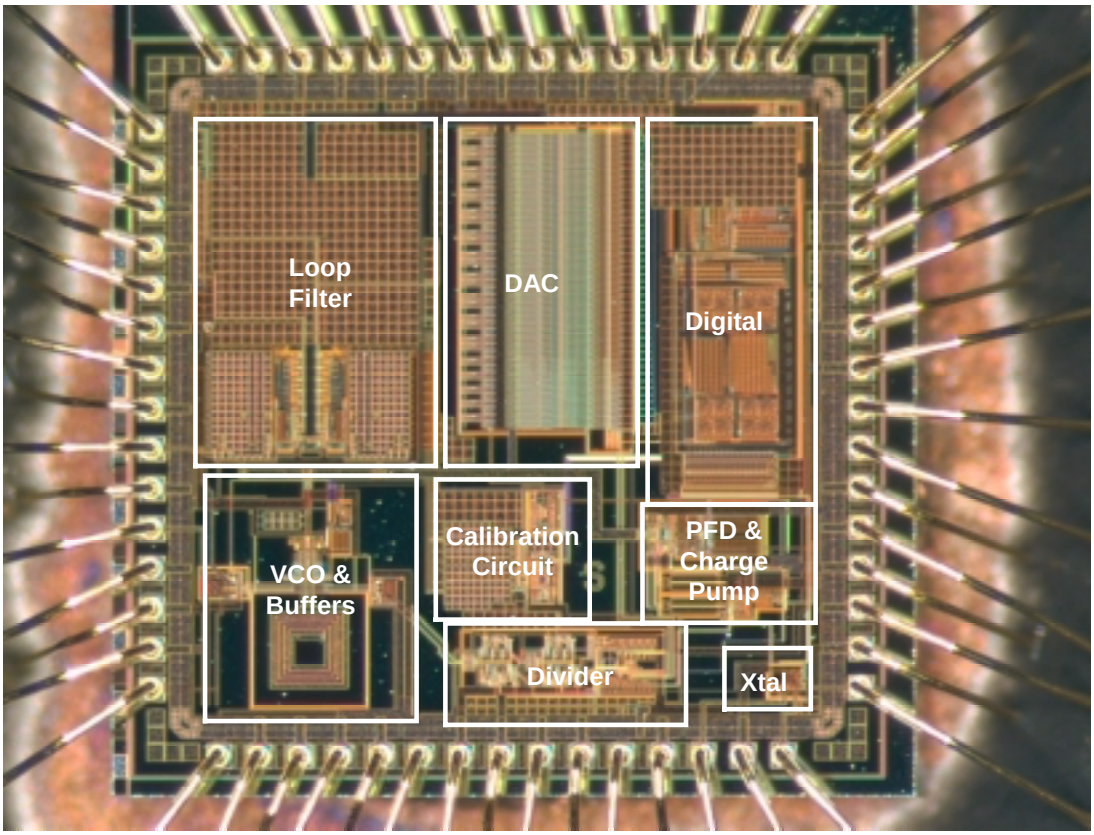


Figure 31: Die Photograph

V. Conclusions

A calibration technique suitable for phase-noise canceling fractional-*N* PLL and a dynamic biasing technique have been presented and demonstrating as enabling components in a low power, fully integrated delta-sigma fractional-*N* PLL. The calibration technique enables a wide loop filter bandwidth, which allows for a fully integrated passive loop filter, and flexibility in the system choices such as reducing the reference frequency, which increases the phase noise. The calibration technique demonstrates fast settling time, enabling its use as a background technique in most wireless transceivers. The dynamic biasing technique is not restricted to being used in this

class of PLL, and can be added on as a simple enhancement to reduce the power consumption of any PLL.

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