The Effects of Inter-Symbol Interference in Dynamic Element Matching DACs

Jason Remple and Ian Galton, *Fellow, IEEE*

***Abstract*—Dynamic element matching (DEM) is often applied to multi-bit DACs to avoid nonlinear distortion that would otherwise result from inevitable mismatches among nominally identical circuit elements. Unfortunately, for such a DEM DAC to fully achieve this objective its constituent 1-bit DACs must be free of inter-symbol interference (ISI), i.e., the error from each 1-bit DAC must not depend on prior samples of the DAC's input sequence. This paper provides the first quantitative general analysis of the effects of ISI on the continuous-time outputs of DEM DACs. The analysis provides some surprising insights such as the conclusion that for certain types of DEM the only nonlinear distortion caused by ISI is second-order distortion. The paper also presents a digital pre-distortion technique that cancels the second-order distortion in the DEM DAC's first Nyquist band if information about the 1-bit DAC mismatches is available.**

***Index Terms*—DAC, DEM, ISI.**

I. Introduction

A MULTI-BIT digital-to-analog converter (DAC) converts a digital input sequence, $x[n]$, to a continuous-time analog output waveform, $y(t)$. In most multi-bit DACs the digital input sequence is mapped to multiple 1-bit digital sequences that each drive a 1-bit DAC, and the outputs of the 1-bit DACs are summed to form $y(t)$. Ideally, each 1-bit DAC generates a two-level analog output waveform that instantaneously switches between its two levels when its input bit value changes from 0 to 1 or 1 to 0. The mapping of $x[n]$ to the 1-bit DAC input sequences and the nominal output levels of the various 1-bit DACs are designed such that in the absence of non-ideal circuit behavior $y(t) = x[n]$ for all t within the nth clock period and each $n = 0, 1, 2, \ldots$.

In practice, non-ideal circuit behavior causes multi-bit DACs to deviate from this ideal behavior. Particularly significant types of non-ideal circuit behavior are component mismatches and nonlinear inter-symbol interference (ISI). Mismatches among nominally identical components that make up the 1-bit DACs inevitably occur during fabrication and cause signal-dependent error in the multi-bit DAC output. Additionally, practical 1-bit DACs do not transition instantaneously between their two levels, so they introduce transient errors. In many cases, a 1-bit DAC's transient error depends on one or more of its prior input bit values as well as its current input bit value. Such transient errors are said to contain ISI. Asymmetry between the rising and falling transient errors of the 1-bit DACs, which typically results from component mismatches, causes the ISI to contain nonlinear distortion [1]–[14].

Depending on the relative scaling of the 1-bit DACs in a multi-bit DAC, and depending on the value of $x[n]$, there can be multiple sets of 1-bit DAC input bit values that would yield the same value of $y(t)$ during the nth clock period in the absence of non-ideal circuit behavior. Dynamic element matching (DEM) is a digital technique that exploits such *redundancy* to manage the error caused by component mismatches [15]–[34]. In the absence of ISI, the only significant error caused by component mismatches in such a DEM DAC is noise-like and uncorrelated with $x[n]$, whereas in a multi-bit DAC without DEM it would be nonlinear distortion. DEM can be implemented such that the noise-like error is spectrally shaped for use in oversampling DEM DACs or scrambled for use in Nyquist-rate DEM DACs.

Unfortunately, DEM does not completely eliminate nonlinear distortion from ISI [35]. Nevertheless, contrary to conventional wisdom, this paper shows that DEM does have a significant effect on the ISI error, and if the DEM satisfies certain properties the effect is beneficial.

The paper analyses the effects of ISI on the continuous-time outputs of DEM DACs. In contrast, previously published work analyzes the effects of ISI on DEM DACs by modelling the ISI as a discrete-time, input-referred error sequence [35]–[37]. Such discrete-time models are useful for oversampling applications in which the DEM DAC output is integrated and sampled, e.g., as in continuous-time $\Delta\Sigma$ ADCs. The sampling operation aliases the ISI into a single Nyquist band, which makes it possible to accurately model the ISI as a discrete-time, input-referred sequence. However, in applications where the DAC output is not sampled such aliasing does not occur, so it is not possible to model the ISI accurately as a discrete-time sequence. Moreover, in most such applications only a single Nyquist band is of interest, and it is impossible to accurately analyze the effects of ISI on a single Nyquist band with a discrete-time, input-referred ISI model. In Nyquist-rate DEM DAC applications, such insight is particularly critical.

The results presented in this paper address this problem. The analysis is general in that it applies to all types of DEM, and it is backward compatible in the sense that the results reduce to prior continuous-time DEM DAC results in the absence of ISI.

Manuscript received April 14, 2016; revised July 9, 2016 and August 12, 2016; accepted August 13, 2016. Date of publication October 6, 2016; date of current version January 6, 2017. This work was supported by the National Science Foundation under Award 1343389, by Analog Devices Inc., and by the corporate members of the UCSD Center for Wireless Communications. This paper was recommended by Associate Editor P. Rombouts.

J. Remple is with Microchip Technology Inc., San Diego, CA 92121 USA, and also with the University of California, San Diego, La Jolla, CA 92092-0407 USA (e-mail: jason.remple@microchip.com).

I. Galton is with the Electrical and Computer Engineering Department, University of California, San Diego, La Jolla, CA 92092-0407 USA (e-mail: galton@ucsd.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2016.2601026

1549-8328 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

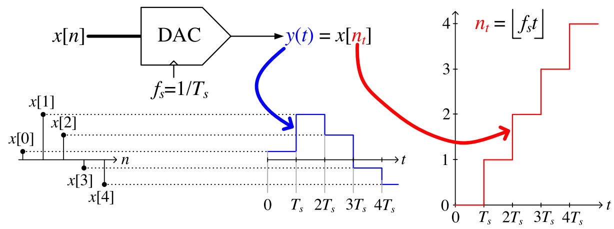

Fig. 1. Ideal NRZ DAC behavior.

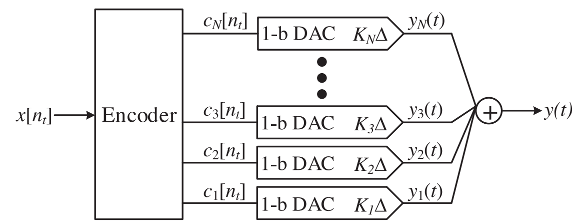

Fig. 2. General form of a multi-bit DAC.

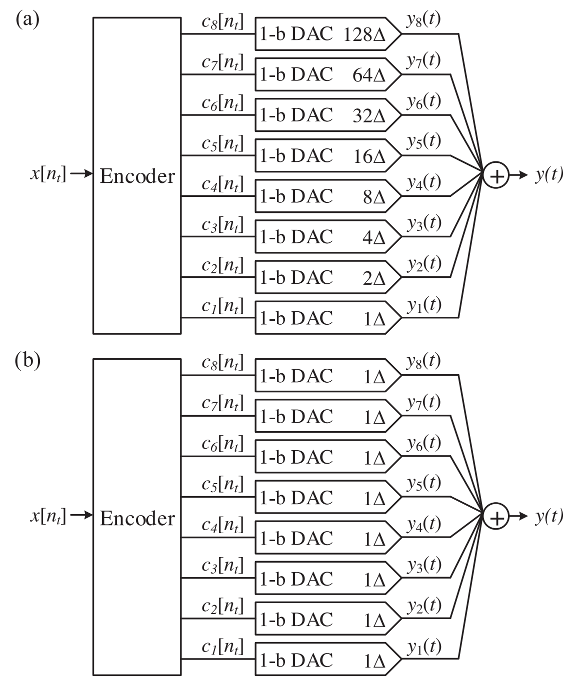

Fig. 3. Example DACs: (a) with power-of-two weighted 1-bit DACs, and (b) unity weighted 1-bit DACs.

It shows that the DEM DAC error resulting from ISI always consists of a linear term, a second-order distortion term, and a term that is noise-like and may or may not also contain nonlinear distortion depending on the type of DEM used. As the results are based on a continuous-time analysis they quantify the effects of ISI on all Nyquist bands of the DEM DAC and they are not subject to the aliasing problem described above that is inherent to prior discrete-time analyses.[1] Additionally, the continuous-time analysis enables some new observations about previously proposed techniques to mitigate ISI, and enables a new method of digitally cancelling nonlinear distortion from ISI in a mismatch-scrambling DEM DAC's first Nyquist band if information about the 1-bit DAC mismatches is known.

The remainder of the paper consists of five main sections. Section II briefly reviews the general form of a continuous-time multi-bit DAC, and the remaining sections present the new results of the paper. Section III defines the general form of the continuous-time error introduced by each of the 1-bit DACs. Section IV presents the ISI analysis with support from two appendices, and Section V applies the results to make observations about previously published ISI reduction techniques in DEM DACs. Section VI presents the new nonlinearity distortion cancellation technique using the results from Section V.

II. Nyquist-Rate DAC Overview

The DAC input, $x[n]$, is an f_s-rate sequence of digital codewords, each of which is interpreted by design convention to have a numerical value in the range

$$\left\{-\frac{M\Delta}{2},\ \Delta-\frac{M\Delta}{2},\ 2\Delta-\frac{M\Delta}{2},\ldots,M\Delta-\frac{M\Delta}{2}\right\} \tag{1}$$

where M is the number of DAC input levels minus one (so M is a positive integer), Δ is the DAC's minimum step-size, and f_s is the clock rate of the DAC. The continuous-time analog output of an ideal non-return-to-zero (NRZ) DAC is given by

$$y(t)=x[n_t] \tag{2}$$

where n_t is a continuous-time function of t given by

$$n_t=\lfloor f_s t\rfloor \tag{3}$$

and $\lfloor f_s t\rfloor$ denotes the largest integer less than or equal to $f_s t$. Examples of the n_t and output waveforms from such a DAC are shown in Fig. 1.

[1]The kth Nyquist band for $k=1,2,\ldots$, is defined as the set of frequencies that satisfy $(\pi(k-1))f_s<|\omega|<(\pi(k-1)+\pi)f_s$.

The general form of a DAC that implements this behavior aside from error caused by non-ideal circuit behavior is shown in Fig. 2. It consists of an all-digital block called an encoder and N 1-bit DACs. The 1-bit DAC outputs, $y_i(t)$, are summed to form the overall DAC output, $y(t)$, i.e.,

$$y(t)=\sum_{i=1}^{N}y_i(t). \tag{4}$$

In general, the output of the ith 1-bit DAC has the form

$$y_i(t)=x_i[n_t]K_i\Delta+e_i(t) \tag{5}$$

where

$$x_i[n_t]=\underbrace{c_i[n_t]-\frac{1}{2}}_{=\pm\frac{1}{2}} \tag{6}$$

$c_i[n]$ is the 1-bit DAC input sequence (which is either 0 or 1 for each n), K_i is a constant called the 1-bit DAC's weight, and $e_i(t)$ represents any deviation from ideal NRZ 1-bit DAC operation, such as noise and distortion from non-ideal analog circuit behavior. By design, each K_i is an integer, $K_1=1$, and $K_i\geq K_{i-1}$ for $i=2,3,\ldots,N$. Examples of DACs with different choices of 1-bit DAC weights are shown in Fig. 3.

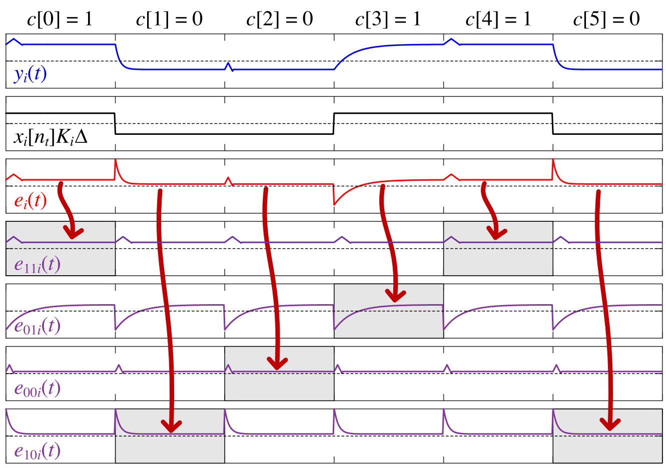

Fig. 4. Example NRZ 1-bit DAC waveforms.

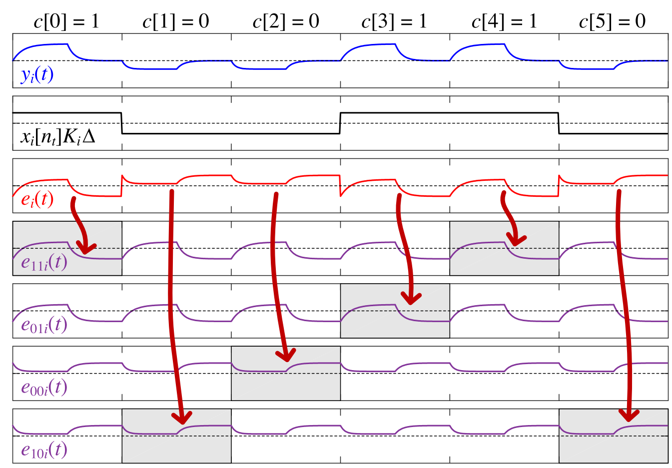

Fig. 5. Example RZ 1-bit DAC waveforms.

For each such DAC, the encoder sets its output bits, $c_i[n_t]$, such that

$$\sum_{i=1}^{N} x_i[n]K_i\Delta = x[n]. \tag{7}$$

Substituting (5) into (4) and (7) with (3) into the result shows that in the absence of deviations from ideal NRZ behavior (i.e., if the $e_i(t)$ terms in (5) were absent) the DAC would have the ideal behavior given by (2).

III. Mismatch, Transient Error, and ISI Model

Particularly significant types of non-ideal 1-bit DAC behaviors are mismatches from fabrication errors among nominally identical components that make up the 1-bit DACs, non-instantaneous rise and fall transitions, and inter-symbol interference (ISI).[2] In current-steering 1-bit DACs, these non-idealities can be realistically modelled as

$$e_i(t) = \begin{cases} e_{11i}(t), & \text{if } c_i\left[n_t-1\right]=1,\, c_i\left[n_t\right]=1 \\ e_{01i}(t), & \text{if } c_i\left[n_t-1\right]=0,\, c_i\left[n_t\right]=1 \\ e_{00i}(t), & \text{if } c_i\left[n_t-1\right]=0,\, c_i\left[n_t\right]=0 \\ e_{10i}(t), & \text{if } c_i\left[n_t-1\right]=1,\, c_i\left[n_t\right]=0 \end{cases} \tag{8}$$

where $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$, are periodic waveforms with period $T_s = 1/f_s$ that represent the error over each clock period corresponding to the four different possibilities of the current and previous 1-bit DAC input bit values. During any given T_s clock period, the 1-bit DAC error, $e_i(t)$, is equal to exactly one of the $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ waveforms.

Example 1-bit DAC waveforms are shown in Fig. 4. The arrows show which of the $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ periods are active, i.e., equal to $e_i(t)$. Each active period of the $e_{10i}(t)$ or $e_{01i}(t)$ waveform represents the transient error associated with an input bit transition from 1 to 0 or 0 to 1, respectively. Each active period of the $e_{00i}(t)$ and $e_{11i}(t)$ waveforms represents errors such as clock feedthrough that occur when the 1-bit DAC's current input bit is unchanged from the previous T_s clock period. The values of $e_{00i}(t)$ and $e_{10i}(t)$ at the end of each T_s clock period represent the final settling error of the 1-bit DAC when its input bit is 0, and those of $e_{11i}(t)$ and $e_{01i}(t)$ represent the final settling error of the 1-bit DAC when its input bit is 1.

Equation (8) models ISI because $e_i(t)$ depends on the 1-bit DAC's current and previous input bit values. In the special case where

$$e_{00i}(t) = e_{10i}(t) \quad \text{and} \quad e_{11i}(t) = e_{01i}(t) \tag{9}$$

it follows from (8) that $e_i(t)$ depends only on the 1-bit DAC's current input bit value, in which case ISI is avoided. This condition can be implemented in practice by resetting the state of each 1-bit DAC at the end of every T_s clock period. For example, in a so-called *return-to-zero* (RZ) 1-bit DAC, the 1-bit DAC output is set to zero (or some other signal-independent level) for a portion of each T_s clock period. Example RZ 1-bit DAC waveforms are shown in Fig. 5. It can be verified visually from Fig. 5 that (9) holds in this case.

The model described above, and hence the results derived in the remainder of the paper, assume that each 1-bit DAC output only depends on the 1-bit DAC's input bit values during the current and immediately prior clock period. In all applications known to the authors, this is an accurate assumption. However, if necessary the model can easily be extended. For example, if the 1-bit DAC output were to depend on the input bit values during the current and prior two clock periods, then $e_i(t)$ could be decomposed into $2^3 = 8$ periodic waveforms, each with period T_s. The results presented in the remainder of the paper could be extended to such a model if necessary. Although this would complicate the equations, it would not require any new ideas or techniques.

IV. Effects on DEM DACs

Depending on the choice of 1-bit DAC weights, there can be multiple sets of encoder output bit values that satisfy (7)

[2]In this context, ISI occurs if $e_i(t)$ depends on not only the current value of $c_i[n]$ but also one or more past values of $c_i[n]$.

for a given DAC input value. Such DACs are said to have *redundancy*. For example, in the unity-weighted 9-level DAC shown in Fig. 3(b), $K_i = 1$ for $i = 1, 2, \ldots, 8$, so (7) is satisfied when $x[n] = -3\Delta$ provided exactly one of the encoder outputs is one and the rest are zero. Hence, in this case there are 8 different (redundant) sets of encoder output values that would yield the same DAC output in the absence of non-ideal circuit behavior. However, given that the 1-bit DAC errors, $e_i(t)$, vary from one 1-bit DAC to another, each of these 8 choices has a different effect on the overall DAC error in general.

DEM DACs take advantage of redundancy to manipulate the usage pattern of the 1-bit DACs to impart desirable properties to the overall DAC error arising from the 1-bit DAC errors. A DEM DAC has the general form shown in Fig. 2 except the encoder is a *DEM encoder*. The DEM encoder selects its output bits according to a deterministic or pseudo-random algorithm that exploits the above-mentioned redundancy while still satisfying (7).

As explained in [22] the output bit sequences of a DEM encoder can be written as

$$c_i[n] = \frac{1}{\Delta}\left(m_i x[n] + \lambda_i[n]\right) + \frac{1}{2} \tag{10}$$

for $i = 1, 2, \ldots, N$, where each m_i is a constant, each $\lambda_i[n]$ is a sequence, and

$$\sum_{i=1}^{N} K_i m_i = 1 \quad \text{and} \quad \sum_{i=1}^{N} K_i \lambda_i[n] = 0. \tag{11}$$

In Nyquist-rate DACs the DEM encoder usually is designed to ensure that the $\lambda_i[n]$ sequences well approximate zero-mean random sequences that are uncorrelated with $x[n]$ and each other and are white, i.e.,

$$\left.\begin{array}{l} E\left\{\lambda_i[n]\right\} = 0 \\ E\left\{\lambda_i[n]\lambda_k[m]\right\} = 0 \text{ for } m \neq n \text{ or } i \neq k \end{array}\right\} \text{regardless of } x[n] \tag{12}$$

where $E\{u\}$ denotes the expected value of u.

As shown in Appendix A, the output of a DEM DAC can be written as

$$y(t) = \alpha(t)x\left[n_t\right] + \beta(t) + e_{\text{DAC}}(t) \tag{13}$$

where

$$\alpha(t) = 1 + \frac{1}{2\Delta}\sum_{i=1}^{N} m_i\left[e_{11i}(t) - e_{00i}(t) + e_{01i}(t) - e_{10i}(t)\right] \tag{14}$$

$$\beta(t) = \frac{1}{4}\sum_{i=1}^{N}\left[e_{11i}(t) + e_{00i}(t) + e_{01i}(t) + e_{10i}(t)\right] \tag{15}$$

and $e_{\text{DAC}}(t)$ is an error waveform that depends on the DAC input sequence, $x[n]$, the $e_i(t)$ waveforms, and the $\lambda_i[n]$ sequences. As $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ are T_s-periodic, so are $\alpha(t)$ and $\beta(t)$.

The desired signal component of the DAC output is the $\alpha(t)x[n_t]$ term in (13). It follows from the result shown in Appendix B that the continuous-time Fourier transform of the $\alpha(t)x[n_t]$ term in (13) is

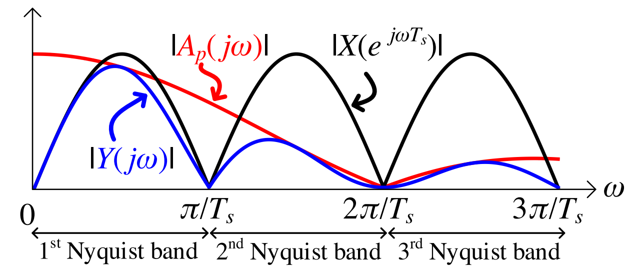

Fig. 6. Example of continuous-time Fourier transform of $\alpha(t)x[n_t]$.

$$\Im_{\text{CT}}\left\{\alpha(t)x\left[n_t\right]\right\} = A_p\left(j\omega\right)X\left(e^{j\omega T_s}\right) \tag{16}$$

where $A_p(j\omega)$ is the continuous-time Fourier transform of $\alpha(t)$ set to zero outside the interval $0 \leq t \leq T_s$, i.e., the continuous-time Fourier transform of

$$\alpha_p(t) = \begin{cases} \alpha(t) & \text{if } 0 \leq t \leq T_s \\ 0 & \text{otherwise} \end{cases} \tag{17}$$

and $X(e^{j\omega Ts})$ is the discrete-time Fourier transform of $x[n]$. This can be interpreted as the result of applying a linear time-invariant (LTI) filter with frequency response $A_p(j\omega)$ to an ideal continuous-time version of $x[n]$. In the absence of non-ideal circuit behavior, $A_p(j\omega)$ is the frequency response of a zero-order hold operation, i.e., a sinc frequency response. Example waveforms for this case are shown in Fig. 6. Although non-ideal circuit behavior causes $A_p(j\omega)$ to deviate somewhat from the ideal sinc frequency response, the deviation is linear and time-invariant, and it also tends to be relatively small. Hence, the deviation rarely results in a significant performance degradation.

The $\beta(t)$ term in (13) is T_s-periodic, so it consists only of tones at multiples of f_s. As these tones do not fall within any Nyquist band of the DAC output and do not depend on the DAC input, they do not cause significant problems in most DAC applications.

Unfortunately, the $e_{\text{DAC}}(t)$ term in (13) can be problematic in applications. As shown in Appendix A, it can be written as

$$e_{\text{DAC}}(t) = e_{\text{MM}}(t) + e_{\text{ISI-linear}}(t) + e_{\text{ISI-nonlinear}}(t) + e_{\text{ISI-noise}}(t) \tag{18}$$

where $e_{\text{MM}}(t)$ is error that arises from component mismatches and non-instantaneous rise and fall transitions but not ISI, and the three other terms are different types of error that arise from ISI. Therefore, these latter terms are all zero if (9) holds for all of the 1-bit DACs. Expressions for each of the terms in (18) are derived in Appendix A and explained below. The expressions show that $e_{\text{ISI-linear}}(t)$ is linearly related to a delayed version of the DAC input, and $e_{\text{ISI-nonlinear}}(t)$ is a second-order distorted version of the DAC input. They also show that if the DEM encoder is such that (12) holds, then $e_{\text{MM}}(t)$ and $e_{\text{ISI-noise}}(t)$ are noise-like terms that are uncorrelated with the DAC input.

The $e_{\mathrm{MM}}(t)$ expression is

$$e_{\mathrm{MM}}(t) = \sum_{i=1}^{N} \varepsilon_i(t)\lambda_i[n_t] \tag{19}$$

where each $\varepsilon_i(t)$ is a T_s-periodic waveform given by

$$\varepsilon_i(t) = \frac{e_{11i}(t) - e_{00i}(t) + e_{01i}(t) - e_{10i}(t)}{2\Delta}. \tag{20}$$

Hence, if (12) is satisfied $e_{\mathrm{MM}}(t)$ is a noise-like waveform that is zero-mean and uncorrelated with the DAC input. Given that each $\lambda_i[n]$ sequence is white, the spectral shape of the noise is a weighted sum of the magnitude squared of the continuous-time Fourier transforms of the $\varepsilon_i(t)$ waveforms set to zero outside the time interval $0 \le t \le T_s$ (this follows from the result presented in Appendix B). If the 1-bit DACs do not introduce ISI, i.e., if each 1-bit DAC satisfies (9), then $e_{\mathrm{MM}}(t)$ is equivalent to the $e_{\mathrm{DAC}}(t)$ expression derived in [20].

The $e_{\text{ISI-linear}}(t)$ expression is

$$e_{\text{ISI-linear}}(t) = \underbrace{\left(\frac{1}{\Delta}\sum_{i=1}^{N} m_i\gamma_i(t)\right)}_{\triangleq\,\gamma(t)} x[n_t - 1] \tag{21}$$

where each $\gamma_i(t)$ is a T_s-periodic waveform given by

$$\gamma_i(t) = \frac{1}{2}\left[e_{11i}(t) - e_{00i}(t) - e_{01i}(t) + e_{10i}(t)\right]. \tag{22}$$

As $\gamma(t)$ is a linear combination of the $\gamma_i(t)$ waveforms, it too is T_s-periodic. It follows that $e_{\text{ISI-linear}}(t)$ has the same general form as the DEM DAC's desired signal except for a one-period delay and a factor of $\gamma(t)$ instead of $\alpha(t)$. Thus, similar to the DEM DAC's desired signal component, $e_{\text{ISI-linear}}(t)$ is equivalent to the result of applying an LTI filter to an ideal continuous-time version of $x[n-1]$. Although it is an error component, it represents linear error and also the magnitude of $\gamma(t)$ tends to be much smaller than $\alpha(t)$ in practice, so $e_{\text{ISI-linear}}(t)$ is rarely problematic in applications.

The $e_{\text{ISI-nonlinear}}(t)$ expression is

$$e_{\text{ISI-nonlinear}}(t) = \underbrace{\left(\frac{1}{\Delta^2}\sum_{i=1}^{N} m_i^2\eta_i(t)\right)}_{\triangleq\,\eta(t)} x[n_t]\,x[n_t - 1] \tag{23}$$

where each $\eta_i(t)$ is a T_s-periodic waveform given by

$$\eta_i(t) = e_{11i}(t) + e_{00i}(t) - e_{01i}(t) - e_{10i}(t). \tag{24}$$

As $\eta(t)$ is a linear combination of the $\eta_i(t)$ waveforms, it too is T_s-periodic. It follows that $e_{\text{ISI-nonlinear}}(t)$ is equivalent to the result of applying an LTI filter to an ideal continuous-time version of $x[n]x[n-1]$. Unfortunately, this is a nonlinear function of the DAC input. As illustrated in Fig. 7, $x[n]x[n-1]$ is proportional to $(x[n]+x[n-1])^2 - (x[n]-x[n-1])^2$ so it can be viewed as the combination of two 2-tap FIR filtered versions of $x[n]$ each passed through a memoryless square law nonlinearity. Consequently, $e_{\text{ISI-nonlinear}}(t)$ is pure second-order distortion that is not addressed by DEM. It is present regardless of whether DEM is used.

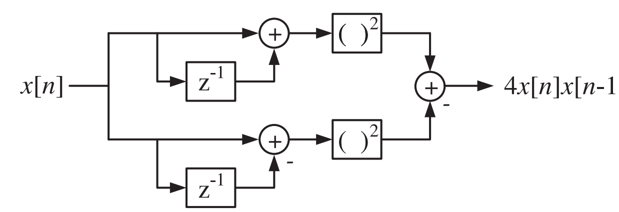

Fig. 7. Second-order nonlinearity caused by ISI.

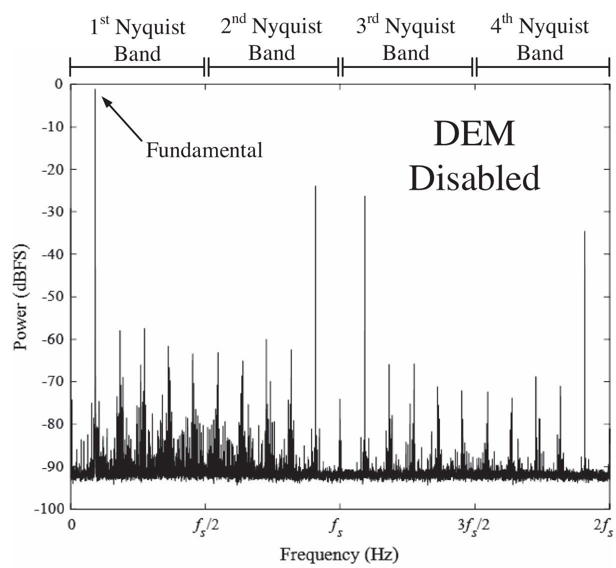

Fig. 8. Power spectrum of the simulated DAC output with DEM disabled.

The $e_{\text{ISI-noise}}(t)$ expression is

$$e_{\text{ISI-noise}}(t) = \sum_{i=1}^{N}\Bigg[\left(\lambda_i[n_t]\lambda_i[n_t-1] + m_i x[n_t]\lambda_i[n_t-1] + m_i x[n_t-1]\lambda_i[n_t]\right)\frac{\eta_i(t)}{\Delta^2} + \lambda_i[n_t-1]\frac{\gamma_i(t)}{\Delta}\Bigg]. \tag{25}$$

Each term in the expression is proportional to either $\lambda_i[n_t]$, $\lambda_i[n_t-1]$, or $\lambda_i[n_t]\lambda_i[n_t-1]$, so if (12) holds then $e_{\text{ISI-noise}}(t)$ is a noise-like waveform that is zero-mean and uncorrelated with $x[n]$ similar to $e_{\mathrm{MM}}(t)$. Consequently, the $e_{\text{ISI-noise}}(t)$ term increases the noise power of the DEM DAC output relative to cases in which ISI is avoided, but it does not introduce harmonic distortion provided (12) is satisfied. However, DEM DACs designed to spectrally shape the error arising from component mismatches do not satisfy (12). In such cases the term in $e_{\text{ISI-noise}}(t)$ proportional to $\lambda_i[n_t]\lambda_i[n_t-1]$ can sometimes introduce harmonic distortion via a mechanism similar to that explained in [38].

Computer simulation results that demonstrate the findings presented above for DACs with NRZ current-steering 1-bit DACs are shown in Figs. 8 and 9. The figures show output power spectra of the 14-bit highly-segmented architecture

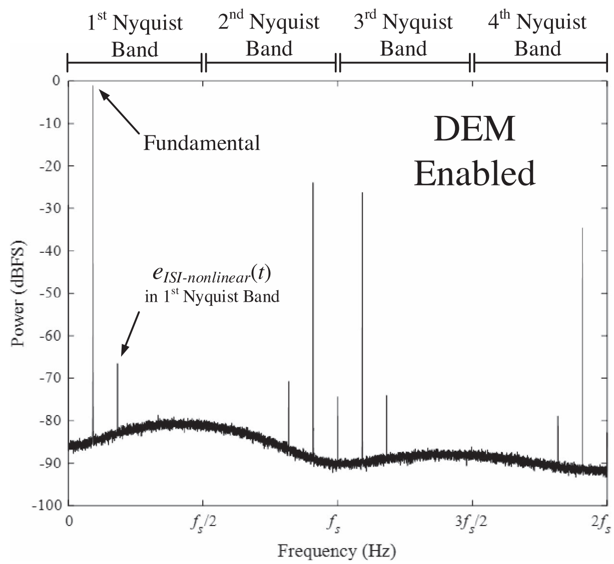

Fig. 9. Power spectrum of the simulated DAC output with DEM enabled.

presented in [20] with a -1 dBFS sinusoidal input signal of frequency $f_{\text{in}} = (0.091)f_s$. The simulated 1-bit DAC error waveforms, $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$, model static current mismatches and first-order (exponential) current transients. The MSB-element current mismatches and transient time-constants were chosen randomly from Gaussian distributions with standard deviations of 0.3% and 5%, respectively. Fig. 8 shows the DAC's output power spectrum with DEM disabled, i.e., with the encoder configured to be deterministic and memoryless and generate output bits that satisfy (7). Significant harmonic distortion from the 1-bit DAC errors in the form of spurious tones is visible in the power spectrum. Fig. 9 shows the DAC's output power spectrum with DEM enabled such that (12) is satisfied. As predicted by the findings described above, only second-order harmonic distortion is visible in the power spectrum when DEM is enabled.

V. Prior DEM DAC ISI Error Mitigation Techniques

A. RZ 1-bit DACs

In principle, ISI error can be avoided altogether if a DEM DAC contains only RZ 1-bit DACs, i.e., if (9) is satisfied by each 1-bit DAC. Unfortunately, such a DEM DAC typically has a lower desired signal power and a lower signal to noise and distortion ratio (SNDR) than a comparable DEM DAC based on NRZ 1-bit DACs. The lower signal power occurs because RZ 1-bit DACs cause the DEM DAC's desired signal component, $\alpha(t)x[n_t]$, to go to zero during the portion of each T_s clock period in which the RZ 1-bit DAC outputs go to zero. This happens because $\alpha(t)$ is a weighted sum of the $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ waveforms as indicated by (14). For example, with the RZ 1-bit DAC waveforms shown in Fig. 5, $\alpha(t)$ is nearly zero for almost half of every T_s clock period, so the power of the DEM DAC's desired signal component in any given Nyquist band is up to 6 dB lower than that of a comparable DEM DAC with NRZ 1-bit DACs.[3] The lower SNDR occurs because RZ 1-bit DACs and NRZ 1-bit DACs with comparable transient settling time constants have comparable transient errors. Hence, the difference in dB between the powers of the $e_{\text{DAC}}(t)$ waveforms for the two cases is smaller than the corresponding difference between the powers of the desired signal components.

These drawbacks of RZ 1-bit DACs typically are not offset by any reduction in power dissipation because RZ 1-bit DACs usually dissipate power even when the 1-bit DAC outputs go to zero. For example, current steering RZ 1-bit DACs typically implement the return-to-zero phase of each clock period by steering their output currents to dummy loads. Hence, their power consumption is not reduced during their return-to-zero phase. Moreover, generating the extra clock phase required to implement the RZ behavior dissipates additional power.

For these reasons, NRZ 1-bit DACs are often favored in high-speed Nyquist-rate DACs. However, as quantified by the findings of this paper, this choice generally comes with ISI error.

B. Balanced Rise and Fall Transitions

It has been suggested in prior work that DAC error from ISI is avoided if each 1-bit DAC's rising transient error is precisely the opposite of its falling transient error, i.e., $e_{01i}(t) = -e_{10i}(t)$ in the notation of this paper [2]. The results presented above indicate that this is not completely true. To avoid error from ISI altogether, every $\eta_i(t)$ and $\gamma_i(t)$ waveform must be zero, and this happens if and only if (9) is satisfied by each 1-bit DAC, i.e., if and only if RZ 1-bit DACs are used. However, it follows from (23) and (25) that for $e_{\text{ISI-nonlinear}}(t)$ and most of the terms in $e_{\text{ISI-noise}}(t)$ to be zero, it is sufficient for just every $\eta_i(t)$ waveform to be zero. As can be seen from (24), this happens when

$$e_{11i}(t) - e_{01i}(t) = -[e_{00i}(t) - e_{10i}(t)] \qquad (26)$$

for every 1-bit DAC. In practice, achieving (26) in every 1-bit DAC, while not eliminating error from ISI completely, eliminates its worst effects. Condition (26) reduces to the above-mentioned $e_{01i}(t) = -e_{10i}(t)$ condition for the special case where the only non-ideal 1-bit DAC behavior is from non-instantaneous output transitions.

C. ISI-Shaping

Another method of mitigating error from ISI is to combine an ISI-shaping algorithm with DEM such that $e_{\text{MM}}(t) + e_{\text{ISI-nonlinear}}(t) + e_{\text{ISI-noise}}(t)$ is zero-mean with a power spectrum that is second-order highpass shaped [36]. In the context of the results presented above, the objective is to choose each $\lambda_i[n]$ such that the terms in $e_{\text{ISI-noise}}(t)$ which are proportional to the $\eta_i(t)$ waveforms cancel the corresponding terms in $e_{\text{ISI-nonlinear}}(t)$. Given that the $\eta_i(t)$ waveforms vary

[3]The $A_p(j\omega)$ term in (16) for an RZ DAC that goes to zero for half of each clock period is a sinc function with half the amplitude of that of an NRZ DAC, although its roll-off is more gradual.

unpredictably with i, the above-mentioned cancellation must occur separately for each $\eta_i(t)$ term. It follows from (23) and (25) that for each $i = 1, 2, \ldots, N$, the factors of $\eta_i(t)$ in $e_{\text{ISI-nonlinear}}(t) + e_{\text{ISI-noise}}(t)$ can be grouped as

$$(m_i x[n] + \lambda_i[n])\,(m_i x[n-1] + \lambda_i[n-1])\,. \tag{27}$$

Therefore, the ISI-shaping algorithm must ensure that (27) is a zero-mean sequence with a second-order highpass spectral shape for each $i = 1, 2, \ldots, N$.

Unfortunately, it follows from (27) that this can only happen if each $\lambda_i[n]$ is correlated with the DAC input. One consequence is that such ISI-shaping algorithms are not compatible with DEM encoders that implement (12), i.e., the type of DEM encoders most appropriate for high-speed Nyquist-rate DACs. Another consequence is that the power spectrum of $e_{\text{DAC}}(t)$ in DEM DACs with ISI-shaping algorithms inevitably contain harmonic distortion. This is most likely the cause of the spurious tones visible in the output spectra from the ISI-shaping DEM DAC presented in [36], although its overall performance is very impressive.

VI. ISI Nonlinear Distortion Cancellation

As shown in Section IV, ISI causes a second-order distortion term in the output of a DEM DAC, i.e., $e_{\text{ISI-nonlinear}}(t) = \eta(t)x[n_t]x[n_t-1]$, where $\eta(t)$ is a T_s-periodic waveform that depends on the 1-bit DAC errors. In many applications, $e_{\text{ISI-nonlinear}}(t)$ is far more problematic than the DAC's other error terms. This section describes a digital technique that can suppress $e_{\text{ISI-nonlinear}}(t)$ within the DEM DAC's first Nyquist band provided $\alpha(t)$ and $\eta(t)$ are known a priori (e.g., through measurement as part of a calibration algorithm).

The idea is to pre-distort the DEM DAC input. This is done by setting the DEM DAC input sequence to be

$$x_{pd}[n] = x[n] + x_c[n] \tag{28}$$

where $x[n]$ is the original input sequence and $x_c[n]$ is a correction sequence that causes a term in the DEM DAC's output that cancels $e_{\text{ISI-nonlinear}}(t)$ over the first Nyquist band.

The $x_c[n]$ sequence is chosen such that

$$A_p(j\omega)\,X_c\!\left(e^{j\omega T_s}\right) + I_p(j\omega)\,X_{\text{ISI-nonlinear}}\!\left(e^{j\omega T_s}\right) \cong 0 \tag{29}$$

for all $|\omega| < \pi f_s$, where $X_c(e^{j\omega T_s})$ is the discrete-time Fourier transform of $x_c[n]$, $I_p(j\omega)$ is the continuous-time Fourier transform of $\eta(t)$ set to zero outside the interval $0 \le t \le T_s$, and $X_{\text{ISI-nonlinear}}(e^{j\omega T_s})$ is the discrete-time Fourier transform of $x_{pd}[n]x_{pd}[n-1]$. The first term on the left side of (29) is the part of the DEM DAC's desired signal component corresponding to $x_c[n]$, and the second term on the left side of (29) is the continuous-time Fourier transform of $e_{\text{ISI-nonlinear}}(t)$ with $x[n_t]$ replaced by $x_{pd}[n_t]$ in (23). Therefore when (29) is satisfied for all $|\omega| < \pi f_s$, $e_{\text{ISI-nonlinear}}(t)$ is approximately cancelled over the DEM DAC's first Nyquist band.

The discrete-time Fourier Transform of $x_c[n]$ is T_s-periodic whereas $A_p(j\omega)$ and $I_p(j\omega)$ are aperiodic functions that are not equal. Consequently, it is only possible to choose $x_c[n]$ such

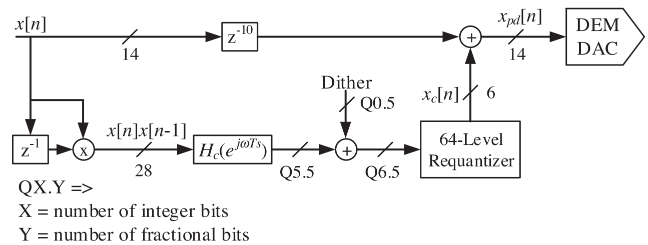

Fig. 10. ISI distortion cancellation technique.

that (29) holds for one T_s-period. This is why $e_{\text{ISI-nonlinear}}(t)$ is only cancelled over the first Nyquist band. Alternatively, $x_c[n]$ could be chosen to cancel $e_{\text{ISI-nonlinear}}(t)$ over the kth Nyquist band for any particular $k = 2, 3, \ldots$, provided $A_p(j\omega)$ is nonzero over the kth Nyquist band.

For a DEM DAC with ideal 1-bit DACs, $\alpha(t) = 1$ and $\eta(t) = 0$, but 1-bit DAC errors cause $\alpha(t)$ and $\eta(t)$ to deviate from these ideals as described in Section IV. Still, in practical, well-designed DEM DACs the deviation tends to be small enough that the power of $e_{\text{ISI-nonlinear}}(t)$ is much lower than the power of the desired signal component over the first Nyquist band. For instance, the simulation results shown in Fig. 9 for the example DEM DAC indicate that the power of $e_{\text{ISI-nonlinear}}(t)$ in the first Nyquist band is more than 65 dB lower than that of the desired signal component. It follows that the mean squared value of the $x_c[n]$ sequence required to cancel $e_{\text{ISI-nonlinear}}(t)$ in the first Nyquist band is much smaller than the mean squared value of $x[n]$. This implies that

$$X_{\text{ISI-nonlinear}}\left(e^{j\omega T_s}\right) \cong \Im_{\text{DT}}\left\{x[n]x[n-1]\right\} \tag{30}$$

where $\Im_{\text{DT}}$ denotes the discrete-time Fourier transform.

Substituting (30) into (29) and solving for $X_c(e^{j\omega T_s})$ indicates that $x_c[n]$ could be synthesized by passing $x[n]x[n-1]$ through a digital filter with a frequency response that approximates $-I_p(j\omega)/A_p(j\omega)$ for $|\omega| < \pi f_s$. However, a practical problem arises in that a digital filter with this frequency response would be non-causal. This problem can be addressed by synthesizing a digital filter that approximates the desired frequency response but with an integer-valued group delay, P, and either driving it with $x[n]x[n-1]$ advanced by P samples, or setting the DEM DAC input to be $x_{pd}[n] = x[n-P] + x_c[n]$.

A system-level diagram of an example implementation is shown in Fig. 10. The DEM DAC is identical to that described above. The digital filter is a 21-tap FIR filter with approximate frequency response

$$H_c\left(e^{j\omega T_s}\right) \cong -e^{-j\omega P T_s}\frac{I_p(j\omega)}{A_p(j\omega)} \text{ for } |\omega| \le \pi f_s \tag{31}$$

where $P = 10$. The digital filter was designed in three steps. First, the Parks-McClellan algorithm was used to generate a zero-phase filter with optimum magnitude response [39], [40]. Second, the zero-phase filter was delayed by P samples in order to be made causal. Finally, the causal filter was fractionally delayed [41] in order to better approximate the non-integer group delay implied by solving (31) for the randomly generated

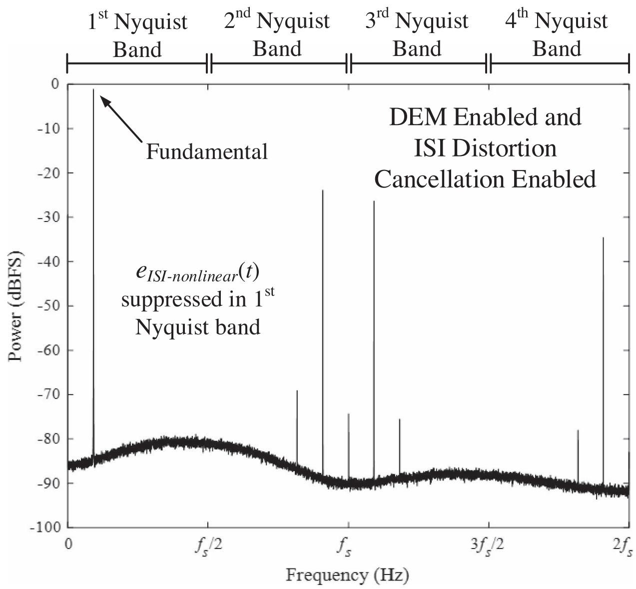

Fig. 11. DAC output with DEM enabled and ISI distortion cancellation enabled.

mismatches. The filter has fractional impulse response values, so its output has finer resolution than the 14-bit DEM DAC can accommodate directly. Therefore, dithered requantization was applied to quantize the filter's output to 6 bits without introducing harmonic distortion [42].

Fig. 11 shows the simulated DEM DAC output spectrum for this system. The simulated DEM DAC and the corresponding $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$ waveforms are identical to those used to generate the power spectrum shown in Fig. 9, but as can be seen from a comparison of Figs. 9 and 11 the addition of $x_c[n]$ suppresses $e_{\text{ISI-nonlinear}}(t)$ in the first Nyquist band of the power spectrum of Fig. 11.

In practice $\alpha(t)$ and $\eta(t)$ are not known a priori so they would have to be measured as part of a calibration system. For example, this could be done with a foreground calibration algorithm that estimates $H_c(e^{j\omega Ts})$ at several uniformly spaced values of ω between 0 and π and then calculates the corresponding FIR filter coefficient values via an inverse fast Fourier transform of the vector of estimates. Each estimate would be obtained via an LMS algorithm [43]. For each value of ω, $x[n]$ in the system of Fig. 10 would be set to a full-scale sinusoid with a frequency of $\omega/2$, an ADC with appropriate filtering would measure the second harmonic of the sinusoid in the DAC's first Nyquist band, and the LMS algorithm would adjust the corresponding value of $H_c(e^{j\omega Ts})$ to zero the measured second harmonic.

VII. Conclusion

This paper quantifies the combined effects of 1-bit DAC mismatches, non-instantaneous rise and fall transitions, and ISI on the continuous-time outputs of DEM DACs. The results apply to most multi-bit DAC architectures and all types of DEM known to the authors, and they reduce to previously published continuous-time DEM DAC results in the absence of ISI. Previously published ISI analyses model ISI as an input-referred discrete-time sequence, so they do not quantify the effects of ISI within individual Nyquist bands. This is acceptable in applications such as $\Delta\Sigma$ ADCs wherein the DEM DAC outputs are sampled, but in other applications the signals of interest typically lie in individual Nyquist bands. The results of this paper address the needs of these latter applications in that they quantify the error within each Nyquist band. As demonstrated in the paper, they make it possible to devise algorithms that cancel error in the Nyquist band of interest. The results also lead to several new insights such as the observation that for certain types of DEM the only nonlinear distortion caused by ISI is second-order distortion.

Appendix A

As indicated in (8), at any given time, t, the error of the ith 1-bit DAC, $e_i(t)$, is equal to one of $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, or $e_{10i}(t)$, depending on the state of $c_i[n_t]$ and $c_i[n_t-1]$. Given that $c_i[n]$ is either 0 or 1 for each i and t, it follows that (8) can be rewritten as:

$$\begin{aligned} e_i(t) = {} & (c_i[n_t-1])(c_i[n_t])e_{11i}(t) + (1-c_i[n_t-1])(c_i[n_t])e_{01i}(t) \\ & + (1-c_i[n_t-1])(1-c_i[n_t])\,e_{00i}(t) \\ & + (c_i[n_t-1])(1-c_i[n_t])\,e_{10i}(t). \end{aligned} \tag{32}$$

Substituting (6) into (32) and the result into (5) gives an expression for the output of the ith 1-bit DAC. This expression can be arranged as

$$\begin{aligned} y_i(t) = {} & x_i[n_t]\,\alpha_i(t)K_i\Delta + \beta_i(t) + x_i[n_t-1]\,\gamma_i(t) \\ & + x_i[n_t]\,x_i[n_t-1]\,\eta_i(t) \end{aligned} \tag{33}$$

where

$$\alpha_i(t) = 1 + \frac{1}{2}\frac{e_{11i}(t) - e_{00i}(t) + e_{01i}(t) - e_{10i}(t)}{K_i\Delta} \tag{34}$$

$$\beta_i = \frac{1}{4}\left[e_{11i}(t) + e_{00i}(t) + e_{01i}(t) + e_{10i}(t)\right] \tag{35}$$

$\gamma_i(t)$ is given by (22), and $\eta_i(t)$ is given by (24). Fig. 12 shows example $\alpha_i(t)$, $\beta_i(t)$, $\gamma_i(t)$, and $\eta_i(t)$ waveforms corresponding to the 1-bit DAC example shown in Fig. 4.

Combining (6) and (10) gives

$$x_i[n_t]\Delta = m_i x[n_t] + \lambda_i[n_t]. \tag{36}$$

Substituting this into (33) and the result into (4) gives

$$\begin{aligned} y(t) = \sum_{i=1}^{N} & (m_i x[n_t] + \lambda_i[n_t])\alpha_i(t)K_i + \beta_i(t) \\ & + (m_i x[n_t-1] + \lambda_i[n_t-1])\,\frac{\gamma_i(t)}{\Delta} \\ & + (m_i x[n_t] + \lambda_i[n_t])\,(m_i x[n_t-1] + \lambda_i[n_t-1])\,\frac{\eta_i(t)}{\Delta^2} \end{aligned} \tag{37}$$

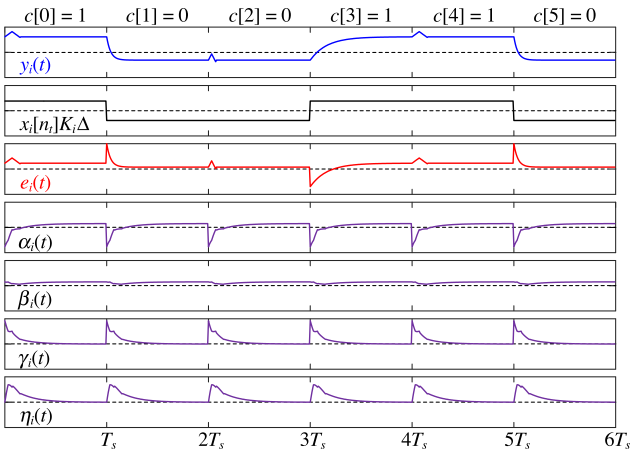

Fig. 12. $\alpha_i(t)$, $\beta_i(t)$, $\gamma_i(t)$, and $\eta_i(t)$ waveforms corresponding to the example $e_{11i}(t)$, $e_{01i}(t)$, $e_{00i}(t)$, and $e_{10i}(t)$, waveforms shown in Fig. 4.

collecting terms and applying (11) yields $y(t) = \alpha(t)x[n_t] + \beta(t) + e_{\mathrm{DAC}}(t)$ where $\alpha(t)$ is given by (14), $\beta(t)$ is given by (15), and $e_{\mathrm{DAC}}(t)$ is given by (18) through (25).

APPENDIX B

The result presented below in this sub-section is not new. However, the authors are not aware of a textbook or paper that presents it directly and it is necessary to explain the results of this paper, so it is derived below.

Let $a(t)$ be any T_s-periodic waveform, let $r[n]$ be any sequence, let

$$s(t) = a(t)r\left[\lfloor f_s t \rfloor\right] \tag{38}$$

and let

$$a_p(t) = \begin{cases} a(t) & \text{if } 0 \le t \le 1/f_s \\ 0 & \text{otherwise.} \end{cases} \tag{39}$$

Then $s(t)$ can be written as

$$s(t) = \sum_{n=-\infty}^{\infty} a_p\left(t - \frac{n}{f_s}\right) r[n]. \tag{40}$$

It follows that the continuous-time Fourier Transform of $s(t)$ is given by:

$$S(j\omega) = A_p(j\omega) \sum_{n=-\infty}^{\infty} r[n]e^{-j\omega n/f_s} = A_p(j\omega)R(e^{j\omega/f_s}) \tag{41}$$

where $A_p(j\omega)$ is the continuous-time Fourier Transform of $a_p(t)$ and $R(e^{j\omega/f_s})$ is the discrete-time Fourier transform of $r[n]$.

REFERENCES

[1] D. Mercer, "A 16-b D/A converter with increased spurious free dynamic range," *IEEE J. Solid-State Circuits*, vol. 29, no. 10, pp. 1180–1185, Oct. 1994.

[2] R. Adams, K. Nguyen, and TewksBury, "Dual return-to-zero pulse encoding in a DAC output stage," U.S. Patent 6 061 010, May 2000.

[3] S. Park, G. Kim, S.-C. Park, and W. Kim, "A digital-to-analog converter based on differential-quad switching," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1335–1338, Oct. 2002.

[4] K. Doris, J. Briaire, D. Leenaerts, M. Vertregt, and A. van Roermund, "A 12b 500 MS/s DAC with > 70 dB SFDR up to 120 MHz in 0.18 um CMOS," *IEEE ISSCC Dig. Tech. Papers 2005*, pp. 116–117.

[5] B. Schafferer and R. Adams, "A 3V CMOS 400 mW 14b 1.4 GS/s DAC for multi-carrier applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 360–362, 2004.

[6] Y. Tang, J. Briaire, K. Doris, R. van Veldhoven, P. van Beek, H. Johannes, A. Hegt, and A. van Roermund, "A 14-bit 200 MS/s DAC with SFDR > 78 dBc, IM3 < −83 dBc and NSD < −163 dBm/Hz across the whole nyquist band enabled by dynamic-mismatch mapping," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1371–1381, Jun. 2011.

[7] A. Bugeja and B.-S. Song, "A self-trimming 14-b 100-MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1841–1852, Dec. 2000.

[8] A. Bugeja, B.-S. Song, P. Rakers, and S. Gillig, "A 14-b 100-MS/s CMOS DAC designed for spectral performance," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1719–1732, Dec. 1999.

[9] E. Olieman, A.-J. Annema, and B. Nauta, "An interleaved full nyquist high-speed DAC technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 704–713, Mar. 2015.

[10] D. Spicer and A. Rodger, "Antiglitch digital-to-analog converter system," U.S. Patent 3 877 023, Apr. 1975.

[11] G. Engel, S. Kuo, and S. Rose, "A 14 b 3/6 GHz current-steering RF DAC in 0.18 μm CMOS with 66 dB ACLR at 2.9 GHZ," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 458–459.

[12] W. Schofield, D. Mercer, and L. Onge, "A 16 b 400 MS/s DAC with <−80 dBc IMD to 300 MHz and <−160 dBm/Hz noise power spectral density," in *Proc. ISSCC Dig. Tech. Papers*, 2003, pp. 126–482.

[13] Q. Huang, P. Francese, C. Martelli, and J. Nielsen, "A 200 MS/s 14b 97 mW DAC in 0.18 um CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 364–532.

[14] W.-H. Tseng, C.-W. Fan, and J.-T. Wu, "A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With > 70 dB SFDR up to 500 MHz," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2845–2856, Dec. 2011.

[15] R. Adams, K. Nguyen, and K. Sweetland, "A 113 dB SNR oversampling DAC with segmented noise-shaped scrambling," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 1998, pp. 62–63.

[16] R. van de Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 1976, pp. 148–149.

[17] L. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 267–273, Apr. 1989.

[18] B. Jewett, J. Liu, and K. Poulton, "A 1.2 Gs/s 15b DAC for precision signal generation," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 110–111.

[19] K. O. Sullivan, C. Gorman, M. Hennessy, and V. Callaghan, "A 12-bit 320-MSample/s current-steering CMOS D/A converter in 0.44 mm^2," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1064–1072, Jul. 2004.

[20] K. L. Chan, J. Zhu, and I. Galton, "Dynamic element matching to prevent nonlinear distortion from pulse-shape mismatches in high-resolution DACs," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2067–2078, Sep. 2008.

[21] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II: Analog Digit Signal Process.*, vol. 44, no. 10, pp. 808–817, Oct. 1997.

[22] I. Galton, "Why dynamic-element-matching DACs work," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 57, no. 2, pp. 69–74, Feb. 2010.

[23] W.-T. Lin, H.-Y. Huang, and T.-H. Kuo, "A 12-bit 40 nm DAC achieving SFDR > 70 dB at 1.6 GS/s and IMD < −61 dB at 2.8 GS/s with DEMDRZ technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 708–717, Mar. 2014.

[24] K. Chan, N. Rakuljic, and I. Galton, "Segmented dynamic element matching for high-resolution digital-to-analog conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3383–3392, Dec. 2008.

[25] F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453–460, Apr. 1995.

[26] I. Fujimori, A. Nogi, and T. Sugimoto, "A multibit delta-sigma audio DAC with 120-db dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1066–1073, Aug. 2000.

[27] R. Radke, A. Eshraghi, and T. Fiez, "A 15-Bit current-mode $\Sigma\Delta$ DAC based upon rotated data weighted averaging," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1074–1084, Aug. 2000.

[28] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\Sigma\Delta$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 42, no. 12, pp. 752–762, Dec. 1995.

[29] B. H. Leung and S. Sutarja, "Multibit $\Sigma - \Delta$ A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 39, no. 1, pp. 35–51, Jan. 1992.

[30] M. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent 5 138 317, Apr. 11, 1992.

[31] W. Redman-White and D. J. L. Bourner, "Improved dynamic linearity in multi-level $\Sigma - \Delta$ converters by spectral dispersion of D/A distortion products," *Proc. Eur. Conf. Circuit Theory Des.*, Sep. 1989, pp. 205–208.

[32] R. W. Adams and T. W. Kwan, "Data-directed scrambler for multi-bit noise-shaping D/A converters," U.S. Patent 5 404 142, Apr. 4, 1995.

[33] E. Tuijl, J. Homberg, D. Reefman, C. Bastiaansen, and L. Dussen, "A 128 fs, multi-bit $\Sigma\Delta$ CMOS audio DAC with real-time DEM and 115 dB SFDR," *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 368–369.

[34] T. S. Kaplan, J. F. Jensen, C. H. Fields, and M. F. Chang, "A 2-GS/s 3-bit $\Sigma\Delta$-modulated DAC with tunable bandpass mismatch shaping," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 603–610, Mar. 2005.

[35] T. Shui, R. Schreier, and F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 331–338, Mar. 1999.

[36] L. Risbo, R. Hezar, B. Kelleci, H. Kiper, and M. Fares, "Digital approaches to ISI-mitigation in high-resolution oversampled multi-level D/A converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2892–2903, Dec. 2011.

[37] A. Sanyal and N. Sun, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit $\Sigma\Delta$ modulators," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 5, no. 4, pp. 598–611, Dec. 2015.

[38] E. Familier, I. Galton, "A fundamental limitation of DC-free quantization noise with respect to nonlinearity-induced spurious tones," *IEEE Trans. Signal Process.*, vol. 61, no. 16, pp. 4172–4180, Aug. 2013.

[39] T. Parks and J. McClellan, "Chebyshev approximation for nonrecursive digital filters with linear phase," *IEEE Trans. Circuit Theory*, vol. CT-19, no. 2, pp. 189–194, Mar. 1972.

[40] J. McClellan and T. Parks, "A computer program for designing optimum FIR linear phase digital filters," *IEEE Trans. Audio Electroacoust.*, vol. AU-21, no. 6, pp. 506–526, Dec. 1973.

[41] T. Laakso, V. Valimaki, M. Karjalainen, and U. Laine, "Spliting the unit delay," *IEEE Signal Process. Mag.*, vol. 13, no. 1, pp. 30–60, Jan. 1996.

[42] R. A. Wannamaker, S. P. Lipshitz, J. Vanderkooy, and J. N. Wright, "A theory of nonsubtractive dither," *IEEE Trans. Signal Process.*, vol. 48, no. 2, pp. 449–516, Feb. 2000.

[43] B. Widrow, J. Glover, J. McCool, J. Kaunitz, C. Williams, R. Hearn, J. Zeidler, E. Dong, and R. Goodlin, "Adaptive noise canceling: Principles and applications," *Proc. IEEE*, vol. 64, no. 12, pp. 1692–1716, Dec. 1975.

Jason Remple received the B.S. degree from the University of California at Los Angeles, CA, USA, in 2005 and the M.S. degree from the University of California at San Diego (UCSD), CA, USA, in 2012, both in electrical engineering. He is currently working towards the Ph.D. degree at UCSD while working at Microchip Technology Inc. in San Diego, CA, USA.

Ian Galton (F'11) received the Sc.B. degree from Brown University, Providence, RI, USA, in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 1989 and 1992, respectively, all in electrical engineering.

Since 1996 he has been a Professor of Electrical Engineering at the University of California, San Diego, CA, USA, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996, he was with the University of California, Irvine, CA, USA, and prior to 1989 he was with Acuson and Mead Data Central. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters and phase-locked loops.

Dr. Galton has served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.