Quantization Noise Cancellation for FDC-Based Fractional-N PLLs

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***Abstract*—This paper presents a quantization noise cancellation technique for frequency-to-digital converter-based fractional-N phase-locked loops (FDC-PLLs). The technique cancels quantization noise prior to the loop filter so the PLL bandwidth can be increased without a significant phase noise penalty. The paper also presents an FDC-PLL architecture enhancement that achieves the effect of a charge pump offset current to improve linearity without the extra current source required by previous implementations.**

***Index Terms*—Charge pump offset current, delta-sigma ($\Delta\Sigma$), frequency-to-digital converter (FDC), frequency synthesizer, phase-locked loop (PLL), quantization noise.**

I. Introduction

FRACTIONAL-N phase-locked loops (PLLs) for frequency synthesis based on second-order delta-sigma ($\Delta\Sigma$) frequency-to-digital converters (FDC-PLLs) of the type shown in Fig. 1 have been shown to offer many of the advantages of both analog and digital PLLs [1], [2]. However, they inherit the same bandwidth versus phase noise tradeoff as analog PLLs and some digital PLLs: suppressing the quantization noise component of the PLL's phase noise comes at the expense of reducing the PLL's bandwidth. For example, in wireless transceiver local oscillator synthesis applications, this tradeoff typically limits analog PLL bandwidths to the order of tens of kHz [3].

In many applications it is desirable to increase the PLL bandwidth above such limits to reduce susceptibility to oscillator pulling, reduce PLL settling time, and enable in-loop carrier modulation. To this end, quantization noise cancellation (QNC) techniques have been proposed that relax the bandwidth versus phase noise tradeoff in both analog and digital PLLs [4]–[10]. The idea is to subtract much of the quantization noise prior to the loop filter so that the loop bandwidth can be increased without a significant phase noise penalty.

This paper presents and analyzes the first QNC technique applicable to FDC-PLLs. It extends the theoretical results presented in [1] to incorporate the QNC technique and demonstrates the findings via simulation and experimental results. The paper also presents a modification of the original FDC-PLL architecture that simplifies the charge pump relative to that presented in [2] without sacrificing performance.

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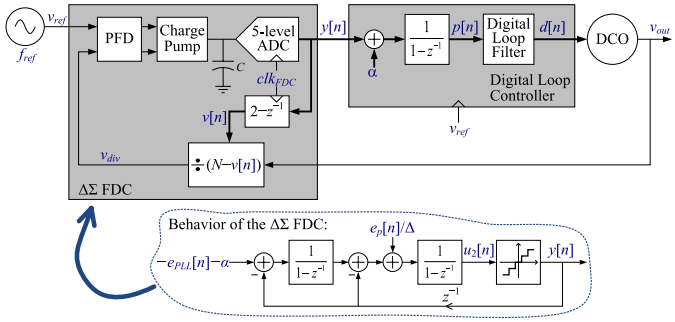

Fig. 1. Second-order $\Delta\Sigma$ FDC-based fractional-N PLL (FDC-PLL).

II. Quantization Noise Cancelling FDC-PLLs

The FDC-PLL proposed in this paper is shown in Fig. 2. It consists of a $\Delta\Sigma$ FDC, a digital loop controller (DLC), and a digitally controlled oscillator (DCO). Its output frequency is $f_{\rm PLL} = (N+\alpha)f_{\rm ref}$, where N is an integer, α is between -0.5 and 0.5, and $f_{\rm ref}$ is the reference oscillator frequency.

The $\Delta\Sigma$ FDC consists of a PFD, charge pump, integrating capacitor, ADC, $2-z^{-1}$ digital block, and multi-modulus divider. The charge pump consists of a positive current source and a negative current source. The positive current source is controlled by the top PFD output to generate a current pulse of amplitude I_{CP} each reference period when the PLL is locked. The negative current source is controlled by a one-shot to generate a current pulse of amplitude $-I_{CP}$ and fixed duration T_{OC} each reference period.

A $2^B \cdot 5$-level ADC of step-size $\Delta/2^B$, where $B \geq 0$, is used in place of the 5-level ADC of step-size Δ in Fig. 1. The variable, $-\hat{e}_q[n]$, is formed from the B least significant bits (LSBs) of the ADC output and used by the QNC technique to cancel much of the $\Delta\Sigma$ FDC's quantization noise prior to the loop filter. For the special case of $B=0, \hat{e}_q[n]=0$ in Fig. 2 so the QNC technique is not implemented.

In the remainder of this section it is first shown that without QNC (i.e., for $B=0$) the $\Delta\Sigma$ FDC in Fig. 2 performs the same signal processing as that in Fig. 1 when the PLLs are locked, but with the advantage that its charge pump requires two instead of three current sources. Then the result is extended for $B>0$ to cover the case with QNC.

A. Modified FDC-PLL Without QNC

Suppose the FDC-PLL in Fig. 1 is locked for all times $t \geq t_0$. For each $n=1,2,\ldots$, let t_n and τ_n be the times of the nth

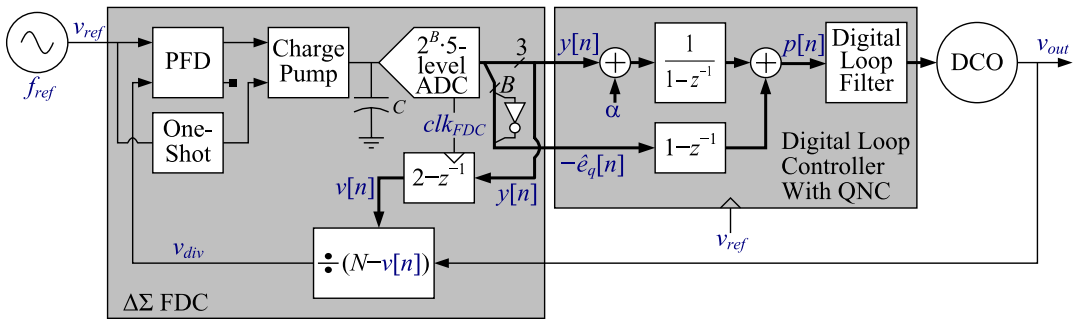

Fig. 2. Proposed FDC-PLL with quantization noise cancellation (QNC FDC-PLL).

rising edges after time t_0 of the reference oscillator output, $v_{\rm ref}(t)$, and the divider output, $v_{\rm div}(t)$, respectively.

The charge pump in the FDC-PLL of Fig. 1 consists of one positive and two negative current sources [2]. The top PFD output controls the positive current source to supply a current pulse of amplitude I_{CP} and duration of $\tau_n - t_n$ to the capacitor during the nth reference period if $t_n \le \tau_n$. The bottom PFD output controls one of the negative current sources to sink a current pulse of amplitude I_{CP} and duration of $t_n - \tau_n$ from the capacitor during the nth reference period if $t_n > \tau_n$. The second negative current source sinks a current pulse of amplitude I_{CP} and duration T_{OC} from the capacitor each reference period. The action of the latter current source induces a phase shift in the PLL output which causes the rising edge of $v_{\rm ref}(t)$ to lead the corresponding rising edge of $v_{\rm div}(t)$ by an average of T_{OC} [2], [5], [10]. The value of T_{OC} is chosen to ensure that $t_n \le \tau_n$ for all n, so only the positive current source is modulated by the $\Delta\Sigma$ FDC feedback loop once the PLL is locked. This prevents mismatches between positive and negative current sources from introducing nonlinear distortion.

The ADC samples the capacitor voltage shortly after each charge pump current pulse settles to zero. Therefore, the voltage sampled during the nth reference period is

$$V_c[n] = V_c[n-1] + (\tau_n - t_n)\frac{I_{CP}}{C} - T_{OC}\frac{I_{CP}}{C} + e_p[n] \quad (1)$$

where $e_p[n]$ represents error in the amount of charge delivered to the capacitor during the nth reference period from noise and other non-ideal circuit behavior in the charge pump, PFD, and divider.

The 5-level ADC output sequence is

$$y[n] = \frac{V_c[n]}{\Delta} + e_q[n] \quad (2)$$

where

$$e_q[n] = \left\lfloor \frac{V_c[n]}{\Delta} + \frac{1}{2} \right\rfloor - \frac{V_c[n]}{\Delta} \quad (3)$$

is the ADC quantization error during the nth reference period, and, for any value w, $\lfloor w \rfloor$ represents the largest integer not greater than w. Substituting (1) into (2) results in

$$y[n] - e_q[n] - (y[n-1] - e_q[n-1]) = (\tau_n - t_n)\frac{I_{CP}}{\Delta C} - T_{OC}\frac{I_{CP}}{\Delta C} + \frac{e_p[n]}{\Delta}. \quad (4)$$

Let $\psi_{\rm ref}[n]$ and $\psi_{\rm PLL}[n]$ be the average frequency errors over the nth reference period of the reference oscillator and PLL output, respectively. As proven in [1], provided that $I_{CP}/(C\Delta) = f_{\rm PLL}$, the signal processing performed by the $\Delta\Sigma$ FDC is equivalent to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 1. Hence, the ADC output sequence can be written as

$$y[n] = -\alpha - e_{\rm PLL}[n] + e_{\Delta\Sigma}[n] \quad (5)$$

where

$$e_{\rm PLL}[n] = \psi_{\rm PLL}[n] - \psi_{\rm ref}[n]\frac{f_{\rm PLL}}{f_{\rm ref}} - \frac{e_p[n] - e_p[n-1]}{\Delta} \quad (6)$$

represents the average frequency error of the PLL output over the nth reference period from all noise sources except $e_q[n]$, and

$$e_{\Delta\Sigma}[n] = e_q[n] - 2e_q[n-1] + e_q[n-2]. \quad (7)$$

Substituting (6) into (5) and the result into (4) gives

$$(\tau_n - t_n)f_{\rm PLL} = \psi_{\rm err}[n] + T_{OC}f_{\rm PLL} - 2e_q[n-1] + 3e_q[n-2] - e_q[n-3] \quad (8)$$

where

$$\psi_{\rm err}[n] = -\left(e_{\rm PLL}[n] - e_{\rm PLL}[n-1]\right) - \frac{e_p[n]}{\Delta}. \quad (9)$$

Thus, $\psi_{\rm err}[n]$ is the result of non-ideal circuit behavior and noise. By definition, $|e_q[n]| \le 0.5$, so (8) and (9) imply that

$$T_{OC} - \frac{3+R}{f_{\rm PLL}} < \tau_n - t_n < T_{OC} + \frac{3+R}{f_{\rm PLL}} \quad (10)$$

where R is the maximum magnitude of $\psi_{\rm err}[n]$. For example, measured results imply that $R \ll 1$ in the FDC-PLL presented in [2].

Therefore, $\tau_n - t_n$ is always positive, and, consequently, the nth rising edge of $v_{\rm div}(t)$ occurs after that of $v_{\rm ref}(t)$, if

$$T_{OC} > \frac{3+R}{f_{\rm PLL}}. \quad (11)$$

Provided (11) is satisfied, the second term on the right side of (1) is always positive once the FDC-PLL is locked so it can be implemented by sourcing a current pulse of magnitude I_{CP} and duration $\tau_n - t_n$ to the capacitor each reference period. The third term on the right side of (1) can be implemented sinking a current pulse of magnitude I_{CP} and duration T_{OC} from the capacitor each reference period. Hence, only two

current sources are necessary: one positive and one negative. The positive current source is identical to that in the FDC-PLL of Fig. 1. The negative current source is driven by a one-shot to generate a current pulse of amplitude $-I_{CP}$ and duration T_{OC} each reference period.

This configuration is shown in Fig. 2, where the top and bottom charge pump inputs control the positive and negative current sources, respectively, and the third current source has been eliminated. The ADC is clocked at time $t_n + T_{\rm delay}$ where $T_{\rm delay}$ is such that

$$\frac{N+\alpha}{f_{\rm PLL}} > T_{\rm delay} > \frac{3+R}{f_{\rm PLL}} + T_{OC} > \frac{2(3+R)}{f_{\rm PLL}} \tag{12}$$

so that the capacitor voltage is sampled shortly after each charge pump current pulse settles to zero, and the DCO input sequence is computed by the DLC before the $(n+1)$th reference rising edge occurs.

Therefore, once the FDC-PLL is locked, the behavior of the $\Delta\Sigma$ FDC of Fig. 2 is identical to that of Fig. 1 for the case of $B = 0$, even though the charge pump consists of two instead of three current sources. Prior to achieving lock, the two FDC-PLL versions do not have identical behavior, but extensive simulations run by the authors do not indicate that locking problems occur in the FDC-PLL of Fig. 2.

B. Quantization Noise Cancellation for FDC-PLLs

If B is a non-negative integer the output of the $2^B \cdot 5$-level ADC at the nth sample time is

$$s[n] = \frac{1}{2^B}\left\lfloor 2^B \frac{V_c[n]}{\Delta} \right\rfloor + \frac{1}{2} \tag{13}$$

and is represented as a $3+B$-bit two's complement binary number. The 3 most significant bits (MSBs) of $s[n]$ are the two's complement representation of the $y[n]$ sequence in Fig. 2. As shown below, for any $B \geq 0$ and for identical ADC input voltages, $y[n]$ takes on the same values as the 5-level ADC output sequence in Fig. 1. Hence, it follows from (5) and Section II-A that $y[n]$ contains second-order highpass-shaped quantization noise, $e_{\Delta\Sigma}[n]$, once the PLL is locked. The DLC accumulates $y[n]+\alpha$, which converts $e_{\Delta\Sigma}[n]$ to first-order highpass-shaped quantization noise given by $e_q[n] - e_q[n-1]$.

The B-bit two's complement sequence $-\hat{e}_q[n]$ in Fig. 2 consists of the B LSBs of $s[n]$ with their MSB inverted. It is an estimate of $-e_q[n]$ up to the resolution of the ADC.

The QNC technique computes the sequence $-(\hat{e}_q[n] - \hat{e}_q[n-1])$ through a first-order differentiator and adds it to the output of the DLC's accumulator. The contribution of the quantization error $e_q[n]$ to the FDC-PLL's output phase noise is thus cancelled to the extent that $\hat{e}_q[n]$ matches $e_q[n]$ and the $\Delta\Sigma$ FDC operates as an ideal second-order $\Delta\Sigma$ modulator so that (5), (6), and (7) hold.

C. $\Delta\Sigma$ FDC Equivalent Signal Processing

The $3+B$ bits used to represent $s[n]$ are denoted as $s_i[n]$, for $i = 0, \ldots, 2+B$, in the order of least to most significant bits. The numerical value of $s[n]$ is

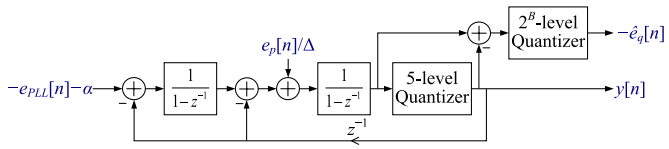

Fig. 3. Equivalent $\Delta\Sigma$ FDC signal processing for QNC FDC-PLLs.

$$s[n] = -4s_{2+B}[n] + \sum_{k=-1}^{B} 2^{-k} s_{-k+B}[n] \tag{14}$$

where the -4 coefficient for $s_{2+B}[n]$ stems from the two's complement representation of $s[n]$. The 3 MSBs of $s[n]$ are interpreted as the sequence

$$y[n] = -4s_{2+B}[n] + 2s_{1+B}[n] + s_B[n] \tag{15}$$

while, by design

$$-\hat{e}_q[n] = -\frac{1}{2}\left(1 - s_{-1+B}[n]\right) + \sum_{k=2}^{B} 2^{-k} s_{-k+B}[n]. \tag{16}$$

The $\Delta\Sigma$ FDC output $y[n]$ can be interpreted as the result of rounding $s[n] - 1/2$ to the nearest integer

$$y[n] = \lfloor s[n] \rfloor \tag{17}$$

so that, from (14) through (17)

$$\hat{e}_q[n] = y[n] - \left(s[n] - \frac{1}{2}\right) \tag{18}$$

can be regarded as the quantization error caused by such rounding operation.

Substituting (13) into (17) gives

$$y[n] = \left\lfloor \frac{\lfloor 2^B V_c[n]/\Delta \rfloor + 2^{B-1}}{2^B} \right\rfloor. \tag{19}$$

For any real number w, integer m and positive integer n, $\lfloor (\lfloor w \rfloor + m)/n \rfloor = \lfloor (w+m)/n \rfloor$ [11]. Hence, (19) gives

$$y[n] = \left\lfloor \frac{V_c[n]}{\Delta} + \frac{1}{2} \right\rfloor. \tag{20}$$

Therefore, $y[n]$ in the $\Delta\Sigma$ FDC of Fig. 2 is identical to $y[n]$ in the $\Delta\Sigma$ FDC in Fig. 1 at all sample times during which the ADC inputs in the two $\Delta\Sigma$ FDCs are equal. This result is independent of B, so the equations derived in Section II-A for the special case of $B = 0$ apply to the $\Delta\Sigma$ FDC in the FDC-PLL of Fig. 2 for any non-negative integer B.

Substituting (2) into (13), and the result into (18), gives

$$\hat{e}_q[n] = y[n] - \frac{1}{2^B}\left\lfloor 2^B y[n] - 2^B e_q[n] \right\rfloor. \tag{21}$$

For any real number w, and integer n, $\lfloor w+n \rfloor = \lfloor w \rfloor + n$ and (17) implies that $y[n]$ is integer-valued, so (21) reduces to

$$-\hat{e}_q[n] = \frac{1}{2^B}\left\lfloor -2^B e_q[n] \right\rfloor. \tag{22}$$

From (2) through (7), and (22), it follows that the signal processing performed by the $\Delta\Sigma$ FDC in Fig. 2 is as shown in Fig. 3 when the PLL is locked. The $y[n]$ output in Fig. 3 is

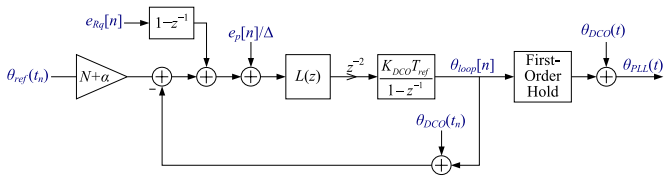

Fig. 4. Phase noise model of the proposed QNC FDC-PLL.

identical to that shown in Fig. 1 for FDC-PLLs without QNC. The $-\hat{e}_q[n]$ output is the estimate of $-e_q[n]$ used by the QNC technique to cancel $\Delta\Sigma$ FDC quantization noise prior to the digital loop filter.

D. Phase Noise Model for QNC FDC-PLLs

Given the equivalence between the $\Delta\Sigma$ FDC in Fig. 2 and that in Fig. 1 with respect to $y[n]$ as derived above, it follows from the corresponding result in [1] that the output of the accumulator in the DLC of Fig. 2 can be written as

$$-\theta_{\rm PLL}(\tau_n) + (N+\alpha)\theta_{\rm ref}(t_n) + \frac{e_p[n]}{\Delta} + e_q[n] - e_q[n-1] \tag{23}$$

where $\theta_{\rm PLL}(t)$ and $\theta_{\rm ref}(t)$ are the PLL's and reference oscillator's instantaneous phase noise in cycles, respectively. As indicated in Fig. 2, $-\hat{e}_q[n] + \hat{e}_q[n-1]$ is added to the output of the accumulator in the DLC to obtain $p[n]$. Thus, (23) and Fig. 2 imply that

$$p[n] = -\theta_{\rm PLL}(\tau_n) + (N+\alpha)\theta_{\rm ref}(t_n) + \frac{e_p[n]}{\Delta} + e_{\Delta\Sigma R}[n] \tag{24}$$

where

$$e_{\Delta\Sigma R}[n] = e_q[n] - e_q[n-1] - (\hat{e}_q[n] - \hat{e}_q[n-1])\,. \tag{25}$$

Therefore, QNC has the effect of replacing the $\Delta\Sigma$ FDC's quantization error term in the output of the DLC's accumulator, i.e., $e_q[n] - e_q[n-1]$, with the smaller error term, $e_{\Delta\Sigma R}[n]$, given by (25).

Hence, the phase noise model presented in [1] for the FDC-PLL shown in Fig. 1 can be extended to apply to the proposed FDC-PLL with QNC by replacing $e_q[n] - e_q[n-1]$ by $e_{\Delta\Sigma R}[n]$ in the result corresponding to (23) in the phase noise model derivation presented in [1].

By rearranging terms in (25), $e_{\Delta\Sigma R}[n]$ can be written as

$$e_{\Delta\Sigma R}[n] = e_{Rq}[n] - e_{Rq}[n-1] \tag{26}$$

where

$$e_{Rq}[n] = e_q[n] - \hat{e}_q[n]. \tag{27}$$

The phase noise model shown in Fig. 4 for the proposed FDC-PLL with QNC follows from (24) and (26) by replacing $e_q[n]$ with $e_{Rq}[n]$ as the input to the first-order differentiator in the phase noise model in [1].

As $e_q[n] = \hat{e}_q[n] + e_{Rq}[n]$, (24)–(26) imply that the FDC-PLL with QNC shown in Fig. 2 cancels the contribution of $\hat{e}_q[n]$ to the FDC-PLL's output phase noise, but does not cancel the contribution of $e_{Rq}[n]$. Although $e_{Rq}[n]$ is not cancelled, it can be made much smaller than $e_q[n]$ by increasing the number of quantization levels in the ADC.

In the presence of an arbitrarily small random noise component in $e_{\rm PLL}[n]$, for any integer n_1 $e_q[n_1]$ and $e_q[n_1+n_2]$ asymptotically converge in distribution as $n_2 \to \infty$ to a pair of independent random variables that are each uniformly distributed between $-\Delta/2$ and $\Delta/2$ [12]. It follows from (22) and (27) that $e_{Rq}[n_1]$ and $e_{Rq}[n_1+n_2]$ asymptotically converge in distribution as $n_2 \to \infty$ to a pair of independent random variables that are each uniformly distributed between 0 and $2^{-B}\Delta$. Consequently, for the purpose of deriving its power spectral density (PSD), $e_{Rq}[n]$ is equivalent to a white, uniformly distributed random process of variance $2^{-2B}\Delta^2/12$.

Assuming that $\theta_{\rm ref}(t_n), e_p[n], e_{Rq}[n]$, and the DCO's instantaneous phase noise, $\theta_{\rm DCO}(t)$, can be modeled as uncorrelated, wide-sense stationary random processes, and that $\theta_{\rm ref}(tn)$, $e_p[n]$, and $\theta_{\rm DCO}(t)$ have zero-mean, the two-sided PSD of $\theta_{\rm PLL}(t)$ is the sum of two-sided PSD components that each correspond to one of the noise signals, i.e.,

$$S_{\theta_{\rm PLL}}(f) = S_{\theta_{\rm PLL}}(f)|_{\rm ref} + S_{\theta_{\rm PLL}}(f)|_{e_p} + S_{\theta_{\rm PLL}}(f)|_{e_{Rq}} + S_{\theta_{\rm PLL}}(f)|_{\rm DCO}\,. \tag{28}$$

The four terms from left to right on the right side of (28) are the components of the two-sided PSD of $\theta_{\rm PLL}(t)$ corresponding to $\theta_{\rm ref}(t_n)$, $e_p[n]$, $e_{Rq}[n]$, and $\theta_{\rm DCO}(t)$, respectively. The phase noise model of Fig. 4 implies the following expressions for these components:

$$S_{\theta_{\rm PLL}}(f)|_{\rm ref} = (N+\alpha)^2\,|G(f)|^2\,S_{\theta_{\rm ref}}(f) \tag{29}$$

$$S_{\theta_{\rm PLL}}(f)|_{e_p} = \frac{T_{\rm ref}}{\Delta^2}\sin^2(\pi T_{\rm ref} f)\,|G(f)|^2\,S_{e_p}(e^{j2\pi T_{\rm ref} f}) \tag{30}$$

$$S_{\theta_{\rm PLL}}(f)|_{e_{Rq}} = \frac{2^{-2B}T_{\rm ref}}{3}\sin^2(\pi T_{\rm ref} f)\,|G(f)|^2 \tag{31}$$

$$S_{\theta_{\rm PLL}}(f)|_{\rm DCO} = |1-G(f)|^2\,S_{\theta_{\rm DCO}}(f) \tag{32}$$

where $S_{\theta_{\rm ref}}(f)$ and $S_{\theta_{\rm DCO}}(f)$ are the two-sided phase noise PSDs in cycles squared per Hz of the reference, and DCO, respectively, $S_{e_p}(e^{j2\pi T_{\rm ref} f})$ is the two-sided discrete-time PSD of $e_p[n]$

$$G(f) = \frac{T(e^{j2\pi T_{\rm ref} f})}{1+T(e^{j2\pi T_{\rm ref} f})}\left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f}\right]^2 \tag{33}$$

and

$$T(z) = K_{\rm DCO}T_{\rm ref}L(z)\frac{z^{-2}}{1-z^{-1}} \tag{34}$$

is the discrete-time loop gain of the FDC-PLL. If the desired units of the PSD are radians squared per Hz, then (28) must be scaled by $4\pi^2$.

III. Implementation and Design Example

Fig. 5 shows output spectra with and without QNC enabled of a 3.5 GHz FDC-PLL designed to demonstrate the effect of the proposed quantization noise cancelling technique [13]. The PLL has a 10-level flash ADC, so $B = 1$. It dissipates 21 mW from 1.0 and 1.2 V supplies, has an active area of 0.56 mm^2, and is identical to the frequency synthesizer in [2] expect that in [2] the adder at the input of the digital loop filter in Fig. 2 is bypassed via a multiplexer. Although not implemented in [13],

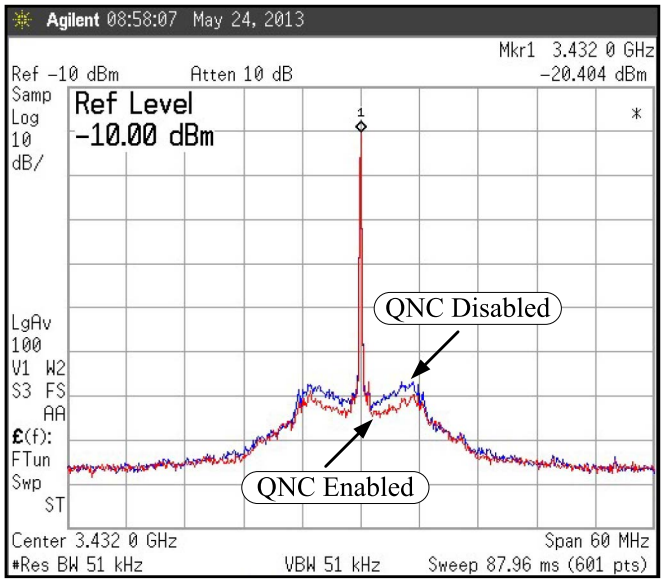

Fig. 5. Measured output phase noise of the QNC FDC-PLL in [13] with and without QNC enabled.

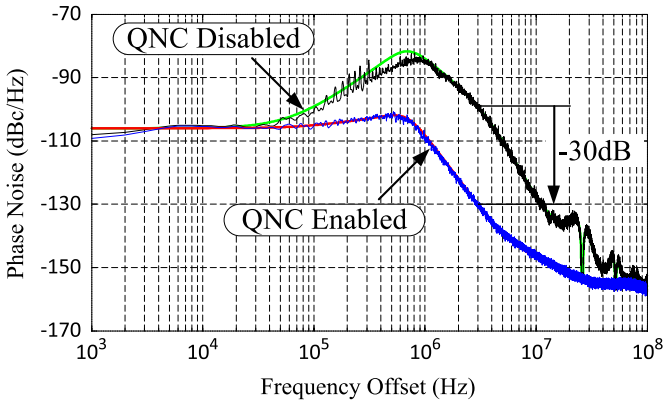

Fig. 6. Calculated PSD plots (smooth curves) and simulated PSD plots (jagged curves) for a 1 MHz bandwidth FDC-PLL with and without QNC enabled.

additional ADC levels would have enabled better $\Delta\Sigma$ quantization noise suppression.

As an example, Fig. 6 shows the phase noise PSD of an FDC-PLL that incorporates QNC with $B = 6$. The data were generated by an event-driven C-language simulator, with and without QNC enabled. A SAR ADC clocked at a rate of $f_{\rm ref}$ would be a practical means of achieving the ADC resolution required for $B = 6$ with a 1.13 mW increase in power dissipation over [13] and 0.026 mm^2 of additional active area [14]. Transistor-level periodic steady-state simulations were performed to estimate the noise levels used by the event-driven simulator [1].

In this design, the FDC-PLL's bandwidth is relaxed to 1 MHz without incurring a significant phase noise penalty as the majority of the $\Delta\Sigma$ FDC quantization noise is removed by QNC prior to the digital loop filter. The solid curves in Fig. 6 are the phase noise PSDs for the FDC-PLL with and without QNC enabled, as predicted by the phase noise model derived in Section II-D. Unlike in narrow-bandwidth FDC-PLLs [1], [2], where it is adequately suppressed by the digital loop filter, $\Delta\Sigma$ quantization noise dominates the output phase noise of the 1 MHz-bandwidth PLL at offset frequencies between 20 kHz and 100 MHz in absence of QNC. As a result, $e_{\rm PLL}[n]$ is correlated with ADC quantization error and the $\Delta\Sigma$ FDC operation departs from that of an ideal second-order $\Delta\Sigma$ modulator. Accordingly, the simulated phase noise PSD in absence of QNC deviates somewhat from the curve predicted by the phase noise model, as shown in Fig. 6.

When QNC is enabled, much of the $\Delta\Sigma$ quantization noise is suppressed prior to the digital loop filter. Hence, the phase noise PSD predicted by (28) through (34) closely matches the simulated phase noise PSD, which supports the results presented in this paper for FDC-PLLs with QNC.

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