A Linearized Model for the Design of Fractional-N Digital PLLs Based on Dual-Mode Ring Oscillator FDCs

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***Abstract*—A digital fractional-N phase-locked loop (PLL) frequency synthesizer based on a second-order $\Delta\Sigma$ frequency-to-digital converter (FDC) without conventional analog components was recently proposed and demonstrated experimentally to have performance in line with state-of-the-art analog PLLs. However, unlike analog PLLs or prior PLLs based on second-order $\Delta\Sigma$ FDCs, it is highly digital and does not require an analog charge pump or ADC, so it is well-suited to implementation in highly-scaled CMOS technology. This paper derives a linearized model of the new architecture and key equations which are necessary for the design of PLLs based on the architecture.**

***Index Terms*—Delta-sigma, digital PLL, FDC, frequency synthesizer.**

I. Introduction

FRACTIONAL-N phase-locked loop frequency synthesizers based on second-order delta-sigma ($\Delta\Sigma$) frequency-to-digital converters (FDCs), referred to as second-order FDC-PLLs in this paper, offer advantages of both analog and digital PLL frequency synthesizers [1]–[3]. In principle, they have the same quantization noise behavior as analog PLLs based on second-order $\Delta\Sigma$ modulators, so like such analog PLLs they can achieve very good spurious tone performance. Yet their loop filters are entirely digital so they are very compact like digital PLLs

Nevertheless, unlike digital PLLs, most prior second-order FDC-PLLs contain an analog charge pump and a coarse ADC. While such FDC-PLLs are not highly sensitive to non-ideal behavior of their charge pumps and ADCs, neither are they immune to it. In particular, the low supply voltages and high device leakage associated with highly-scaled CMOS technology result in non-ideal charge pump and ADC behavior that can limit FDC-PLL performance [3].

Recently, a new second-order FDC-PLL architecture that uses a dual-mode ring oscillator and digital logic instead of a charge pump and ADC was proposed and a prototype IC based on the architecture was demonstrated [4]. The new FDC-PLL avoids the above-mentioned issues associated with the charge pump and ADC so it is more amenable to implementation in highly-scaled CMOS technology than prior second-order FDC-PLLs.

This paper provides a detailed analysis of the new FDC-PLL architecture. It derives key equations and a linearized model which are necessary for the system-level design of the PLL. Section II provides a general description of fractional-N PLLs based on second-order $\Delta\Sigma$ FDCs. Section III describes the details of the new FDC-PLL, derives the key theoretical results of the paper with support from the Appendix, and describes the effects of non-ideal circuit behavior on the FDC-PLL's performance. Sections IV and V apply these results to develop the phase noise model and a design example.

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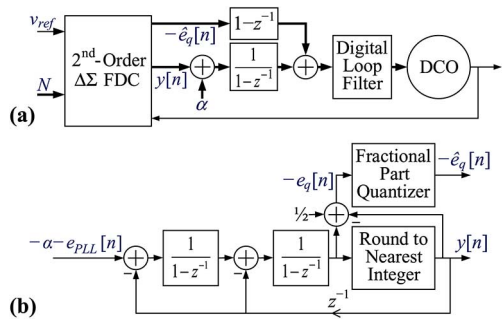

Fig. 1. (a) High-level diagram of an FDC-PLL with quantization noise cancellation (QNC), (b) signal processing equivalent of the $\Delta\Sigma$ FDC when it is locked.

II. FDC-PLL Overview

The FDC-PLL presented in [4] has the high-level architecture shown in Fig. 1(a). Its analog input is a reference oscillator signal, $v_{ref}(t)$, which, ideally, is periodic with frequency f_{ref}. Its output ideally is periodic with frequency $f_{PLL} = (N + \alpha)f_{ref}$, where N is an integer and α is a fractional value between -0.5 and 0.5.

The $\Delta\Sigma$ FDC within the FDC-PLL (the details of which are described in Section III) generates two f_{ref}-rate digital sequences, $y[n]$ and $-\hat{e}_q[n]$. As shown in Section III, the $y[n]$ sequence has the form

$$y[n] = -\alpha - e_{PLL}[n] + e_{\Delta\Sigma}[n] \tag{1}$$

where $e_{PLL}[n]$ is a measurement of the average frequency error of the PLL output over the nth reference period from all noise sources except quantization noise and $e_{\Delta\Sigma}[n]$ is identical to the highpass shaped quantization noise of a second-order $\Delta\Sigma$ modulator. Although no $\Delta\Sigma$ modulator is explicitly implemented within the $\Delta\Sigma$ FDC, its *behavior* is identical to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 1(b). Thus, $e_{\Delta\Sigma}[n]$ is equivalent to the result of passing the quantization error from rounding to the nearest integer through a highpass digital filter with transfer function $(1 - z^{-1})^2$ [5] The $-e_q[n]$ sequence shown in Fig. 1(b) is the fractional part of the output of the $\Delta\Sigma$

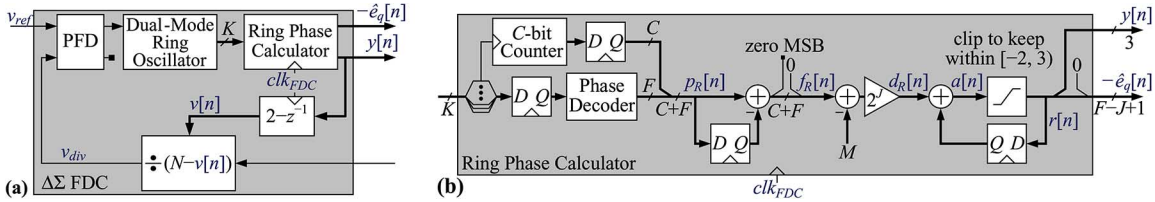

Fig. 2. (a) The new ring oscillator based ΔΣ FDC, (b) implementation details of the ring phase calculator within the ΔΣ FDC.

modulator's second accumulator, and $-\hat{e}_q[n]$ is a quantized version of $-e_q[n]$. It can verified from well-known properties of the second-order ΔΣ modulator that

$$e_{\Delta\Sigma}[n] = e_q[n] - 2e_q[n-1] + e_q[n-2] \tag{2}$$

The accumulator prior to the digital loop filter in the FDC-PLL operates on $y[n] + \alpha$, so it follows from (1) and (2) that its output is an accumulated version of $-e_{PLL}[n]$ plus $e_q[n] - e_q[n-1]$. The former is a measure of the PLL's phase error, and the latter is first-order highpass shaped quantization noise [2], [3]. Hence, each output sample of the accumulator is nearly proportional to the amount of charge in each charge pump pulse in an analog PLL with a second-order ΔΣ modulator. Consequently, if the $-\hat{e}_q[n]$ path shown in Fig. 1(a) is omitted, the FDC-PLL can be designed to have nearly the same loop dynamics and quantization noise performance as an analog PLL with a second-order ΔΣ modulator [2].

The $-\hat{e}_q[n]$ path shown in Fig. 1(a) performs quantization noise cancellation (QNC) [6]. By design, $\hat{e}_q[n]$ is approximately equal to $e_q[n]$, so the $-\hat{e}_q[n]$ path in the FDC-PLL of Fig. 1(a) approximately cancels $e_q[n] - e_q[n-1]$ prior to the digital loop filter. This allows the PLL bandwidth to be increased without significantly increasing the contribution of quantization noise to the PLL's phase noise. When QNC is not implemented, as is the case in the FDC-PLL presented in [3], the loop filter's bandwidth must be low enough to sufficiently attenuate the first-order highpass shaped quantization noise. QNC is a variant of similar techniques that have been applied to both analog and digital PLLs [7]–[11].

III. Ring Oscillator Based ΔΣ FDC

A. ΔΣ FDC Architecture

The ΔΣ FDC presented in this paper is a slightly generalized version of that presented in [4]. Its structure is shown in Fig. 2(a). It consists of a phase frequency detector (PFD), a dual-mode ring oscillator (DMRO), a digital ring phase calculator (the details of which are shown in Fig. 2(b)), a digital $2 - z^{-1}$ block, and a multi-modulus divider. The PFD and divider have the same functionality as those in an analog PLL, and the DMRO and ring phase calculator details are described below.

The DMRO is implemented as a ring of K nominally identical inverters. Each inverter has a propagation delay that is one of two values depending on whether the top PFD output, $u(t)$, is high or low. The nominal instantaneous output frequency of the DMRO (neglecting switching transients) is given by

$$f_{DMRO}(t) = \begin{cases} f_{high}, & \text{if } u(t) = 1, \\ f_{low}, & \text{if } u(t) = 0, \end{cases} \tag{3}$$

where $u(t)$ is the top PFD output, and f_{high} and f_{low} are constants. Ideally,

$$f_{high} - f_{low} = 2^{-J} f_{PLL} \tag{4}$$

and

$$f_{low} = \frac{M - 2^{-J} f_{PLL} T_{\bar{u}}}{T_{ref}} \tag{5}$$

where $T_{ref} = 1/f_{ref}$ is the reference period, J is an integer chosen under the constraint that $2^{1-J}K$ must be integer-valued, M is a positive integer, and $T_{\bar{u}}$ must satisfy

$$\frac{4}{f_{PLL}} < T_{\bar{u}} < \frac{T_{ref}}{2} - \frac{4}{f_{PLL}} \tag{6}$$

The reasons for (4)–(6) are explained in the context of the analysis presented in Section III-B. As shown via the analysis, when the FDC-PLL is locked $T_{\bar{u}}$ is the average PFD pulse width, and the DMRO is locked to an average frequency of Mf_{ref}. The integer J is a design parameter that specifies a tradeoff between the DMRO's frequency spread and its contribution to the FDC-PLL's overall phase noise. As explained shortly, it is not critical that (4) and (5) be satisfied exactly or that the frequency transitions are instantaneous.

The details of the ring phase calculator are shown in Fig. 2(b). Its input is the DMRO's set of K inverter outputs. The C-bit counter is clocked by one of the DMRO inverter outputs, so the counter increments once per DMRO cycle and rolls over modulo 2^C. The C counter bits are interpreted as an unsigned number in the range $\{0, 1, 2, \ldots, 2^C - 1\}$.

The ring phase calculator's clock signal, clk_{FDC}, is an inverted version of the reference, so its period is T_{ref}. The number of counter bits is chosen to satisfy

$$C \geq \log_2\left(\frac{f_{high}}{f_{ref}}\right) \tag{7}$$

As explained in Section III-B, this ensures that the counter rolls over no more than one time per clk_{FDC} period.

At any given time the C-bit counter output represents the integer part of the DMRO's phase modulo 2^C. Therefore, the fractional part of the phase goes to zero each time the counter output increments or rolls over.

Both the C-bit counter output and the K DMRO inverter outputs are sampled on each rising edge of clk_{FDC}. A phase decoder block that consists of combinatorial logic maps the K sampled inverter outputs to one of $2K$ possible quantized fractional phase values of the DMRO. Specifically, its nth output sample is the greatest number in the set $\{0, 1/(2K), 2/(2K), 3/(2K), \ldots, 1 - 1/(2K)\}$ that is less than or equal to the fractional part of the DMRO's phase at the time of the nth rising edge of clk_{FDC}. Consequently, its output is an unsigned fractional F-bit number. If K is a power of two, then $F = 1 + \log_2 K$. Otherwise, F must be larger than $1 + \log_2 K$ so the phase decoder output represents the set of fractional values with negligible round-off error.

The sequence $p_R[n]$ in Fig. 2(b) is the sum of the sampled counter output and the fractional phase decoder output. It is interpreted as an unsigned fixed-point sequence with the C sampled counter bits forming its integer part and the F fractional

phase decoder bits forming its fractional part. Thus, $p_R[n]$ is a quantized representation of the absolute DMRO phase in cycles measured at the nth rising edge of clk_{FDC} that rolls over modulo 2^C cycles.

The portion of the ring phase calculator to the right of $p_R[n]$ performs two's complement arithmetic.[1] The sequence $f_R[n]$ is obtained by performing a two's complement difference of $p_R[n]$ and $p_R[n-1]$, and replacing the MSB with zero. The clipping accumulator operates on $d_R[n] = 2^J(f_R[n]-M)$ and generates the output sequence

$$r[n] = \begin{cases} a[n], & \text{if } -2 \le a[n] < 3, \\ 3 - 2^{J-1}/K, & \text{if } a[n] \ge 3, \\ -2, & \text{if } a[n] < -2, \end{cases} \tag{8}$$

where

$$a[n] = r[n-1] + d_R[n] \tag{9}$$

The ring phase calculator output, $y[n]$, is an integer-valued two's complement sequence formed from the 3 MSBs of $r[n]$. The $-\hat{e}_q[n]$ output is a fractional two's complement sequence formed from the $F - J$ LSBs of $r[n]$ with an appended MSB set to 0.

B. The ΔΣ FDC's Equivalence to a ΔΣ Modulator

An oscillator's ideal instantaneous phase is the sum of a time function that represents its phase noise and the integral of its ideal frequency. Hence, the instantaneous phases of the reference oscillator, PLL output, and DMRO, respectively, in units of cycles are $p_{ref}(t) = f_{ref}t + \theta_{ref}(t)$, $p_{PLL}(t) = f_{PLL}t + \theta_{PLL}(t)$, and

$$p_{DMRO}(t) = \int_0^t f_{DMRO}(\tau)d\tau + \theta_{DMRO}(t) \tag{10}$$

where $\theta_{ref}(t)$, $\theta_{PLL}(t)$, and $\theta_{DMRO}(t)$ are the respective phase noise time functions.

The following definitions are used through the remainder of the paper. The time sequences, γ_n, t_n, and τ_n, for $n = 0, 1, 2, \ldots$, are the times of the nth rising edges of clk_{FDC}, the reference signal, and the divider output, respectively, after time $t = 0$. The phase noise changes per reference period of the PLL output, the reference signal, and the DMRO are defined as

$$\psi_{PLL}[n] = \theta_{PLL}(\tau_n) - \theta_{PLL}(\tau_{n-1}), \tag{11}$$

$$\psi_{ref}[n] = \theta_{ref}(t_n) - \theta_{ref}(t_{n-1}), \tag{12}$$

and

$$\psi_{DMRO}[n] = \theta_{DMRO}(\gamma_n) - \theta_{DMRO}(\gamma_{n-1}), \tag{13}$$

respectively. Therefore, $\psi_{ref}[n]$ and $\psi_{DMRO}[n]$ represent the average frequency errors multiplied by T_{ref} of the reference oscillator and DMRO, respectively. When the PLL is locked the average period of the divider output is the reference period, so $\psi_{PLL}[n]$ is approximately the average frequency error of the PLL output multiplied by T_{ref}.

Throughout the paper it is assumed that

$$|(N+\alpha)\psi_{ref}[n] - \alpha - \psi_{PLL}[n]| + 2^{J+1}\,|\psi_{DMRO}[n]| < 1 \tag{14}$$

for all $n \ge 0$. The α term on the left side of (14) has a magnitude bounded by 0.5, and the other terms have magnitudes that are much smaller than 0.5 in practical PLLs, so (14) is not a difficult requirement to meet.

PFD Pulse Width Derivation: The kth rising edge of the reference oscillator output, $v_{ref}(t)$, occurs at time t_k which is exactly the point in time at which the reference oscillator's instantaneous phase, $p_{ref}(t)$, crosses an integer boundary. Thus,

$$f_{ref}t_k + \theta_{ref}(t_k) = k \tag{15}$$

for each integer k. Subtracting (15) with $k = n-1$ from (15) with $k = n$ and applying $f_{PLL} = (N+\alpha)f_{ref}$, results in

$$f_{PLL}[t_n - t_{n-1}] = (N+\alpha)\,[1 - \theta_{ref}(t_n) + \theta_{ref}(t_{n-1})] \tag{16}$$

The $\Delta\Sigma$ FDC shown in Fig. 2 is configured such that the divider modulus during the nth reference period is $N - v[n-1]$, so there are exactly $N - v[n-1]$ DCO periods between the $(n-1)$th and nth rising edges of the divider output, i.e., the PLL output's phase change between time τ_{n-1} and time τ_n is $N - v[n-1]$ cycles. Therefore,

$$f_{PLL}\tau_n + \theta_{PLL}(\tau_n) - f_{PLL}\tau_{n-1} - \theta_{PLL}(\tau_{n-1}) = N - v[n-1] \tag{17}$$

which can be rewritten as

$$f_{PLL}[\tau_n - \tau_{n-1}] = N - v[n-1] - \theta_{PLL}(\tau_n) + \theta_{PLL}(\tau_{n-1}) \tag{18}$$

Subtracting (16) from (18), and applying (11), (12), and $v[n] = 2y[n] - y[n-1]$ gives

$$\begin{aligned}(\tau_n - t_n)f_{PLL} = (\tau_{n-1} - t_{n-1})f_{PLL} - 2y[n-1] + y[n-2] \\ -\psi_{PLL}[n] + (N+\alpha)\psi_{ref}[n] - \alpha\end{aligned} \tag{19}$$

Clipping Accumulator Input Derivation: The DMRO's maximum frequency is f_{high}, so its maximum phase change in cycles over a clk_{FDC} period (i.e., over a duration of $1/f_{ref}$) is f_{high}/f_{ref}. Hence, the number of counter bits dictated by (7) is large enough that the counter has at least as many levels as the maximum number of DMRO cycles over a clk_{FDC} period, so the counter rolls over no more than one time per clk_{FDC} period.

Zeroing the MSB following the $p_R[n] - p_R[n-1]$ calculation indicated in Fig. 2(b) has the effect of adding 2^C when $p_R[n] - p_R[n-1]$ is negative. Therefore,

$$f_R[n] = \begin{cases} p_R[n] - p_R[n-1] + 2^C, & \text{if } p_R[n] < p_R[n-1], \\ p_R[n] - p_R[n-1], & \text{otherwise.} \end{cases} \tag{20}$$

It follows from the definition of $p_R[n]$ in Section III-A that the only way $p_R[n]$ can be less than $p_R[n-1]$ is if the counter rolled over during the nth clk_{FDC} period, i.e., between the $(n-1)$th and nth rising clk_{FDC} edges. Each counter rollover has the effect of subtracting 2^C from what would otherwise be the counter's output value and only one rollover is possible per clk_{FDC} period. This with (20) implies that counter rollovers have no effect on $f_R[n]$.

Consequently, $f_R[n]$ can be written in terms of $p_{DMRO}(\gamma_n)$ as

$$f_R[n] = p_{DMRO}(\gamma_n) - p_{DMRO}(\gamma_{n-1}) + e_{Rq}[n] - e_{Rq}[n-1] \tag{21}$$

where

$$e_{Rq}[n] = \frac{1}{2K}\,\lfloor 2K\, p_{DMRO}(\gamma_n) \rfloor - p_{DMRO}(\gamma_n) \tag{22}$$

is DMRO quantization noise. It follows that $f_R[n]$ is a quantized representation of the DMRO's phase change in units of cycles over the nth clk_{FDC} period.

[1] Although not shown in Fig. 5, in practice a zero MSB would be appended to the bus that represents $p_R[n]$ to convert its format to two's complement notation without changing its value.

Substituting (3) into (10) and taking a first difference of the result gives

$$p_{DMRO}(\gamma_n) - p_{DMRO}(\gamma_{n-1}) = \int_{\gamma_{n-1}}^{\gamma_n} u(\tau)(f_{high} - f_{low})d\tau + f_{low}T_{ref} + \psi_{DMRO}[n] \quad (23)$$

Substituting (4) and (5) into this result gives

$$p_{DMRO}(\gamma_n) - p_{DMRO}(\gamma_{n-1}) = 2^{-J} f_{PLL} \left[\int_{\gamma_{n-1}}^{\gamma_n} u(\tau)d\tau - T_{\bar{u}} \right] + M + \psi_{DMRO}[n] \quad (24)$$

In the remainder of this section, it is assumed that the $\Delta\Sigma$ FDC is locked for all $n = 1, 2, 3, \ldots$. The Appendix derives the conditions under which the $\Delta\Sigma$ FDC becomes locked and proves that for all n at which it is locked the clipping accumulator does not clip and

$$\gamma_{n-1} < t_n < \tau_n < \gamma_n \quad (25)$$

By definition $u(t)$ goes to 1 at each time t_n and goes to 0 at each time τ_n, so (25) implies that (24) can be written as

$$p_{DMRO}(\gamma_n) - p_{DMRO}(\gamma_{n-1}) = 2^{-J} f_{PLL}[\tau_n - t_n - T_{\bar{u}}] + M + \psi_{DMRO}[n] \quad (26)$$

Substituting this into (21) and applying the operations shown in Fig. 2(b) prior to the clipping accumulator implies that the input to the clipping accumulator can be written as

$$d_R[n] = (\tau_n - t_n - T_{\bar{u}})f_{PLL} + 2^J (\psi_{DMRO}[n] + e_{Rq}[n] - e_{Rq}[n-1]) \quad (27)$$

Clipping Accumulator Output Derivation: As shown in the Appendix, when the $\Delta\Sigma$ FDC is locked the clipping accumulator does not clip, so, (8), (9), and (27) imply that for $k = 1, 2, \ldots$

$$r[k] = r[k-1] + (\tau_k - t_k - T_{\bar{u}})f_{PLL} + 2^J (\psi_{DMRO}[k] + e_{Rq}[k] - e_{Rq}[k-1]) \quad (28)$$

Solving (28) with $k = n-1$ for $(\tau_{n-1} - t_{n-1})f_{PLL}$, and substituting the result into (19), gives

$$\begin{aligned}(\tau_n - t_n)f_{PLL} &= T_{\bar{u}}f_{PLL} + r[n-1] - r[n-2] - 2y[n-1] + y[n-2] \\ &\quad - 2^J (\psi_{DMRO}[n-1] + e_{Rq}[n-1] - e_{Rq}[n-2]) \\ &\quad - \psi_{PLL}[n] + (N+\alpha)\psi_{ref}[n] - \alpha \end{aligned} \quad (29)$$

It follows from (59) in the Appendix that when the clipping accumulator does not clip, the truncation operation associated with forming $y[n]$ from the 3 MSBs of $r[n]$ causes

$$y[n] = a[n] + e_{yq}[n] \quad (30)$$

where

$$e_{yq}[n] = \lfloor a[n] \rfloor - a[n] \quad (31)$$

This with (8) and (29) gives

$$\begin{aligned}(\tau_n - t_n)f_{PLL} &= T_{\bar{u}}f_{PLL} - y[n-1] - e_q[n-1] + e_q[n-2] \\ &\quad - 2^J \psi_{DMRO}[n-1] - \psi_{PLL}[n] + (N+\alpha)\psi_{ref}[n] - \alpha \end{aligned} \quad (32)$$

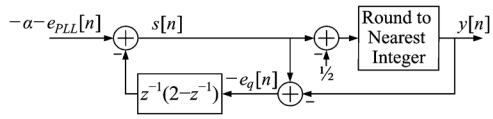

Fig. 3. Error feedback form of a second-order $\Delta\Sigma$ modulator.

where

$$e_q[n] = 2^J e_{Rq}[n] + e_{yq}[n] \quad (33)$$

Substituting (32) into (28) with $k = n$ gives

$$a[n] = s[n] + 2^J e_{Rq}[n] \quad (34)$$

where

$$\begin{aligned}s[n] = &-2e_q[n-1] + e_q[n-2] \\ &- \psi_{PLL}[n] + (N+\alpha)\psi_{ref}[n] - \alpha \\ &+ 2^J (\psi_{DMRO}[n] - \psi_{DMRO}[n-1]) \end{aligned} \quad (35)$$

$\Delta\Sigma$ *Modulator Equivalence:* Substituting (34) into (30) gives

$$y[n] = s[n] + e_q[n] \quad (36)$$

where $e_q[n]$ is given by (33). By definition, $y[n]$ is integer-valued. It is shown in the Appendix that $-1 < e_q[n] \leq 0$ when the $\Delta\Sigma$ FDC is locked, which implies that for each n, there is exactly one value of $e_q[n]$ that causes $s[n] + e_q[n]$ to be integer-valued. Consequently,

$$e_q[n] = \lfloor s[n] \rfloor - s[n] \quad (37)$$

Therefore, even though $e_q[n]$ is the result of quantization in two physical locations within the $\Delta\Sigma$ FDC, one following the DMRO and the other following the clipping accumulator, mathematically it is equivalent to the quantization error caused a single quantization operation, i.e., that of rounding $s[n]$ down to the nearest integer less than or equal to $s[n]$. Rounding any value, x, down to the nearest integer less than or equal to x, is the same as rounding $x - 1/2$ to the nearest integer.

This with (35) and (36) proves that when the $\Delta\Sigma$ FDC is locked, $y[n]$ is equivalent to that generated by the block diagram shown in Fig. 3, with

$$e_{PLL}[n] = \psi_{PLL}[n] - (N+\alpha)\psi_{ref}[n] - 2^J (\psi_{DMRO}[n] - \psi_{DMRO}[n-1]) \quad (38)$$

The block diagram shown in Fig. 3 is the error-feedback form of a second-order $\Delta\Sigma$ modulator, which is known to have the same input to $y[n]$ relationship as the second-order $\Delta\Sigma$ modulator shown in Fig. 1(b) under equivalent initial conditions [5]. It follows from the well-known behavior of second-order $\Delta\Sigma$ modulators, or, alternatively, from (35) through (38) that $y[n]$ can be written as

$$y[n] = -\alpha - e_{PLL}[n] + e_q[n] - 2e_q[n-1] + e_q[n-2] \quad (39)$$

The self-dithering property of the second-order $\Delta\Sigma$ modulator ideally causes $e_q[n]$ to have a power spectral density equivalent to that of zero-mean white noise [2], [3], [5], [12].

It follows from (62) in the Appendix and (31) that $\hat{e}_q[n] = e_{yq}[n]$ when the clipping accumulator does not clip. Thus, (33) implies that

$$-\hat{e}_q[n] = -e_q[n] + 2^J e_{Rq}[n] \quad (40)$$

As shown in the Appendix the values taken on by $e_{yq}[n]$ are multiples of $2^{J-1}/K$, so the same must be true of $\hat{e}_q[n]$. Equation (22) implies that $-2^{J-1}/K < 2^J e_{Rq}[n] \leq 0$, so for each n there is exactly one value of $2^J e_{Rq}[n]$ that causes $-e_q[n] + 2^J e_{Rq}[n]$ to be a multiple of $2^{J-1}/K$. It follows that $\hat{e}_q[n]$ must have the form

$$-\hat{e}_q[n] = -\frac{2^{J-1}}{K}\left\lfloor \frac{K}{2^{J-1}} e_q[n] \right\rfloor \tag{41}$$

which represents quantization of $-e_q[n]$ to the nearest multiple of $2^{J-1}/K$ that is less than or equal to $-e_q[n]$. This is the operation performed by the fractional part quantizer shown in Fig. 1(b).

C. Average PFD Pulse-Width

If the $\Delta\Sigma$ FDC is locked for all $t \geq 0$, it follows from (28) that the output of the clipping accumulator can be written as

$$r[n] = r[0] + 2^J e_{Rq}[n] - 2^J e_{Rq}[0] + \sum_{k=1}^{n} \left((\tau_k - t_k - T_{\bar{u}}) f_{PLL} + 2^J \psi_{DMRO}[k] \right) \tag{42}$$

and as shown above $r[n]$ is bounded for all $n \geq 1$. The first three terms in (42) are bounded by definition, so this implies that the summation in (42) must be bounded too for all $n \geq 1$. This is only possible if the average of the summed terms is zero, so it implies

$$\lim_{n\to\infty} \frac{1}{n} \sum_{k=1}^{n} (\tau_k - t_k) = T_{\bar{u}} - \frac{2^J}{f_{PLL}} \left(\lim_{n\to\infty} \frac{1}{n} \sum_{k=1}^{n} \psi_{DMRO}[k] \right) \tag{43}$$

By definition, the left side of (43) is the average pulse width of the PFD output, $u(t)$, when the $\Delta\Sigma$ FDC is locked, and the right side is $T_{\bar{u}}$ minus a scaled version of the average DMRO frequency error. Therefore, the average pulse width of $u(t)$ is approximately $T_{\bar{u}}$, and if the average DMRO frequency error is zero, it is exactly $T_{\bar{u}}$. This result is used in Section III-E in the explanation of why the DMRO need not have instantaneous frequency transitions.

D. Average DMRO Frequency

As described above, if the $\Delta\Sigma$ FDC is locked for all $t \geq 0$, then the clipping accumulator does not clip, so the operations shown in Fig. 2(b) imply that

$$r[n] = r[n-1] + 2^J \left(f_R[n] - M \right) \tag{44}$$

An implication of $r[n]$ being bounded is that the average frequency of the DMRO is Mf_{ref}. This follows because (44) can only be bounded if the average of $f_R[n]$ is M. As described above, $f_R[n]$ represents the phase change in cycles over the nth clk_{FDC} period (which has a duration of a reference period), so the DMRO must have an average frequency of Mf_{ref}.

Given that $r[n]$ is an accumulated version of $f_R[n] - M$, it can be interpreted as a quantized measurement of the difference between the phase of the DMRO and the phase of an ideal oscillator of frequency Mf_{ref} sampled at the time of the nth rising edge of clk_{FDC}. As $y[n]$ is the integer part of $r[n]$, it can be interpreted as a measure of this phase difference rounded down to the nearest integer.

E. Effects of non-Ideal Circuit Behavior

Typically, in frequency synthesizer applications the most troublesome non-ideal fractional-N PLL behavior is the generation of fractional spurious tones in the PLL's output. This sub-section describes the types of non-ideal circuit behavior within the FDC-PLL that can cause fractional spurious tones.

All fractional-N PLLs perform quantization, which is a highly nonlinear operation, so this is a potential source of fractional spurious tones. In both analog PLLs and second-order FDC-PLLs, the self-dithering property of higher-than-first-order, multi-bit $\Delta\Sigma$ modulation ideally suppresses spurious tones [2], [3], [5], [12].

Of course, non-ideal circuit behavior can degrade the $\Delta\Sigma$ FDC's equivalence to a second-order $\Delta\Sigma$ modulator, which can degrade the self-dithering property. As can be verified from the equivalence proof in Section III-B, the first accumulator in the equivalent $\Delta\Sigma$ modulator shown in Fig. 1(b) derives from the frequency-to-phase integrating behavior of the multi-modulus divider, and both $\Delta\Sigma$ modulator feedback loops derive from the $\Delta\Sigma$ FDC's $2 - z^{-1}$ local feedback. As the divider and $2 - z^{-1}$ block are digital, the first accumulator and both feedback paths are inherently ideal.

The second accumulator in the equivalent $\Delta\Sigma$ modulator derives from the frequency-to-phase integrating behavior of the DMRO implied by (10). The DMRO is not an all-digital structure, so it is not inherently ideal. However, the FDC-PLL is fairly insensitive to non-ideal DMRO behavior in much the same way that analog PLLs are fairly insensitive to non-ideal charge pump behavior. It is well known that non-ideal charge pump switching transients do not cause fractional spurious tones in an analog PLL provided each current source has time to settle whenever it is turned on or off, and provided the rising and falling transient shapes are independent of the times at which the current source is turned on and off, respectively [13]. For the same reasons, non-ideal DMRO frequency switching transients do not cause fractional spurious tones in the FDC-PLL provided the high and low durations of $u(t)$ each reference period are long enough for the transients to settle out, and the rising and falling transient shapes are independent of the times at which $u(t)$ goes high and low, respectively.

As shown in the Appendix $-1 < e_q[n] \leq 0$ when the $\Delta\Sigma$ FDC is locked, so it follows from (14) and (32) that the minimum and maximum high durations of $u(t)$ each reference period are $T_{\bar{u}} - 4/f_{PLL}$ and $T_{\bar{u}} + 4/f_{PLL}$, respectively, when the $\Delta\Sigma$ FDC is locked. Thus, provided the DMRO's frequency switching transients settle out within $1/2T_{ref} - 4/f_{PLL}$, $T_{\bar{u}}$ can be set to ensure that the DMRO has sufficient time to settle each time it changes frequency. Furthermore, the faster the DMRO transients settle out, the larger the acceptable range of values of $T_{\bar{u}}$ and, therefore, f_{low}.

In practical DMROs each switching transient does depend somewhat on when in the DMRO's cycle the corresponding transition of $u(t)$ occurs. However, simulation and experimental results indicate that DMROs can be designed for which this effect does not significantly degrade the FDC-PLL's performance [4]. Specifically, transistor-level simulations indicate that the phase of the DMRO presented in [4] deviates from its ideal linear phase behavior by at most $\pm 0.35\%$ per reference period. Behavioral-level simulations further predict that such error results in fractional spurious tones with powers that are below -70 dBc in band and that drop quickly as the fractional frequency is increased out of band.

Another source of non-ideal error is that f_{high} and f_{low} will not differ by exactly $2^{-J} f_{PLL}$ as specified by (4). It can be

verified by a slight extension of the analysis presented in Section III-B that a percentage error in this difference causes the same percentage error to occur in the gain of the equivalent $\Delta\Sigma$ modulator's second accumulator. It is well known that the quantization noise and signal transfer functions of a second-order $\Delta\Sigma$ modulator are not highly sensitive to deviations in the gain of its second accumulator [5]. It follows that the FDC-PLL is not highly sensitive to deviations of $f_{high} - f_{low}$ from its ideal value of $2^{-J} f_{PLL}$. Simulation results that support this claim are presented in Section V.

Another type of DMRO-related non-ideal behavior is coupling of the DMRO oscillation waveforms into other parts of the PLL. However, as proven in Section III-D, the average DMRO frequency is a fixed integer multiple of f_{ref}, which greatly reduces the potential of the DMRO to introduce fractional spurious tones. If the average DMRO frequency were not a multiple of the reference frequency (as in PLLs based on SRO-TDCs as described in Section III-F), its fundamental and harmonics would have fractional relationships to those of the FDC-PLL output. In this case, parasitic coupling of the DMRO output lines into the DCO or reference circuitry would cause fractional spurious tones.

The results described above are supported by the experimental results presented in [4]. The FDC-PLL presented in [4] has a worst case measured in-band fractional spurious tone power of -60 dBc, and, as expected, the worst-case measured fractional spurious tone power drops quickly as the fractional frequency is increased outside of the loop bandwidth. This is the best spurious tone performance reported to date for a digital PLL. Compared to other digital PLLs with similarly low phase noise, the FDC-PLL achieves an order of magnitude lower spurious tone power than previously reported in the literature.

F. Comparison to GRO-TDC and SRO-TDC Based PLLs

This subsection compares the FDC-PLL presented above to prior digital PLLs based on gated ring oscillator (GRO) time-to-digital converters (TDCs) and switched ring oscillator (SRO) TDCs [14]–[17].[2] In each such PLL, the TDC consists of a DMRO, i.e., either a GRO or SRO, followed by a digital $1-z^{-1}$ block, so it is equivalent to a ring oscillator based first-order $\Delta\Sigma$ ADC [18].

These TDC based PLLs each have a frequency control mechanism similar to that of an analog PLL in that the divider modulus is controlled by a digital $\Delta\Sigma$ modulator such that its average modulus is $N + \alpha$. However, it differs from an analog PLL in that a TDC, a digital loop filter, and a DCO are used in place of a charge pump, analog loop filter, and voltage controlled oscillator.

The TDC does the equivalent of integrating and dumping the top PFD output pulse each reference period and quantizing the result. Its $1 - z^{-1}$ block simultaneously neutralizes the integration performed by the DMRO and imposes first-order highpass spectral shaping on the quantization error. Thus, the output of the TDC is a quantized measure of the DMRO's frequency.

[2]A GRO is the special case of a DMRO with $f_{low} = 0$. Initially, the SRO was presented as a generalization of the GRO to allow for $f_{low} \geq 0$ [16], but it has since been used in the literature to denote a block that is distinct from a GRO (i.e., a DMRO with $f_{low} \neq 0$) [17]. As the results of this paper hold regardless of whether the FDC-PLL incorporates a GRO or an SRO, the term DMRO has been used to avoid potential confusion.

The TDC's DMRO is switched between two frequencies as in the $\Delta\Sigma$ FDC, but its sampled phase does not control the divider modulus. Instead, it is subjected to a $1 - z^{-1}$ transfer function, the result of which is passed directly to the PLL's loop filter.

In contrast, in the $\Delta\Sigma$ FDC the DMRO's sampled phase controls the divider modulus such that the $\Delta\Sigma$ FDC output is equivalent to second-order $\Delta\Sigma$ modulation of the PLL's frequency error minus α. The $\Delta\Sigma$ FDC's quantization noise shaping is not the result of an explicit $1 - z^{-1}$ transfer function as in the TDCs described above, but rather the result of the two integrations performed within the $\Delta\Sigma$ FDC's local feedback as described in Section III-E. Digital circuitry following the $\Delta\Sigma$ FDC subtracts α, and accumulates the result, so, as in the TDC based PLLs described above, the input to the loop filter is a measure of the PLL's phase error plus first-order shaped quantization noise. However, unlike TDC based PLLs, the $\Delta\Sigma$ FDC inherits the self-dithering property of second-order $\Delta\Sigma$ modulation and its benefits with respect to spurious tone suppression as described in Section III-E.

Furthermore, as described above, the $y[n]$ output of the $\Delta\Sigma$ FDC is the quantized difference between the phase of the DMRO and that of an ideal oscillator of frequency Mf_{ref}. The local feedback within the $\Delta\Sigma$ FDC keeps $y[n]$ bounded, which causes the average frequency of the DMRO in the $\Delta\Sigma$ FDC to lock to Mf_{ref} as described in Section III-D. In contrast, in the TDC based PLLs described above the TDC output is a quantized measure of the DMRO's frequency, so the GRO or SRO generally has a fractional relationship to f_{ref}.

G. Comparison to Other FDC-PLLs

This subsection compares the FDC-PLL presented above to previously published FDC-PLLs. These prior FDC-PLLs are based on either first-order $\Delta\Sigma$ FDCs [19]–[22] or second-order $\Delta\Sigma$ FDCs [1]–[3].

A first-order $\Delta\Sigma$ FDC uses the phase integrating behavior of its divider without any additional integration to achieve first-order quantization noise shaping, so its output sequence is given by (1) but with $e_{\Delta\Sigma}[n] = e_q[n] - e_q[n-1]$. It can be used in place of the second-order $\Delta\Sigma$ FDC shown in Fig. 1(a) without the QNC path to implement a first-order FDC-PLL. While first-order $\Delta\Sigma$ FDCs have the advantage of simplicity, their quantization noise is identical to that of a first-order $\Delta\Sigma$ modulator so it tends to have large spurious tones even in the absence of non-ideal circuit behavior [5].

The prior second-order $\Delta\Sigma$ FDCs use a charge pump and ADC instead of a DMRO and digital logic to implement the equivalent $\Delta\Sigma$ modulator's second integrator and quantizer. Although the block diagram of such a $\Delta\Sigma$ FDC appears less complicated than that of the DMRO based FDC-PLL shown in Fig. 2, the authors have found the latter to be more area-efficient in CMOS technology at or below the 65 nm node because of its highly-digital structure. It also tends to work significantly better at low supply voltages and in the presence of high device leakage, because it is difficult to design a good charge pump integrator under such conditions.

However, the charge pump and ADC based $\Delta\Sigma$ FDC has an advantage in IC technology with low device leakage. This is because the charge pump is only on, and, hence, only injects noise, for a small portion of each reference period. In contrast, unless a GRO-version of the DMRO is used, the DMRO injects noise continuously. In particular, the $1/f^3$ noise it injects can

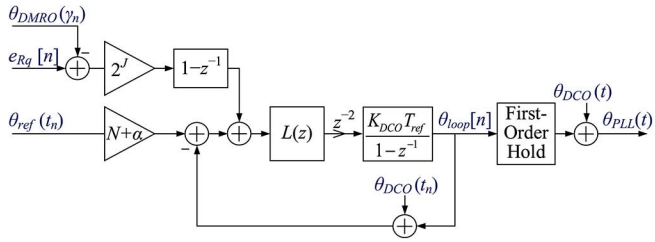

Fig. 4. Linearized model of the FDC-PLL.

be problematic, because, as predicted by the linearized model shown in Fig. 4, this noise shows up as a $1/f$ noise component of the PLL's phase noise. In principle, a GRO-version of the DMRO would avoid this problem. Unfortunately, a GRO would likely have greater frequency-transient time-dependence than an SRO [17], and, as explained in Section III-E, this can cause spurious tones in the PLL's phase noise.

IV. FDC-PLL Linearized Model

Like many PLLs, the FDC-PLL's output phase noise, $\theta_{PLL}(t)$, has a nearly linear and time-invariant dependence on the noise waveforms introduced by its components. Hence, it is useful to model the FDC-PLL as a linear time-invariant system to provide a tractable means of analyzing its phase noise performance and loop dynamics. Such a model is necessary for the system-level design of the PLL. The results derived in Section III allow the linearized model of the FDC-PLL presented in [2] to be extended to the FDC-PLL presented in this paper with only minor modifications.

The modifications are required to include the effect of DMRO phase noise instead of charge pump noise, and to include the effect of QNC. Equations (13), (38), and (39) imply that the contribution of DMRO phase noise to the $\Delta\Sigma$ FDC's $y[n]$ output is

$$-2^J\left(\theta_{DMRO}(\gamma_n) - 2\theta_{DMRO}(\gamma_{n-1}) + \theta_{DMRO}(\gamma_{n-2})\right) \tag{45}$$

Therefore, the $\Delta\Sigma$ FDC applies the same $(1-z^{-1})^2$ transfer function to $-2^J\theta_{DMRO}(\gamma_n)$ as it applies to the quantization noise, $e_q[n]$. Equation (39) and the operations shown in Fig. 1(a) imply that the input to the digital loop filter can be written as

$$-e_{PLL}[n] + e_q[n] - e_q[n-1] - \hat{e}_q[n] + \hat{e}_q[n-1] \tag{46}$$

With (40) this can be written as

$$-e_{PLL}[n] + 2^J e_{Rq}[n] - 2^J e_{Rq}[n-1] \tag{47}$$

Therefore, QNC effectively replaces $e_q[n]$ with $2^J e_{Rq}[n]$ at the input of the digital loop filter. Applying these results to the linearized model presented in [2] gives the modified linearized model shown in Fig. 4. The model parameters not defined previously are $\theta_{DCO}(t)$, $L(z)$, and K_{DCO}, which are the phase error waveform of the DCO, the digital loop filter's transfer function, and the DCO gain, respectively.[3]

The linearized model does not contain noise sources corresponding to the divider, PFD, or the counter and ring sampler registers in the ring phase calculator. If necessary, these noise sources can be included in the model, but typically they are not significant in practice. The divider output usually is resynchronized to a DCO edge, thereby negating most of its noise. PFD noise tends to be negligible relative to the PLL's other noise sources. The jitter introduced by the counter and ring sampler registers in the ring phase calculator are subjected to the same transfer function as $\theta_{DMRO}(\gamma_n)$, but tend to have much lower power and relatively flat spectra, so their contribution to the FDC-PLL's phase noise usually is not significant.

Although periodic steady state (PSS) circuit simulations can be used to quickly estimate the power spectral density (PSD) functions of the various noise sources within the FDC-PLL, existing PSS circuit simulations tools are not applicable to the FDC-PLL as a whole because of the non-periodic nature of the $\Delta\Sigma$ FDC. An expression for the FDC-PLL's phase noise PSD in terms of the PSD functions of its noise sources is derived below to address this issue.

It is assumed that $e_{Rq}[n]$, $\theta_{ref}(t_n)$, $\theta_{DMRO}(\gamma_n)$, and $\theta_{DCO}(t)$ can be modeled as uncorrelated, wide-sense stationary random processes and that $\theta_{ref}(t_n)$, $\theta_{DMRO}(\gamma_n)$, and $\theta_{DCO}(t)$ have zero mean. It follows that the two-sided PSD of $\theta_{PLL}(t)$ is the sum of two-sided PSD components that each correspond to one of the noise signals, i.e., the two-sided PSD of $\theta_{PLL}(t)$ has the form

$$\begin{aligned} S_{\theta_{PLL}}(f) = {} & S_{\theta_{PLL}}(f)|_{e_{Rq}} + S_{\theta_{PLL}}(f)|_{DMRO} \\ & + S_{\theta_{PLL}}(f)|_{ref} + S_{\theta_{PLL}}(f)|_{DCO} \end{aligned} \tag{48}$$

where the four terms from left to right on the right side of (48) are the components of the two-sided PSD of $\theta_{PLL}(t)$ corresponding to $e_{Rq}[n]$, $\theta_{DMRO}(\gamma_n)$, $\theta_{ref}(t_n)$, and $\theta_{DCO}(t)$, respectively.

Reasoning similar to that presented in [2] can be applied to the linearized model shown in Fig. 4 to obtain the following expressions for these components

$$S_{\theta_{PLL}}(f)|_{e_{Rq}} = \frac{2^{-2(F-J)}T_{ref}}{3}\sin^2(\pi T_{ref}f)\,|G(f)|^2 \tag{49}$$

$$\begin{aligned} S_{\theta_{PLL}}(f)|_{DMRO} = {} & 2^{2J+2}\sin^2(\pi T_{ref}f)\,|G(f)|^2 \\ & T_{ref}S_{\theta_{DMRO}}\left(e^{j2\pi T_{ref}f}\right) \end{aligned} \tag{50}$$

$$S_{\theta_{PLL}}(f)|_{ref} = (N+\alpha)^2\,|G(f)|^2\,S_{\theta_{ref}}(f) \tag{51}$$

and

$$S_{\theta_{PLL}}(f)|_{DCO} = |1-G(f)|^2\,S_{\theta_{DCO}}(f) \tag{52}$$

where $S_{\theta_{ref}}(f)$ and $S_{\theta_{DCO}}(f)$ are the two-sided phase noise PSDs in cycles squared per Hz of the reference and DCO, respectively, $S_{\theta_{DMRO}}(e^{j2\pi T_{ref}f})$ is the two-sided discrete-time PSD of $\theta_{DMRO}(\gamma_n)$ in cycles squared,

$$G(f) = \frac{T\left(e^{j2\pi T_{ref}f}\right)}{1+T\left(e^{j2\pi T_{ref}f}\right)}\left[\frac{\sin(\pi T_{ref}f)}{\pi T_{ref}f}\right]^2 \tag{53}$$

and

$$T(z) = K_{DCO}T_{ref}L(z)\frac{z^{-2}}{1-z^{-1}} \tag{54}$$

is the discrete-time loop gain of the FDC-PLL.

Standard PSS circuit simulations can be used to estimate the phase noise PSDs of the reference and DCO in (51) and (52), but estimating the phase noise PSD of the DMRO in (50) is less straightforward. This is because the FDC-PLL changes the frequency of the DMRO each reference period, which is not handled well by existing PSS simulation tools. In the next section this issue is addressed by upper bounding

[3]The *DCO Gain* is defined as the amount in Hz by which the DCO frequency changes when the DCO input changes by unity.

$T_{ref}S_{\theta_{DMRO}}(e^{j2\pi T_{ref}f})$ as the maximum of two simulated phase noise PSDs, each corresponding to the DMRO running continuously at one of its two frequencies. This results in an upper bound for the contribution of the DMRO to the FDC-PLL's phase noise.

All phase noise waveforms are in units of cycles, so $S_{\theta_{PLL}}(f)$ has units of cycles squared per Hz. It follows from the definition of dBc/Hz presented in [23] and [24] that the FDC-PLL's output phase noise PSD in dBc/Hz is

$$10\log\left[4\pi^2 S_{\theta_{PLL}}(f)\right] \tag{55}$$

for $f \geq 0$.

The first factor in the expression for $G(f)$ is the lowpass filter transfer function of the linearized model's discrete-time loop, and the second factor is the lowpass filtering effect of the first-order hold. Both terms are unity at $f = 0$, so $G(f)$ has a lowpass shape and $1 - G(f)$ has a highpass shape. The $\sin^2(\pi T_{ref}f)$ term in (49) and (50) attenuates spectral power within the pass-band of $G(f)$. Therefore, the behavior implied by (49), (51), and (52) is similar to that of a second-order $\Delta\Sigma$ modulator based analog PLL with QNC [7].

Typically, the phase noise of a ring oscillator consists of $1/f^2$ and $1/f^3$ components within the PLL bandwidth. The $\sin^2(\pi T_{ref}f)$ term in (50) imposes a $(\pi T_{ref}f)^2$ transfer function term within the PLL bandwidth, so the $1/f^2$ and $1/f^3$ components of the DMRO phase noise contribute flat and $1/f$ noise components, respectively, to the FDC-PLL's output phase noise PSD.

V. Design Example

Table I shows relevant parameters used to create a system-level simulation of an FDC-PLL targeted for 65 nm CMOS implementation. The reference source is a high-quality crystal oscillator with a flat phase noise floor of -155 dBc/Hz beyond a few kHz offset. The DCO is an LC-based core with power-of-two-weighted coarse and unit-weighted fine capacitor banks, the latter of which consists of the high-Q frequency control elements (FCEs) introduced in [3].

Each FCE has a nominal frequency step of 25 kHz. The output of the digital loop filter is a fixed point sequence with an update rate of f_{ref}. Its integer portion drives FCEs directly, and its fractional portion drives FCEs through a second-order digital $\Delta\Sigma$ modulator clocked at an eighth of the DCO frequency [25]. This achieves an effective DCO step-size of approximately 100 Hz.

The DMRO is a 16-stage pseudo-differential version of the ring oscillator presented in [4] with $f_{high} = 4.7$ GHz and $f_{low} = 1.2$ GHz. It uses the multi-path technique proposed in [26], which, as demonstrated in [4] enables operation at these frequencies in 65 nm CMOS technology. The DMRO frequency is controlled via current-starving switches. Simulations show that the DMRO's phase noise is relatively independent of whether the DMRO frequency is set to f_{high} or f_{low}, but as explained in Section IV, the worse of the two phase noise spectra is used for system simulation to err on the side of pessimism.

The 16 pseudo-differential stages of the DMRO divide each DMRO period into 32 phases, so $F = 5$ in Fig. 2(b). The choice of $f_{high} - f_{low} = f_{pll}$ satisfies (4) with $J = 0$. Thus, $\hat{e}_q[n]$ has 5 bits of resolution, so the FDC-PLL's suppression of quantization noise via QNC is approximately 30 dB.

TABLE I
Design Parameters and Evaluation Settings

Design Parameters		Value
Reference Source	Frequency, f_{ref}	26 MHz
	White phase noise	−155 dBc/Hz
DCO	DCO gain, K_{DCO}	25 kHz
	Phase noise at 1 MHz	−129 dBc/Hz
	1/f noise corner	100 kHz
DMRO	Number of stages, K	16
	Low frequency, f_{low}	1.2 GHz
	High frequency, f_{high}	4.7 GHz
	Phase noise at 10 MHz	−125 dBc/Hz
	1/f noise corner	1 MHz
ΔΣ FDC Parameters	Reference edge to clk_{FDC} delay	19.2 ns
	Counter bits, C	8
	Fixed count, M	80
	Fractional phase bits, F	5
	Frequency scale factor, J	0
Loop Dynamics	Loop gain multiplier, K_M	1.25
	Proportional gain, K_P	2^5
	Integral gain, K_I	2^{-4}
	IIR poles, λ_0, λ_1	2^{-3}, 2^{-1}
PLL Settings	Output frequency, f_{PLL}	3.484 GHz
	Integer multiplier, N	134
	Fractional multiplier, α	0.0003846153
	Loop bandwidth	140 kHz
	Phase margin	70 degrees

With the above choices of f_{high} and f_{ref}, (7) implies that an 8 bit counter in the ring phase calculator is sufficient. The reference period is 38.4 ns, so the DMRO is sampled 19.2 ns after each rising edge of the reference signal. The value of M was chosen in conjunction with f_{low} via (5) to ensure that the average $u(t)$ up-duration, $T_{\bar{u}}$, is a quarter of the reference period. This allows 9.6 ns of DMRO settling time after each rising and falling edge of $u(t)$.

The digital loop filter consists of two single-pole IIR stages and a proportional-integral (PI) stage. Its transfer function is

$$L(z) = K_M \cdot \frac{K_P + (K_I - K_P)z^{-1}}{1 - z^{-1}} \cdot \prod_{i=0}^{1} \frac{\lambda_i}{1 - (1 - \lambda_i)z^{-1}} \tag{56}$$

For this example, the 140 kHz bandwidth was chosen as it allows the $\Delta\Sigma$ FDC quantization noise to be just large enough that it begins to influence overall phase noise at 1–10 MHz offsets.

The FDC-PLL was simulated with an event-driven behavioral simulator written in C. The simulator generates events for the reference clock edges, DCO edges, and DMRO edges. At each event it uses the current state of the PLL including all the noise sources to update the occurrences of future events, and then advances the simulator time to the next event. The phase noise composite plot of Fig. 5 was generated by selectively enabling the various FDC-PLL noise sources. As expected, the reference phase noise, quantization noise and DMRO phase noise have similar characteristic roll-offs outside the PLL bandwidth because of the $G(f)$ term in (49), (50), and (51). The $\Delta\Sigma$ FDC quantization noise is suppressed at a rate of 20 dB/decade toward low frequencies, as a result of the second-order highpass-shaped frequency noise being converted to first-order highpass-shaped phase noise by the loop, in accordance with (49). Also visible is the rising 10 dB/dec phase noise contribution from the

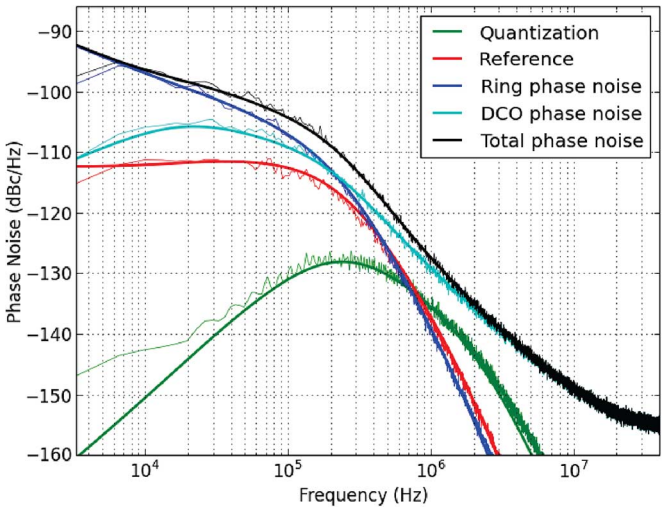

Fig. 5. Simulated and calculated FDC-PLL phase noise PSD contributions from individual noise sources (heavy lines represent calculated results).

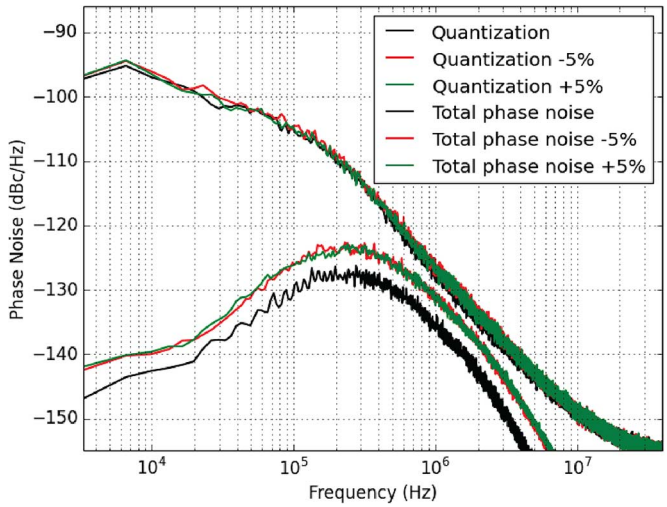

Fig. 6. Simulated FDC-PLL phase noise PSD functions with 5% variation in f_{high} and f_{low}.

$1/f^3$ region of DMRO's phase noise, which, in this case, dominates the total in-band phase noise.

Fig. 6 shows simulated FDC-PLL phase noise PSD functions for f_{high} de-tuned such that $f_{high} - f_{low}$ deviates by $\pm 5\%$ from its ideal value of f_{pll}, to support the claim in Section III-E that the FDC-PLL has low sensitivity to deviations from the ideal DMRO frequencies. As indicated in Fig. 6, the phase noise PSD functions corresponding to $\pm 5\%$ $f_{high} - f_{low}$ errors are nearly indistinguishable from the ideal PSD functions, and no significant spurious tones are visible (the simulated fractional frequency is 10 kHz, so non-ideal behavior would be expected to induce spurious tones at multiples of 10 kHz relative to f_{pll}).

APPENDIX

A. Clipping Accumulator Output Quantizer Behavior

The clipping accumulator's input, and, hence, its output are two's complement fixed point sequences with $F - J$ fractional bits. The clipping operations of (8) are such that the integer part of its output is a 3-bit two's complement sequence restricted to the set $\{-2, -1, 0, 1, 2\}$. Therefore, $r[n]$ is a $3 + F - J -$ bit two's complement sequence with values given by

$$r[n] = -4r_{2+F-J}[n] + \sum_{k=0}^{1+F-J} 2^{-(F-J-k)} r_k[n] \tag{57}$$

where $r_k[n]$ for $k = 0, 1, \ldots, 2 + F - J$ are the bits that make up $r[n]$ ordered from LSB to MSB. As indicated in Fig. 3, $y[n]$ is taken to be the three MSBs of $r[n]$. It is interpreted as an integer-valued two's complement sequence, so it can be written as

$$y[n] = -4r_{2+F-J}[n] + 2r_{1+F-J}[n] + r_{F-J}[n] \tag{58}$$

Given that $y[n]$ is the integer part of $r[n]$, (8) implies that it can be expressed as

$$y[n] = \begin{cases} \lfloor a[n] \rfloor, & \text{if } -2 \le a[n] < 3 \\ 2, & \text{if } a[n] \ge 3 \\ -2, & \text{if } a[n] < -2 \end{cases} \tag{59}$$

where $a[n] = r[n-1] + d_R[n]$

As indicated in Fig. 3, the bottom output of the ring phase calculator is taken to be the fractional bits of $r[n]$ with a zero-valued MSB appended. It is interpreted as an $F - J + 1 -$ bit two's complement sequence so it can be written as

$$-\hat{e}_q[n] = \sum_{k=0}^{F-J-1} 2^{-(F-J-k)} r_k[n] \tag{60}$$

It follows from (57), (58), and (60) that

$$y[n] = r[n] + \hat{e}_q[n] \tag{61}$$

so (8) and (59) imply that

$$-\hat{e}_q[n] = \begin{cases} a[n] - \lfloor a[n] \rfloor, & \text{if } -2 \le a[n] < 3 \\ 1 - 2^{J-1}/K, & \text{if } a[n] \ge 3 \\ 0, & \text{if } a[n] < -2 \end{cases} \tag{62}$$

This implies that $\hat{e}_q[n]$ can be interpreted as the quantization error introduced by rounding $r[n]$ down to the nearest integer less than or equal to $r[n]$.

B. $\Delta\Sigma$ FDC Locking Conditions

The derivation of (32) in Section III-B is valid for any sample time n provided both (25) is satisfied and the clipping accumulator does not clip at sample times $n-1$ and $n-2$. Let k be any integer greater than 1 and suppose that at times $n = k-1$ and $n = k-2$ (25) is satisfied and the clipping accumulator does not clip. Therefore, (32) implies that

$$\begin{aligned} &(\tau_k - t_k) f_{PLL} \\ &\quad = T_{\bar{u}} f_{PLL} - y[k-1] - e_q[k-1] + e_q[k-2] \\ &\qquad -2^J \psi_{DMRO}[k-1] - \psi_{PLL}[k] + (N+\alpha)\psi_{ref}[k] - \alpha \end{aligned} \tag{63}$$

where for $n = k-1$ and $n = k-2$

$$e_q[n] = 2^J e_{Rq}[n] + e_{yq}[n], \tag{64}$$

$e_{yq}[n]$ is given by (31), and $e_{Rq}[n]$ is given by (22).

By design, the values taken on by $f_R[n]$ are multiples of $1/(2K)$, so the operations indicated by (8) and (9) imply that the values taken on by $a[n]$ are multiples of $2^{J-1}/K$. Also by design, $2^{1-J}K$ is integer-valued, so every integer is a multiple of $2^{J-1}/K$. Therefore, (31) implies that $e_{yq}[n]$ is a multiple of $2^{J-1}/K$ and that

$$-1 + \frac{2^{J-1}}{K} \le e_{yq}[n] \le 0 \tag{65}$$

for $n = k-1$ and $n = k-2$. Equation (22) implies that

$$-\frac{2^{J-1}}{K} < 2^J e_{Rq}[n] \leq 0 \tag{66}$$

for all sample times n, so it follows from (64) and (65) that

$$-1 < e_q[n] \leq 0 \tag{67}$$

for $n = k-1$ and $n = k-2$.

By definition, $t_n - \gamma_{n-1} \cong 1/2T_{ref}$ for all n (assuming a reference signal duty cycle of 50%), so to satisfy (25) at time $n = k$, it is necessary that

$$0 < \tau_k - t_k < \frac{T_{ref}}{2} \tag{68}$$

It follows from (14), (63), and (67) that

$$T_{\bar{u}} - \frac{4}{f_{PLL}} < \tau_k - t_k < T_{\bar{u}} + \frac{4}{f_{PLL}} \tag{69}$$

Given that $f_{PLL} = (N+\alpha)/T_{ref}$ and $T_{\bar{u}}$ is in the range given by (6), it follows from (69) that (68) and, therefore, (25) are satisfied at time $n = k$.

This result and the starting assumption that (25) is satisfied and the clipping accumulator does not clip at times $n = k-1$ and $n = k-2$ are sufficient conditions for the derivation of (34) and (35) in Section III-B to be valid at sample time $n = k$. Therefore,

$$a[k] = s[k] + 2^J e_{Rq}[k] \tag{70}$$

where

$$\begin{aligned} s[k] = & -2e_q[k-1] + e_q[k-2] \\ & - \psi_{PLL}[k] + (N+\alpha)\psi_{ref}[k] - \alpha \\ & + 2^J \left(\psi_{DMRO}[k] - \psi_{DMRO}[k-1]\right) \end{aligned} \tag{71}$$

This with (14) and (67) imply that $-2 < s[k] < 3$. As shown above, the values taken on by $a[k]$ are multiples of $2^{J-1}/K$ as are the set of integers. Therefore, if $-2 < s[k] < -2+2^{J-1}/K$, it follows that $a[k] = -2$ because this is the only multiple of $2^{J-1}/K$ that (70) can attain given (65). If $s[k] > -2+2^{J-1}/K$, (66) and (70) imply that $r[k] > -2$. Furthermore, $r[k] < 3$, because $2^J e_{Rq}[n] \leq 0$ and $s[k] < 3$.

The above analysis proves that $-2 \leq a[k] < 3$, so clipping does not occur at sample time $n = k$. It also shows that (25) is satisfied at time $n = k$, and that is (67) satisfied at time $n = k-1$. As k was an arbitrary time index greater than 1, it follows by induction that the clipping accumulator does not clip and that both (25) and (67) are satisfied for all sample times $n \geq k-2$.

On the basis of the above analysis, the $\Delta\Sigma$ FDC is defined to be locked at sample time n provided both (25) is satisfied and the clipping accumulator does not clip at sample times $n-1$ and $n-2$. The above analysis shows that once it is locked, it will stay locked for all future sample times provided (14) holds for all future sample times.

REFERENCES

[1] W. T. Bax and M. A. Copeland, "A GMSK modulator using a $\Delta\Sigma$ frequency discriminator-based synthesizer," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1218–1227, Aug. 2001.

[2] C. Venerus and I. Galton, "Delta-sigma FDC based fractional-N PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1274–1285, May 2013.

[3] C. Venerus and I. Galton, "A TDC-free mostly-digital FDC-PLL frequency synthesizer with a 2.8–3.5 GHz DCO," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 450–463, Feb. 2015.

[4] C. Weltin-Wu, G. Zhao, and I. Galton, "A highly-digital frequency synthesizer using ring oscillator frequency-to-digital conversion and noise cancellation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2015.

[5] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2005.

[6] C. Venerus, "Delta-sigma FDC based fractional-N PLLs with multirate quantizing dynamic element matching," Ph.D. dissertation, Univ. California, San Diego, CA, USA, 2013.

[7] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1-Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

[8] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700 kHz bandwidth $\Delta\Sigma$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.

[9] S. E. Meninger and M. H. Perrott, "A 1 MHz bandwidth 3.6 GHz 0.18 um CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 966–980, Apr. 2006.

[10] A. Swaminathan, K. Wang, and I. Galton, "A wide-bandwidth 2.4GHz ISM-band fractional-N PLL with adaptive phase-noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec. 2007.

[11] H. Hedayati, B. Bakkaloglu, and W. Khalil, "A 1 MHz-bandwidth type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2009, pp. 389–390.

[12] I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inf. Theory*, vol. 40, no. 3, pp. 848–859, May 1994.

[13] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York: McGraw-Hill, 2001, pp. 562–566.

[14] C. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise, wide-BW 3.6 GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.

[15] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009.

[16] A. Elshazly, B. Young, S. Rao, and P. K. Hanumolu, "A 13 b 315fsrms 2 mW 500 MS/s 1 MHz bandwidth highly digital time-to-digital converter using switched ring oscillators," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 464–465.

[17] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators—analysis, design, measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.

[18] M. Hoven, A. Olsen, T. S. Lande, and C. Toumazou, "Delta-sigma modulators using frequency-modulated intermediate values," *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 13–22, Jan. 1997.

[19] M. A. Ferriss and M. P. Flynn, "A 14 mW fractional-N PLL modulator with a digital phase detector and frequency switching scheme," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2464–2471, Nov. 2008.

[20] W. Khalil, S. Shashidharan, T. Copani, S. Chakraborty, S. Kiaei, and B. Bakkaloglu, "A 700- μA 405-MHz all-digital fractional-N frequency-locked loop for ISM band applications," *IEEE Microw. Theory Tech.*, vol. 59, no. 5, pp. 1319–1326, May 2011.

[21] L. Li, M. P. Flynn, and M. A. Ferriss, "A 5.8 GHz digital arbitrary phase-setting type II PLL in 65 nm CMOS with 2.25o resolution," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2012, pp. 317–320.

[22] M. Talegaonkar, T. Anand, A. Elkholy, A. Elshazly, R. K. Nandwana, S. Saxena, B. Young, W. Choi, and P. K. Hanumolu, "A 4.4–5.4 GHz digital fractional-N PLL using $\Delta\Sigma$ frequency-to-digital converter," in *Proc. Symp. VLSI Circuits*, Jun. 2014.

[23] *IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology-Random Instabilities*, IEEE Standard 1139–2008.

[24] Phase Noise Guide: Agilent Technologies PSA Series Spectrum Analyzers Option 226, Part Number: E4440–90328.

[25] R.-B. Staszewski *et al.*, "Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 815–828, Nov. 2003.

[26] S.-J. Lee, B. Kim, and K. Lee, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 289–291, Feb. 1997.

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