A TDC-Free Mostly-Digital FDC-PLL Frequency Synthesizer With a 2.8–3.5 GHz DCO

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***Abstract*—This paper presents the first published fully-integrated digital fractional-N PLL based on a second-order frequency-to-digital converter (FDC) instead of a time-to-digital converter (TDC). The PLL's quantization noise is nearly identical to that of a conventional analog delta-sigma modulator based PLL ($\Delta\Sigma$-PLL). Hence, the quantization noise is highpass shaped and is suppressed by the PLL's loop filter to the point where it is not a dominant contributor to the PLL's output phase noise. However, in contrast to a $\Delta\Sigma$-PLL, the new PLL has an entirely digital loop filter and its analog components are relatively insensitive to non-ideal analog circuit behavior. Therefore, it offers the performance benefits of a $\Delta\Sigma$-PLL and the area and scalability benefits of a TDC-based digital PLL. Additionally, the PLL's digitally controlled oscillator (DCO) incorporates a new switched-capacitor frequency control element that is insensitive to supply noise and parasitic coupling. The PLL is implemented in 65 nm CMOS technology, has an active area of 0.56 mm^2, dissipates 21 mW from 1.0 and 1.2 V supplies, and its measured phase noise at 3.5 GHz is -123, -135, and -150 dBc/Hz at offsets of 1, 3, and 20 MHz, respectively. The PLL's power consumption is lower than previously published digital PLLs with comparable phase noise performance.**

***Index Terms*—Delta-sigma modulator, fractional-N, frequency synthesizer, PLL, TDC.**

I. Introduction

CONVENTIONAL analog fractional-N PLLs based on charge-pumps and digital delta-sigma modulators ($\Delta\Sigma$-PLLs) of the type shown in Fig. 1 are used extensively for frequency synthesis in high-performance applications such as wireless transceivers because of their fine tuning resolution and low phase noise [1]–[4]. Unfortunately, their performance tends to be limited by device leakage and low supply voltages in highly-scaled CMOS IC technology. Moreover, the narrow loop bandwidth necessary to suppress $\Delta\Sigma$ quantization noise often requires loop filter capacitance on the order of hundreds of picofarads, which usually dictates off-chip implementation and can add significantly to the overall system cost.

Several fractional-N PLL architectures based on time-to-digital converters (TDC-PLLs) such as shown in Fig. 2 have been proposed to mitigate these problems [5]–[30]. By using TDCs and digital filters in place of charge pumps and analog filters, TDC-PLLs offer reduced area, cost, and power consumption over conventional $\Delta\Sigma$-PLLs in highly-scaled CMOS technology. Unfortunately, TDC quantization noise is coarse and not as well suppressed by the PLL as $\Delta\Sigma$ quantization noise in $\Delta\Sigma$-PLLs, which has thus far prevented TDC-PLLs from achieving the phase noise and spurious tone performance demonstrated by state-of-the-art $\Delta\Sigma$-PLLs [31]–[40].

This paper presents the first published IC implementation of the $\Delta\Sigma$ frequency-to-digital converter (FDC) based PLL (FDC-PLL) architecture proposed in [41] which is an extension of that proposed in [42] and has higher-order quantization noise shaping than those presented in [43]–[45]. The FDC-PLL uses an FDC in place of a TDC in such a way that its quantization noise and loop dynamics are nearly identical to those of a $\Delta\Sigma$-PLL, yet its loop filtering is entirely digital as in a TDC-PLL. Although the FDC contains some analog components, it is relatively insensitive to non-ideal analog circuit behavior. The FDC-PLL IC's power consumption is lower than previously published digital PLLs with comparable phase noise performance, and its area is comparable to the lowest-area digital PLL in its performance class. Therefore, as demonstrated by the results presented in this paper, the FDC-PLL offers the benefits of both a $\Delta\Sigma$-PLL and a TDC-PLL.

Additionally, the paper presents two enhancements of the original FDC-PLL architecture that are also applicable to TDC-PLLs. Its digitally controlled oscillator (DCO) incorporates a new switched-capacitor frequency control element (FCE) that is insensitive to supply noise and parasitic coupling, and it incorporates a new timing scheme that reduces the potential for metastability that would otherwise arise from the need to resample the digital loop filter output across different clock domains.

II. FDC-PLL Signal Processing

A. Loop Overview

As illustrated in the high-level block diagram of Fig. 3, the FDC-PLL consists of a $\Delta\Sigma$ FDC, a digital loop controller (DLC), and a DCO. Its output frequency is $(N+\alpha)f_{ref}$, where N is an integer, α is between -0.5 and 0.5, and f_{ref} is the reference oscillator frequency. As shown in [41], the signal processing performed by the $\Delta\Sigma$ FDC when the PLL is locked

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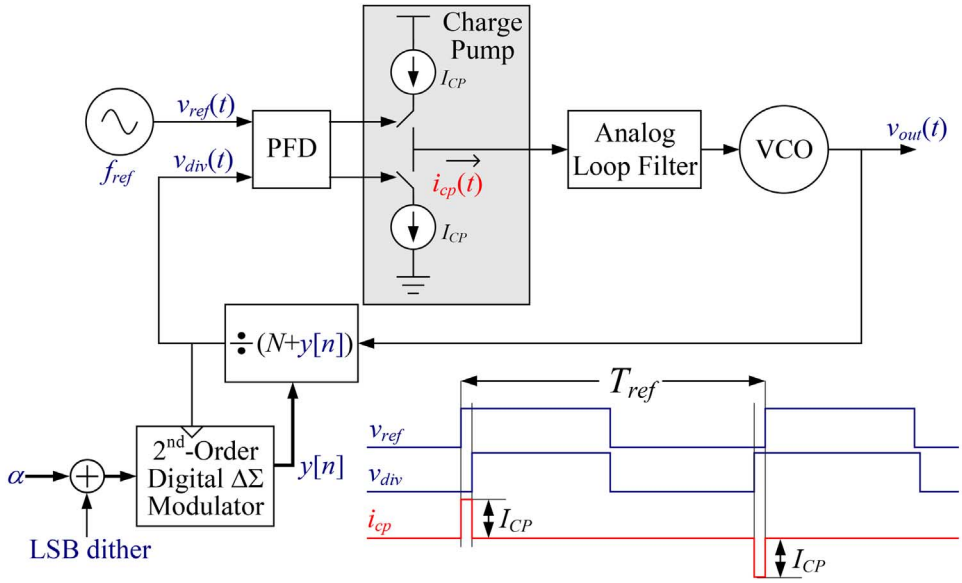

Fig. 1. Block diagram of a $\Delta\Sigma$ modulator based charge-pump fractional-N PLL ($\Delta\Sigma$-PLL) with output frequency $(N+\alpha)f_{ref}$, where N is an integer, α is a fractional value, and f_{ref} is the reference frequency.

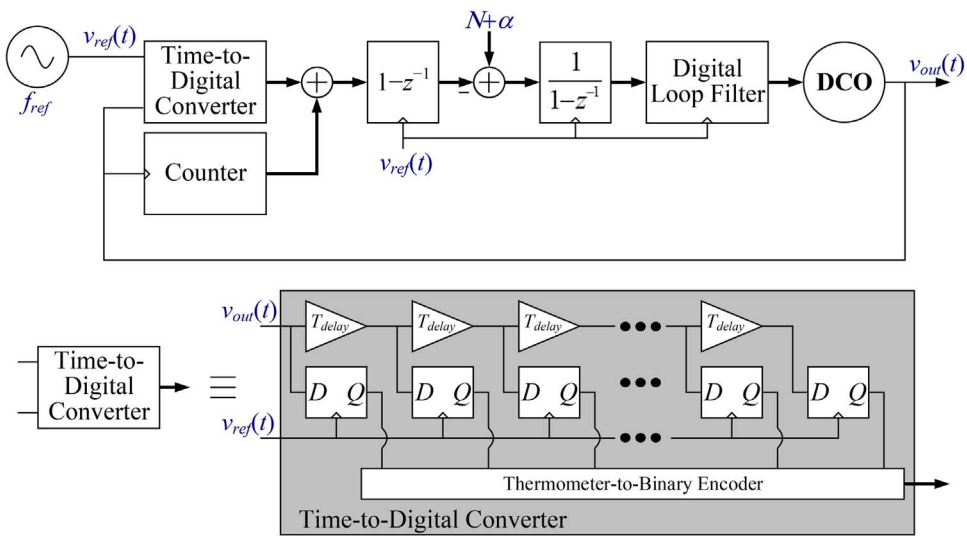

Fig. 2. Block diagram of a time-to-digital converter based fractional-N PLL (TDC-PLL) with output frequency $(N+\alpha)f_{ref}$.

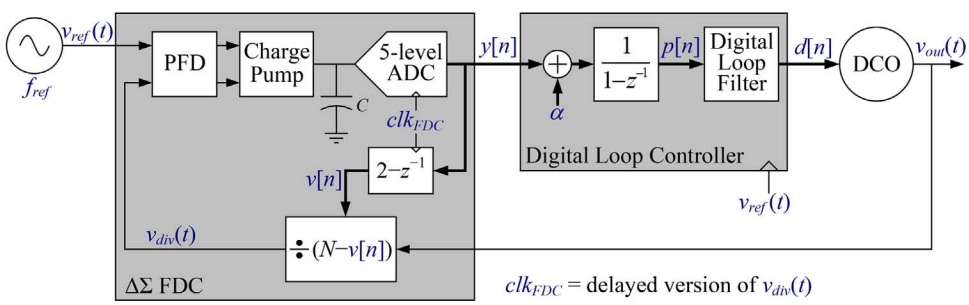

Fig. 3. Block diagram of a $\Delta\Sigma$ frequency-to-digital converter based fractional-N PLL (FDC-PLL) with output frequency $(N+\alpha)f_{ref}$.

is equivalent to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 4, where $\psi_{ref}[n]$ and $\psi_{PLL}[n]$ are the average frequency errors over the nth reference period of the reference oscillator and PLL output, respectively, $e_p[n]$ is the combined error from noise and other non-ideal circuit behavior in the charge pump, PFD, and divider, and $e_{ADC}[n]$ is ADC quantization noise.[1]

[1]Throughout this paper phase error sequences are in units of cycles, and frequency error sequences, such as $\psi_{ref}[n]$ and $\psi_{PLL}[n]$, are in units of Hz.

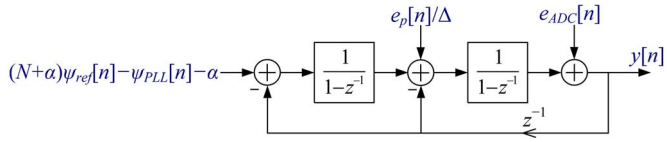

Fig. 4. Equivalent signal processing block diagram of the $\Delta\Sigma$ FDC in the FDC-PLL.

The $\Delta\Sigma$ modulator equivalence depicted in Fig. 4 implies that $y[n]$, which is the output of the 5-level ADC, is equal to $-\alpha$ plus second-order highpass shaped ADC quantization noise plus terms proportional $\psi_{ref}[n]$, $\psi_{PLL}[n]$, and $e_p[n]-e_p[n-1]$. The DLC accumulates $y[n]+\alpha$ and passes the result through the digital loop filter. The accumulator converts the frequency error terms to phase errors, the second-order highpass shaped ADC quantization noise to first-order highpass shaped noise, and the $e_p[n]-e_p[n-1]$ term to a term proportional to $e_p[n]$. Aside from the shaped quantization noise and $e_p[n]$ terms, the accumulator output, $p[n]$, can be interpreted as the FDC-PLL's phase error in cycles during the nth reference period.

The transfer function of the loop filter is $L(z) = L_{PI}(z)L_{LPF}(z)$ where

$$L_{PI}(z)=K_P+K_I\frac{1}{1-z^{-1}} \quad L_{LPF}(z)=\prod_{i=0}^{3}\frac{\lambda_i}{1-(1-\lambda_i)z^{-1}} \tag{1}$$

and K_P, K_I, and λ_i for $i = 0$, 1, 2, and 3 are constants. The constants are chosen such that $L_{PI}(z)$ sets the PLL's bandwidth and phase margin and $L_{LPF}(z)$ provides additional lowpass filtering outside of the PLL bandwidth to suppress out of band ADC quantization noise [46].

In the FDC-PLL IC the loop filter output has a 6-bit integer part and a 26-bit fractional part. This resolution is greater than required to achieve the targeted phase noise performance, so dithered quantization (not shown in Fig. 3) is applied to the loop filter output to reduce the bit width to 14 bits. The resulting DCO input sequence, $d[n]$, has a 6-bit integer part and an 8-bit fractional part. It causes the instantaneous frequency of the DCO during the nth reference period to be well approximated as:

$$f_{PLL}(t) = f_c + K_{DCO}d[n-1] + \psi_{DCO}(t) \tag{2}$$

where f_c, K_{DCO} and $\psi_{DCO}(t)$ are the DCO's nominal center frequency, gain, and instantaneous frequency error, respectively.[2]

B. $\Delta\Sigma$ Frequency-to-Digital Converter

The $\Delta\Sigma$ FDC concept and an early architecture were first presented in [47] and then presented again in [48]. The architecture was refined and rigorously analyzed in [49], and the first IC implementation was published in [50]. The version of the $\Delta\Sigma$ FDC used in this work is shown in Fig. 3 [41].

It consists of a phase-frequency detector (PFD), charge pump, capacitor, 5-level ADC, $2-z^{-1}$ digital block, and frequency divider. When the FDC-PLL is locked, each rising edge of the reference oscillator signal occurs within a small fraction of a reference period from a corresponding rising edge of the divider output [41]. In this paper, for each $n = 0, 1, 2, \ldots$, the time of the nth rising edge of the reference oscillator is denoted as t_n and the time of the corresponding rising edge of the divider output is denoted as τ_n. Without loss of generality the FDC-PLL is assumed to be locked by time t_0.

The PFD and charge pump implement the same functionality as in a conventional $\Delta\Sigma$-PLL (Fig. 1), although, as explained shortly, the charge pump current, I_{CP}, in an FDC-PLL tends to be lower than that in a $\Delta\Sigma$-PLL with comparable performance. The FDC-PLL's charge pump also contains an additional current source beyond the two shown in Fig. 1 that introduces an offset current pulse waveform [32], [39]. The offset current pulse waveform consists of a current pulse of nominal amplitude $-I_{CP}$ and duration $T_{OC} \cong 2.5$ ns each reference period such that $\tau_n > t_n$ for all n. Therefore, only the positive current source in the charge pump is modulated by the feedback loop once the FDC-PLL is locked.

The 5-level ADC samples the capacitor voltage shortly after each charge-pump current pulse settles to zero. The nth ADC output sample, $y[n]$, is applied to the DLC as described above, and is also applied to the $2-z^{-1}$ block so the nth divider modulus is $N-v[n]$, where $v[n] = 2y[n]-y[n-1]$. The divider and the $\Delta\Sigma$ FDC timing are such that each divider modulus value controls the time of the first rising edge of the divider output following the corresponding ADC sample time, i.e., such that $N - v[n]$ DCO cycles occur between times τ_n and τ_{n+1}.

As described above and proven in [41], the signal processing performed by $\Delta\Sigma$ FDC is equivalent to that of the second-order $\Delta\Sigma$ modulator shown in Fig. 4. Hence, well-known $\Delta\Sigma$ modulator results, e.g., see [51], imply that the ADC output sequence can be written as

$$y[n] = x[n] + e_{ADC}[n] - 2e_{ADC}[n-1] + e_{ADC}[n-2], \tag{3}$$

where

$$x[n] = (N+\alpha)\psi_{ref}[n] - \psi_{PLL}[n] - \alpha + \frac{e_p[n]-e_p[n-1]}{\Delta} \tag{4}$$

and Δ is the flash ADC's nominal step size. Furthermore, it follows from the results presented in [52] that even a small amount of input-referred thermal noise causes the ADC quantization noise, $e_{ADC}[n]$, to well-approximate a white, zero-mean, uniformly distributed random process. Therefore, the ADC quantization noise is "well-behaved" like the quantization noise introduced by a dithered digital $\Delta\Sigma$ modulator in a conventional $\Delta\Sigma$-PLL [53], [54].

The equivalent $\Delta\Sigma$ modulator's first accumulator is the result of phase being the integral of frequency, its second accumulator is implemented by the $\Delta\Sigma$ FDC's charge pump and the capacitor, and both of its feedback loops are implemented by the $\Delta\Sigma$ FDC's $2-z^{-1}$ local feedback loop through the divider [41]. Consequently, the FDC-PLL's implementation of the $\Delta\Sigma$ modulator's first accumulator and outer feedback path are inherently ideal. To the extent that the charge pump implements ideal current sources and the integrating capacitor is an ideal capacitor,

[2]The *DCO Gain* is defined as the amount by which the DCO frequency changes when $d[n]$ changes by unity.

the transfer function of the second accumulator in the equivalent $\Delta\Sigma$ modulator is given by

$$\left[\frac{I_{CP}}{(N+\alpha)f_{ref}C\Delta}\right]\frac{1}{1-z^{-1}} \tag{5}$$

The values of I_{CP}, C, and Δ are set to approximate

$$I_{CP} = (N+\alpha)f_{ref}C\Delta, \tag{6}$$

so the nominal gain of the second accumulator is unity as depicted in Fig. 4. As in a conventional second-order $\Delta\Sigma$ modulator, the quantization noise transfer function of the $\Delta\Sigma$ FDC is relatively insensitive to the gain of its second accumulator [41]. For example, varying I_{CP} by $\pm 10\%$ about the ideal value specified by (6) does not cause the performance of the FDC-PLL to change significantly from that reported in Section IV of this paper. Similarly, and also like a conventional $\Delta\Sigma$ modulator, the $\Delta\Sigma$ FDC's performance is not highly sensitive to non-ideal behavior of either the charge pump or the ADC.

Both the charge pump and ADC are non-differential, a design choice that was made because of the FDC-PLL's low sensitivity to their performance. The ADC's nominal step-size is $\Delta = 40$ mV. The DCO's frequency range, and therefore the maximum range of $(N+\alpha)f_{ref}$, is 2.8 GHz and 3.5 GHz, so, as dictated by (6), I_{CP} is less than 200 μA.

C. Signal Processing Comparison to TDC-PLLs

To date, low-noise TDC-PLLs have been published with TDCs that either perform coarse quantization without quantization noise shaping [5]–[27] or with first-order highpass quantization noise shaping, [28]–[30], [55], [56]. TDC quantization noise is injected at the input of the digital loop filter and the output of the digital loop filter adjusts the DCO's frequency. Quantization is a highly nonlinear process, so coarse quantization tends to introduce strong spurious tones and wideband input-dependent error. First-order quantization noise shaping attenuates the error at low frequencies, and the digital loop filter bandwidth can be chosen to attenuate the error at higher frequencies. However, the quantization noise from quantization noise shaping TDC architectures published to date is mathematically equivalent to the quantization noise of a first-order $\Delta\Sigma$ modulator. Unfortunately, even in the absence of non-ideal circuit behavior, first-order $\Delta\Sigma$ modulators are notorious for having quantization noise that varies widely with input amplitude and contains strong spurious tones [51].

In contrast, the power spectral density (PSD) of the quantization noise from a second-order $\Delta\Sigma$ modulator with at least a two-bit quantizer and an arbitrarily low level of input-referred white noise is identical to the output of a filter with transfer function $(1-z^{-1})^2$ driven by white noise of variance $\Delta^2/12$ [52]. Therefore, in the absence of non-ideal circuit behavior, the quantization noise from a second-order $\Delta\Sigma$ modulator has an input-independent PSD and is free of spurious tones.

As described above, the second-order shaped quantization noise from the $\Delta\Sigma$-FDC gets converted to first-order shaped noise at the input to the digital loop filter in the FDC-PLL. In this sense, the FDC-PLL is like a TDC-PLL with a first-order quantization nose shaping TDC. The primary signal processing difference is that the first-order shaped noise in the FDC-PLL originates from the equivalent of a second-order $\Delta\Sigma$ modulator, so in principle it is expected to be signal-independent and free of spurious tones.

D. Signal Processing Comparison to $\Delta\Sigma$-PLLs

The bandwidth and phase margin of a conventional $\Delta\Sigma$-PLL depend on the charge pump current and loop filter capacitance, both of which must be relatively large to achieve the narrow loop bandwidth required to suppress $\Delta\Sigma$ quantization noise without introducing excessive circuit noise. In the case of the FDC-PLL with a loop filter of the form described above, the PLL bandwidth is

$$f_{BW} \cong \frac{K_{DCO}K_P}{2\pi} \tag{7}$$

and to a good approximation the phase margin depends only on K_{DCO}, K_P, K_I, and f_{ref} [41]. Therefore, in contrast to a $\Delta\Sigma$-PLL, the charge pump current and capacitance in the FDC-PLL do not affect the PLL bandwidth or phase margin, so their values can be chosen on the basis of only noise and power dissipation considerations. This allows them to be much smaller than their counterparts in a comparable $\Delta\Sigma$-PLL.

In a $\Delta\Sigma$-PLL, the $\Delta\Sigma$ quantization noise is generated with perfect accuracy in the digital domain and LSB dither causes it to be free of spurious tones. However, the $\Delta\Sigma$ quantization noise is inevitably subjected to nonlinear distortion from non-ideal analog circuit behavior such as charge pump current source mismatches which can induce spurious tones [39]. The opposite situation occurs in the FDC-PLL. Its $\Delta\Sigma$ quantization noise is generated via analog components, so excessive non-ideal analog circuit behavior such as low charge pump output impedance can induce spurious tones. However, the components between the FDC and DCO are digital so the $\Delta\Sigma$ quantization noise is not subjected to nonlinear distortion after the FDC that could further induce spurious tones.

E. DCO Frequency Control

The DCO is an analog LC oscillator whose frequency is controlled by banks of fine, intermediate, and coarse frequency control elements (FCEs) as shown in Fig. 5. Each FCE contributes to the DCO's tank a capacitance that can take on one of two values depending on the state of the FCE's input bit. The nominal minimum step sizes of the fine, intermediate, and coarse FCE banks are 12 kHz, 390 kHz, and 5.3 MHz, respectively, and their nominal frequency ranges are 768 kHz, 24.57 MHz, and 673.1 MHz, respectively. The DCO's center frequency is 3.15 GHz, so the FCE banks can tune the DCO over a nominal range of 2.8 GHz to 3.5 GHz in nominal steps of 12 kHz. The nominal frequency ranges of the fine and intermediate FCE banks are significantly larger than the nominal step sizes of the intermediate and coarse FCE banks, respectively, to avoid frequency gaps much larger than 12 kHz anywhere in the DCO's tuning range even with inevitable FCE component mismatches.

The coarse and intermediate FCE banks are controlled from off-chip via a serial port interface (SPI) and the fine FCE bank is controlled by the output of the DLC, $d[n]$. Simulations and

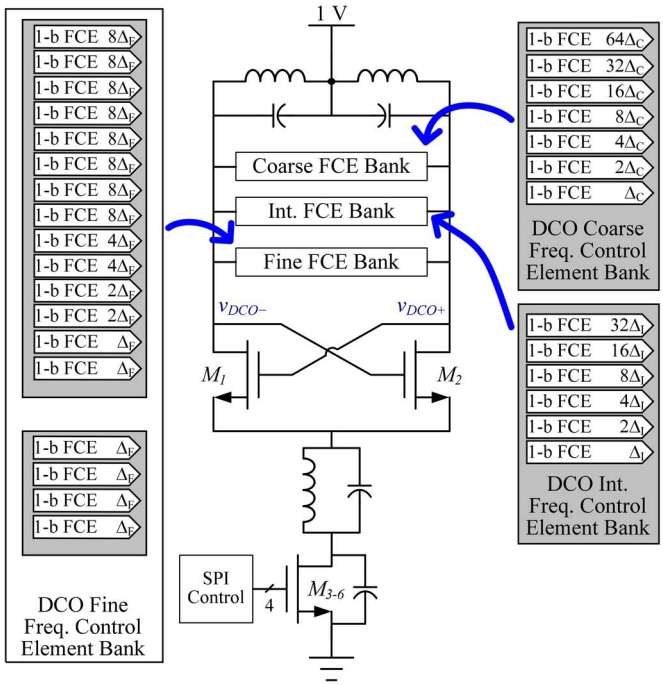

Fig. 5. Digitally controlled oscillator.

analysis indicate that the 768 kHz frequency range of the fine FCE bank is more than large enough to accommodate the output swing of the DLC when the FDC-PLL is locked in the absence of significant DCO temperature or power supply voltage drifts. In applications that require the FDC-PLL to be locked for periods of time that are long enough for temperature or supply voltage changes to cause the DCO's center frequency to change by more than several hundred kHz, a larger fine FCE bank frequency range or an algorithm to adaptively update the intermediate FCE bank settings would be required to maintain lock.

The FDC-PLL prototype was designed to achieve the GSM mobile telephone standard's strict phase noise specifications. The standard dictates phase noise of no more than -150 dBc/Hz at a 20 MHz offset for a 3.5 GHz output frequency, which places a practical requirement that the DCO's thermal noise be the dominant source of phase noise at offset frequencies between 10 and 20 MHz [5]–[7], [11]. A minimum DCO frequency step of 200 Hz is necessary to ensure that the DCO's quantization noise is not a significant contributor to the PLL's phase noise in the 10–20 MHz offset frequency range.

The minimum MOM capacitor size realizable via the project's design kit library is 0.375 fF. Had FCEs been used that simply switch this minimum capacitance in and out of the DCO tank, the corresponding minimum DCO frequency step would have been about 570 kHz. Instead, as described in Section III-B, a new switched capacitor structure is introduced that combines four MOM capacitors and a switch such that the capacitance introduced into the DCO tank by the minimum-size FCE in the fine FCE bank changes by only about 18 aF when the FCE control bit changes state. This corresponds to a minimum frequency step of about 12 kHz.

Unfortunately, the 12 kHz minimum frequency step is still much larger than 200 Hz. Therefore, as is commonly done in TDC-PLLs, the integer part of $d[n]$ controls the DCO directly and the fractional part of $d[n]$ is oversampled and quantized by a digital $\Delta\Sigma$ modulator prior to the DCO [5]–[7], [11]. In typical designs the $\Delta\Sigma$ modulator is clocked between $f_{PLL}/16$ and $f_{PLL}/4$ to limit power consumption and satisfy the timing requirements of the $\Delta\Sigma$ modulator's digital logic [57]. In the FDC-PLL IC, the $\Delta\Sigma$ modulator clock frequency is approximately $f_{PLL}/16$ as described in detail in the next section. The highpass shaped quantization noise from the $\Delta\Sigma$ modulator frequency modulates the DCO, but the resulting phase noise is attenuated by the intrinsic frequency-to-phase integration of the DCO. Consequently, the phase noise introduced by the $\Delta\Sigma$ modulator's quantization noise is well below the phase noise floor of the FDC-PLL. Given that the integer part of $d[n]$ controls the DCO frequency in steps of 12 kHz, it follows that the 8-bit fractional part of $d[n]$ controls the DCO frequency in steps of about 50 Hz, which is well below the 200 Hz requirement.

III. FDC-PLL Circuit Details

The FDC-PLL IC was fabricated in the STMicroelectronics 65 nm, 7 metal layer, CMOS process. It consists of the core FDC-PLL blocks and SPI mentioned in the previous section, as well as a crystal buffer, divider buffer, output buffer, and bias generator. The PFD, charge pump, ADC, bias generator, and crystal buffer are implemented with low-power (LP) MOS transistors and operate from a supply voltage of 1.2 V. The other IC blocks are implemented with general-purpose (GP) MOS transistors and operate from a supply voltage of 1.0 V. All capacitors are either MOS bypass capacitors or MOM capacitors. The IC occupies 1 mm by 1.3 mm including pads and ESD circuitry, and its active area is 0.56 mm^2.

A. Digitally Controlled Oscillator

The DCO topology is shown in Fig. 5. Except for the FCE banks, it is a conventional LC oscillator [58]. Its tank consists of a two-turn 1.5 nH center-tapped inductor in parallel with fixed capacitors and the three FCE banks. The inductor is from the STMicroelectronics design kit library and has a differential quality factor of 16.5 at 3.5 GHz. The cross-coupled nMOS switching transistors are thick-oxide devices to accommodate the DCO's output swings of up to 1.8 V. The DCO's current is controlled by four parallel power-of-two-weighted nMOS tail transistors that can each be turned off or biased in triode under SPI control. A 10 pF capacitor in parallel with the tail transistors shunts their noise to limit its contribution to the DCO's phase noise. A parallel inductor and capacitor between the switching and tail transistors boosts the impedance between the switching transistors and ground at frequencies around the DCO's second harmonic to prevent the switching transistors from excessively loading the DCO's tank [58].

B. Fine Frequency Control Elements

As described in Section II-E, each FCE takes on one of two capacitance values depending on the state of its input bit. The FCEs published to date are implemented as either switched capacitors or as MOS varactors with two-level control voltages

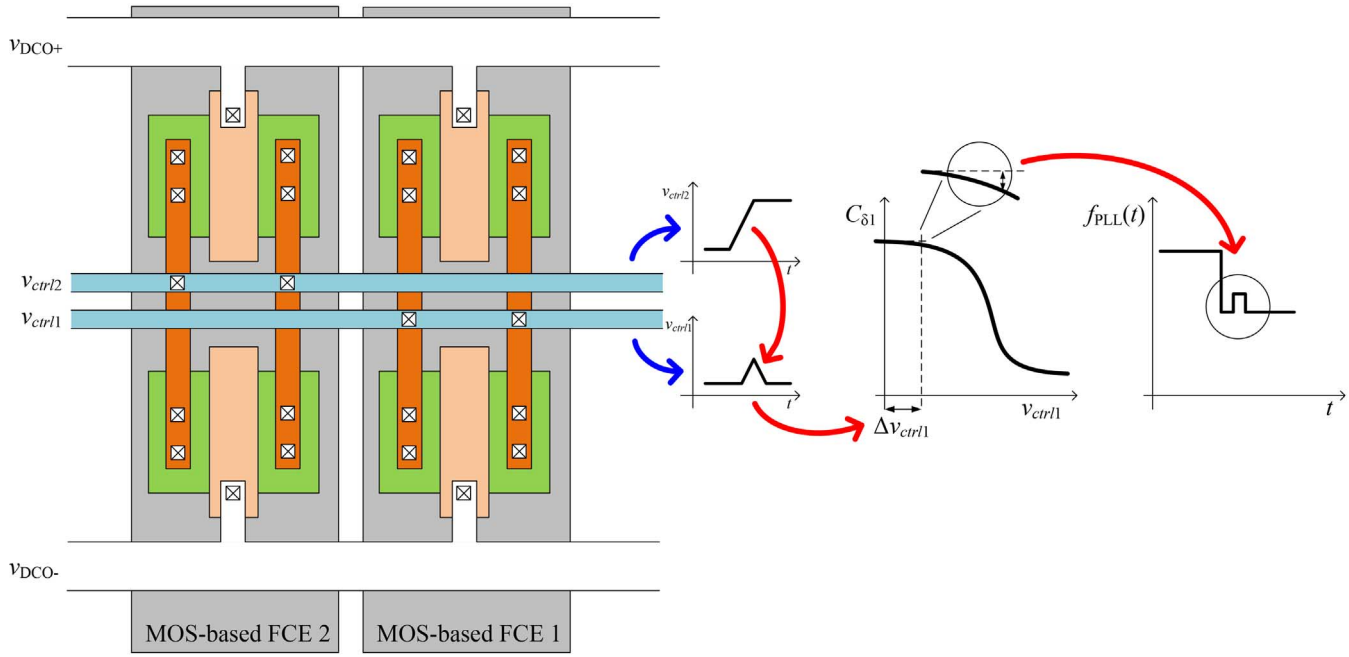

Fig. 6. Example of how cross-talk between the control lines of two different MOS-based FCE's causes unintended frequency modulation of the DCO.

[5]–[30]. Such FCEs have been demonstrated to have capacitance steps as low as tens of attofarads, and, when implemented in parallel with the DCO tank, to have frequency steps as low as tens of kHz.

The minimum frequency step can be further reduced by connecting the FCEs to the DCO such that the tank sees a scaled version of their capacitance steps. One approach is to connect the FCEs across the sources of the DCO's cross-coupled transistors [24], [59]. Another approach is to inductively couple the FCEs to the DCO tank [30]. Both approaches enable very small minimum frequency steps, e.g., as low as 150 Hz in [59]. Furthermore, compared to connecting the FCEs in parallel with the DCO tank, the techniques offer improved FCE matching because they use larger FCEs for any given minimum frequency step. However, they both have the potential to reduce the DCO's quality factor and involve added complexity. Neither technique was used in this work because they were not deemed necessary to achieve the desired target specifications. Nevertheless, the new FCEs proposed below are applicable to the two techniques.

MOS varactor based FCEs consist of two MOS capacitors with their sources and drains driven by a shared control voltage and their gates driven by the respective differential DCO outputs. The control voltage is a two-level signal, often from a buffer driven by the FCE's control bit. Although the capacitance introduced into the tank by the FCE varies over the DCO period, its average value over any given DCO period depends on the state of the control voltage during that period [60]. The high and low control voltage levels, which are often the supply voltages, are chosen such that small variations in the two voltage levels cause as little change as possible in the average capacitance.

However, the average capacitance versus voltage curve is never completely flat around the control voltage levels, so disturbances coupled into the control lines of MOS varactor based FCEs can be a source of DCO phase noise. For example, suppose the input bit to an FCE does not change state but that of an adjacent FCE does change state at a given clock edge. Ideally, the control voltage of the first FCE would remain constant while that of the second FCE transitions between levels. Unfortunately, the transition of the second FCE's control voltage can induce a disturbance on the control voltage of the first FCE which causes a DCO frequency glitch as depicted in Fig. 6. Similarly, disturbances coupled into the power supply lines of the FCE control voltage buffers also cause DCO frequency glitches. Originally the FDC-PLL IC was designed with MOS varactor based FCEs, but simulations with post layout extracted parasitics suggested that these phenomena would significantly degrade the FDC-PLL's phase noise.

The new switched capacitor based FCE shown in Fig. 7(a) was developed to circumvent these issues. It consists of two sets of two MOM capacitors with slightly different values, denoted as C_F and $C_F+\delta_F$ for the unit-weight FCEs, and an nMOS transistor switch. The switch consists of a switching transistor sandwiched between half-sized dummy transistors to cancel charge injection. When the switch is open, the top and bottom pairs of capacitors in Fig. 7(a) are each connected in series across the DCO tank. When the switch is closed, the parallel combination of the two left capacitors in Fig. 7(a) and that of the two right capacitors in Fig. 7(a) are connected in series across the DCO tank. Therefore, the change in DCO tank capacitance when the FCE's input bit is switched from high to low is

$$C_{\delta F} = \frac{\delta_F^2}{4C_F + 2\delta_F} \tag{8}$$

It follows that $C_{\delta F}$ can be made very small, and it is a monotonic function of the difference between the FCE's two capacitor sizes, δ_F. The monotonicity ensures that any bank of nominally equal FCEs will exhibit monotonic behavior no matter how small $C_{\delta F}$ is or how poorly matched the FCE capacitors

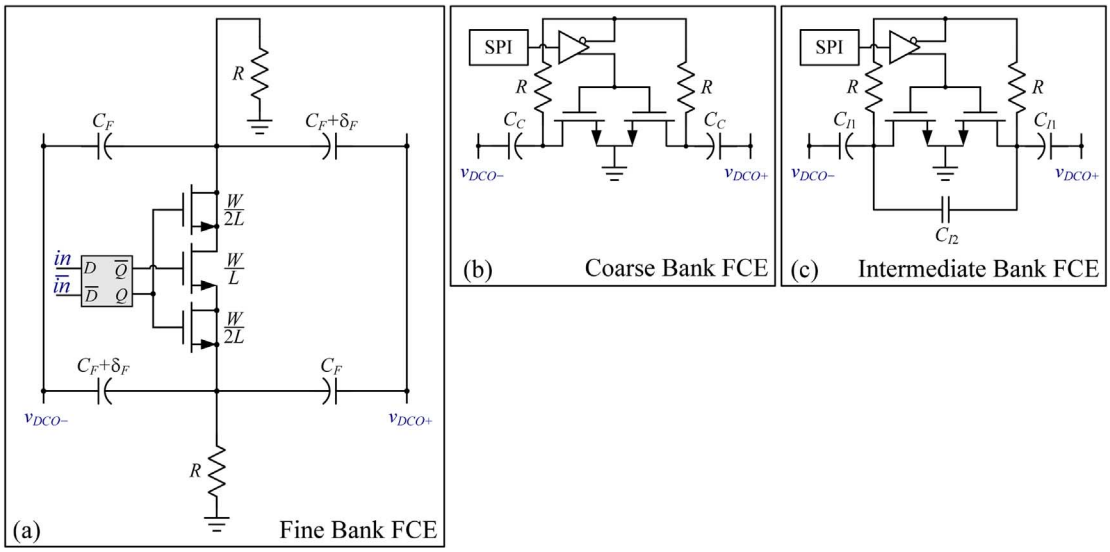

Fig. 7. The DCO's (a) fine, (b) coarse, and (c) intermediate frequency control elements (FCEs).

are. Equation (8) also implies that $C_{\delta F}$ can be made quite large because every doubling of δ_F increases $C_{\delta F}$ by approximately a factor of 4. The practical upper limit on $C_{\delta F}$ is dictated by the maximum fixed FCE capacitance acceptable for a given application; the FCE's fixed capacitance is less than $C_F + \delta_F/2$.

In the prototype IC, $C_F = 7.37$ fF and $\delta_F = 0.75$ fF, so the minimum capacitance step-size of the fine FCE bank is $C_{\delta F} \cong 18$ aF. The nodes to which the switch is connected have low voltage swings because $C_F \gg \delta_F$, so charge redistribution occurs quickly when the switch closes and any charge injection not cancelled by the dummy transistors mainly affects the DCO common mode voltage. To the extent that the switch's leakage and on-resistance are negligible, the FCE avoids the coupling problems described above for MOS varactor based FCEs.

The FCE switch is controlled by a fully differential D flip-flop, which consists of two copies of a low-hysteresis flip-flop [61]. The flip-flop clocks and inputs are provided differentially to minimize the net current flow across the power supply domains of the DLC and fine FCE bank. Simulations indicate that the quality factor of the unity-weighted FCE is 185, which implies that the bank of fine FCEs is not a significant contributor to the DCO's phase noise.

Random IC fabrication errors cause the FCE capacitors, and therefore the capacitance steps of the FCEs, to deviate from their ideal values by amounts that can be modelled as samples of independent random variables. As shown in the Appendix, this implies that the relative error of the unit-weight FCE capacitance step satisfies

$$\frac{\sigma_{\delta F}}{C_{\delta F}} \cong \sqrt{\frac{C_F}{C_{\delta F}}}\left(\frac{\sigma_F}{C_F}\right) \tag{9}$$

provided $C_F \gg \delta_F$, where σ_F and $\sigma_{\delta F}$ are the standard deviations of each C_F capacitor and the FCE's capacitance step, respectively. For the prototype IC, the expected relative error of each C_F capacitor is about 0.01, so (9) implies that the expected relative error of the 18 aF FCE capacitance step is about 0.2.

Typically, scaling the size of a capacitor on an IC by a factor of 1/x causes the relative capacitance error to scale by a factor of $\sqrt{x}$ [62], [63]. Therefore, (9) implies that the relative error of the unit-weight FCE capacitance step is the same as would be expected of a physically implemented capacitor of value $C_{\delta F}$ if it were possible to implement such a small capacitor directly.

This is an important property of the FCE of Fig. 7(a) that is not shared by other methods of synthesizing small capacitance steps from larger capacitors. For example, suppose an FCE were implemented that switches a capacitor of size C_F into the DCO tank when the FCE's input bit is high and replaces it with a capacitor of size $C_F + C_{\delta F}$ when the FCE's input bit is low. The FCE's capacitance step would therefore be $C_{\delta F}$, and given that it is usually possible to realize IC capacitors that differ by less than the minimum realizable capacitor size, $C_{\delta F}$ could be made quite small. However, it can be verified that the relative error of the FCE's capacitance step would be $\sqrt{2C_F/C_{\delta F}}$ larger than the right side of (9). For example, the expected relative error of an 18 aF FCE capacitance step would be about 29 times larger than that of the FCE of Fig. 7(a).

C. Fine FCE Bank and Its Control Interface

As indicated in Fig. 8, the fine FCE bank consists of 14 FCEs, each of which ideally adjusts the DCO frequency by $\pm K\Delta_F/2$ depending on its input bit, where K is the FCE's *weight* and is 1, 2, 4, or 8, and Δ_F has a nominal value of 12 kHz. The DCO input sequence, $d[n]$, is updated once per reference period. The encoder shown in Fig. 8 maps each sample of $d[n]$ to a 14-bit segmented code, $c_I[n]$, which represents the integer part of $d[n]$, and a 9-bit two's complement fractional part, $x_f[n]$. The fractional part of $d[n]$ is an 8-bit sequence, so the bit width of $x_f[n]$ is one bit larger than necessary. The extra bit and the FCE weights shown in Fig. 8 were implemented for future compatibility with a new segmented multirate dynamic element matching (DEM) algorithm extended from work presented in

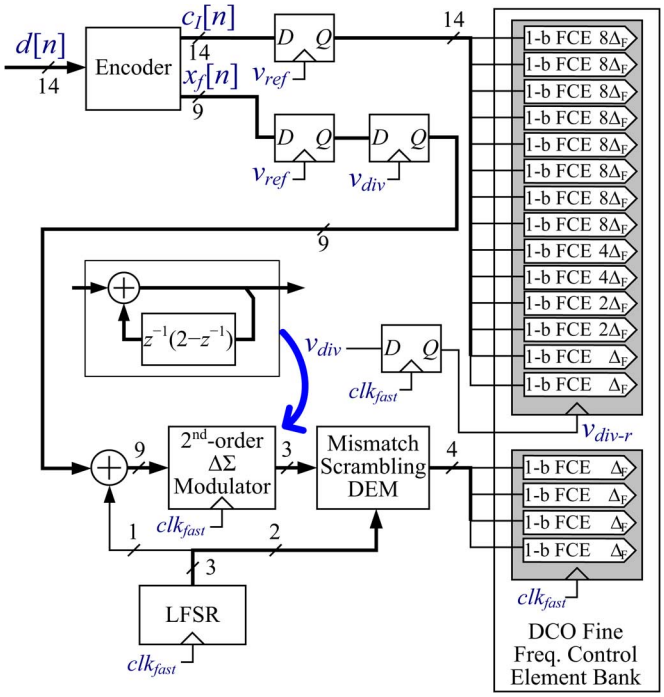

Fig. 8. The DCO's fine FCE bank control interface.

[64], but the new DEM algorithm is not used in this work so the mapping performed by the encoder is deterministic.

To reduce the possibility of disturbing the sampling phase of the ADC, which occurs shortly after each rising edge of the divider output, the DLC is clocked on the reference signal so it settles before the flash ADC is sampled. Therefore, both $c_I[n]$ and $x_f[n]$ are updated on each rising edge of the reference. As shown in Fig. 8 and described below, $x_f[n]$ is resampled on the divider output and $c_I[n]$ is first resampled on the reference signal and then sampled into the FCE's on clock edges that each occur shortly after a rising edge of the divider output. Metastability is avoided in these resampling operations because, as mentioned above, the charge pump's offset current pulse waveform ensures that when the PLL is locked the nth rising edge of the divider output always occurs after the nth rising edge of the reference oscillator. While metastability events can potentially occur before the PLL locks, they are rare and only occur when the PLL is so far out of lock that its feedback information is not meaningful. Hence, they do not significantly affect the locking process.

The resampled version of $x_f[n]$ is applied to an oversampled error-feedback second-order digital $\Delta\Sigma$ modulator with LSB dither [51]. The encoder is such that $x_f[n]$ takes on values that range from -1 to $-1/256$ with a minimum step-size of 1/256. The digital $\Delta\Sigma$ modulator's input is an oversampled version of $x_f[n]$ plus LSB dither which takes on values of 0 and 1/256 with equal probability. The quantization step size of the digital $\Delta\Sigma$ modulator is unity, so its output takes on values of -2, -1, 0, and 1. The LSB dither ensures that the digital $\Delta\Sigma$ modulator's quantization noise is asymptotically independent of $x_f[n]$ and the dither, and has a PSD equal to that of the output of a filter with transfer function $(1-z^{-1})^2$ driven by white noise with a variance of 1/12. It is possible that the PLL's phase noise could have been relied upon to achieve approximately the same result in the absence of LSB dither, but the cost of LSB dither in terms of area and power consumption is negligible so it was included to ensure the result. Furthermore, it is certainly beneficial during open loop measurement of the DCO's phase noise.

The DEM encoder shown in Fig. 8 is a mismatch-scrambling tree structure with three switching blocks based on extra-LSB encoding to simplify the logic [65]. Its purpose is to scramble the usage pattern of the four FCEs it drives such that mismatches among the FCEs do not cause nonlinear distortion [66]. The rationale for including DEM is that nonlinear distortion is known to induce spurious tones in $\Delta\Sigma$ quantization noise [39]. An LFSR generates the $\Delta\Sigma$ modulator LSB dither and two pseudo-random bit sequences used by the DEM encoder.

The v_{div} signal shown in Fig. 8 is the main divider output signal described previously. The clk_{fast} signal is also generated by the divider (as a byproduct of its design, as shown in Fig. 9 [67]) and is synchronous to v_{div}. When $N-v[n]$ is a multiple of 16, every clk_{fast} period in the corresponding divider period is 16 DCO periods long. When $N-v[n]$ is not a multiple of 16, all but one of the clk_{fast} periods in the corresponding divider period are 16 DCO periods long, and one clk_{fast} period is extended by up to 15 extra DCO periods to ensure that the next rising edge of v_{div} is synchronous to a rising edge of clk_{fast}. This ensures that there are an integer number of clk_{fast} periods in each divider period, so metastability is avoided in the flop-flops clocked by clk_{fast} that sample signals which are synchronous with v_{div}. A potential drawback of this scheme is that the FCEs clocked by clk_{fast} have a time-varying period, which causes high-frequency quantization noise to fold down to low frequencies. However, simulations indicate that the error caused by this phenomenon is well below the phase noise floor of the FDC-PLL.

For loop bandwidths of 100 kHz or lower, the signal swing of $d[n]$ resulting from FDC quantization noise and other noise sources in the FDC-PLL is much smaller than unity. Therefore, for most FDC-PLL output frequencies, only the FCEs controlled by the fractional part of $d[n]$ via the digital $\Delta\Sigma$ modulator toggle when the FDC-PLL is locked. However, if the FDC-PLL frequency is such that the mean of $d[n]$ is near an integer boundary, the slower-clocked FCEs controlled by the integer part of $d[n]$ can also toggle even when the FDC-PLL is locked. In the absence of FCE mismatches, such toggling of the slow FCEs has no effect on performance. Yet mismatches are inevitable, and simulations indicate that the expected level of mismatches can degrade the FDC-PLLs phase noise between about 40 kHz and 2 MHz offsets by up to 10 dB in such boundary cases.

This issue is shared by the majority of TDC-PLLs because most oversample and quantize the fractional part of their loop filter outputs along the lines described above. Unfortunately, it is not widely reported in the literature to the knowledge of the authors, and was not appreciated by the authors until after the FDC-PLL IC was submitted for fabrication. Otherwise, digital logic would have been included that detects when $d[n]$ is near an integer boundary and dynamically adds one to $x_f[n]$ when necessary such that $c_I[n]$ can remain constant even when the integer part of $d[n]$ changes by one.

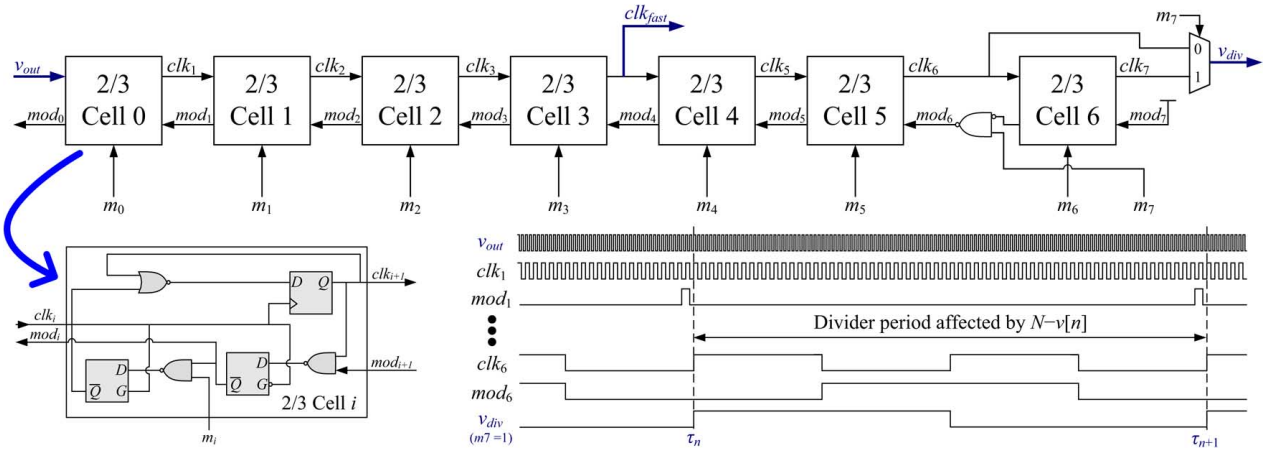

Fig. 9. Simplified architecture and operation of the frequency divider (circuitry that resynchronizes the divider outputs to v_{out} is used but not shown).

D. Coarse and Intermediate FCE Banks

The FCEs in the fine FCE bank are capable of accurately synthesizing very small capacitance steps, as described above, but they would not be area-efficient if used to synthesize very large capacitance steps. The FCE shown in Fig. 7(b) is more area-efficient for synthesizing very large capacitance steps, so it is used in the coarse FCE bank.

The coarse FCE bank consists of 7 power-of-two-weighted FCEs of the form shown shown in Fig. 7(b), and has a nominal minimum frequency step of $\Delta_C = 5.3$ MHz. Each FCE consists of a pair of capacitors that are connected in series across the DCO tank when the FCE's input bit is high and disconnected from each other when the FCE's input bit is low. When disconnected from each other, the bottom plates of the capacitors are connected to the positive supply voltage through large resistors to prevent forward biasing of the pn junctions in the nMOS transistors. In the unit-weight coarse FCE, $C_C = 14$ fF, $R = 40$ kΩ, and each nMOS switch has a simulated $R_{on} = 43$ Ω, so the FCE's quality factor is 74.

Even with the smallest available MOM capacitors, the minimum frequency step of the coarse FCE bank would be larger than the frequency range of the fine FCE bank. Therefore, an intermediate FCE bank is required to bridge the gap. The intermediate FCE bank consists of 6 power-of-two-weighted FCEs of the form shown in Fig. 7(c), and has a nominal minimum frequency step of $\Delta_I = 390$ kHz. The FCE differs from those in the coarse FCE bank only in that a capacitor is connected across the switch. When the FCE's input bit is high, the two C_{I1} capacitors are connected in series across the DCO tank, and when the FCE's input bit is low, the two C_{I1} capacitors and the C_{I2} capacitor are connected in series across the DCO tank. In the unit-weight intermediate FCE, $C_{I1} = 3.6$ fF, $C_{I2} = 12$ fF, $R_{on} = 113$ Ω, so the FCE's quality factor is 111.

IV. Measurement Results

A die photograph of the FDC-PLL IC is shown in Fig. 10. The IC was tested in a QFN 24 package soldered on a custom printed circuit test board. Its measured power consumption is 21 mW.

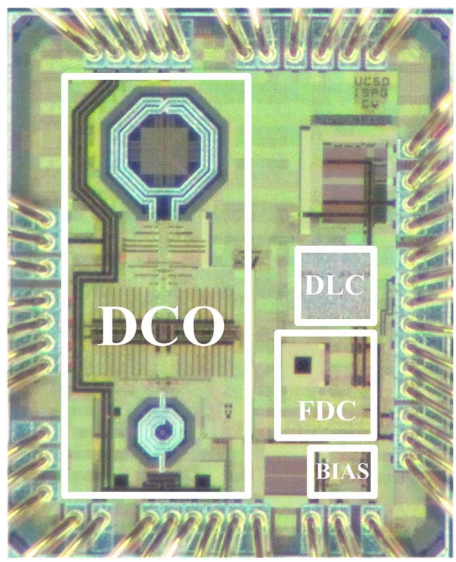

Fig. 10. Die photograph.

TABLE I
Supply Voltages and Measured Current Consumption of the Various FDC-PLL Circuit Blocks

Circuit	Supply Voltage	Current
Digitally Controlled Oscillator	1.0 V	9.84 mA
Fine-Bank FCE Flip Flops	1.0 V	0.13 mA
DLC, DCO input encoder and ΔΣ modulator	1.0 V	2.04 mA
Charge Pump, PFD, and ADC	1.2 V	1.85 mA
Divider	1.0 V	0.36 mA
Bias Generator	1.2 V	0.96 mA
Crystal Oscillator Buffer	1.2 V	0.65 mA
Divider Buffer and Output Buffer	1.0 V	4.41 mA

Table I provides a breakdown of the supply voltage and measured current consumption by circuit block, and Table II provides a summary of the FDC-PLL IC's measured performance.

TABLE II
PERFORMANCE TABLE WITH COMPARISON TO RELEVANT PRIOR ART

	This Work	[28]	[11]	[6]	[20]	[24]	[25]
Technology	65 nm	130 nm	130 nm	90 nm	65 nm	55 nm	65 nm
Supply (V)	1.0/1.2	1.5	Not Stated	1.2	1.2/2.5	1.5	1.5/1.2
Reference Frequency (MHz)	26	50	26	26	35	26	78
Output Frequency (GHz)	3.5	3.7	3.6	0.9	3.5	1.8	4.0
Bandwidth (kHz)	40	500	50	40	3400	800(***)	Not Stated
In-band Phase Noise (dBc/Hz)	-70	-108	-79	-81	-101	-102	-109
Out-of-band Phase Noise (dBc/Hz)	-123@1MHz -135@3MHz -150@20MHz	-132@3MHz -150@20MHz	-126@1MHz -135@3MHz -152@20MHz	-117@1MHz -152@20MHz	-123@3MHz(*)	-154@20MHz	-150@20MHz
Fractional Spur Power (dBc)	-43	-42	Not Stated	Not Stated	-58	-50	-40
Reference Spur Power (dBc)	-82	-65	-84	Not Stated	-61	Not Stated	-56
Power Consumption (mW)	21	46.7	45.6	50.4	28(**)	41.6	45
Area (mm^2)	0.56	0.95	0.86	Not Stated	0.44	0.7	0.6

(*) For DCO only.
(**) Includes input and output buffers (19.3 mW at 2.5 V) for consistency with other PLLs in the table.
(***) The maximum bandwidth achievable by the PLL is 3 MHz. The figure reported is for the case for which measurement data was reported in the paper.

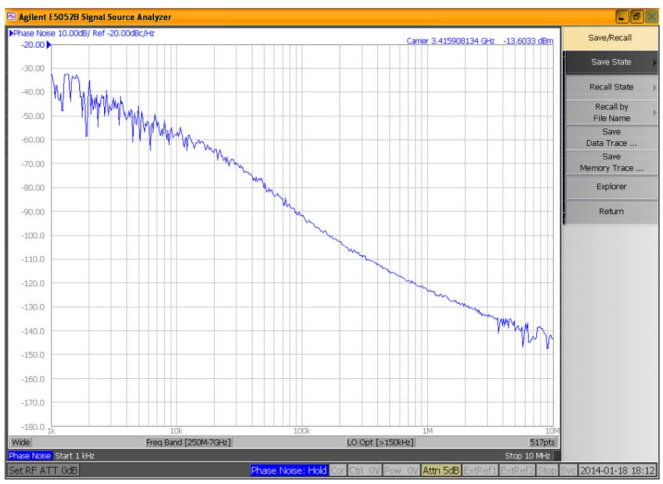

Fig. 11. Representative measured FDC-PLL phase noise spectrum, the corresponding phase noise spectrum predicted by the theoretical results, and the GSM phase noise mask.

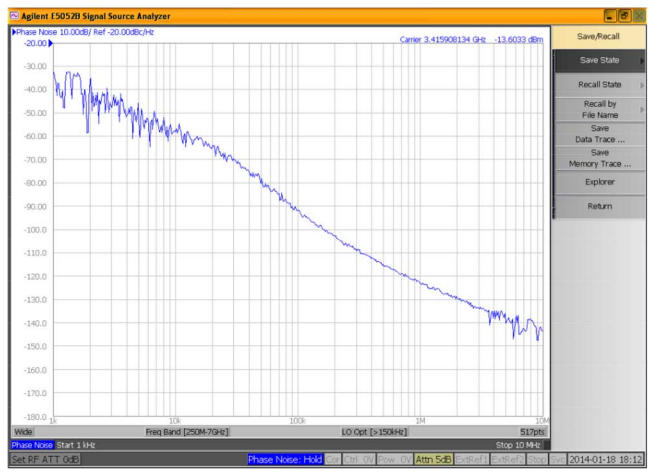

Fig. 12. Measured phase noise spectrum of the free-running DCO.

Fig. 11 shows a typical measured phase noise spectrum, the corresponding phase noise spectrum predicted by the theoretical results presented in [41], and the GSM phase noise mask for an FDC-PLL output frequency of about 3.446 GHz. The predicted phase noise spectrum was obtained by applying the theoretical transfer function that the FDC-PLL imposes on the DCO's phase noise to a piecewise approximation of the measured free-running DCO phase noise spectrum shown in Fig. 12 (measured with the digital inputs to the DCO held constant). As indicated in Fig. 11 the measured and predicted phase noise spectra are in agreement, which also confirms the expected result that the DCO's phase noise is the dominant contributor to the FDC-PLL's phase noise at all frequency offsets. As indicated in Table II, the measured results exemplified by the data shown in Fig. 11 indicate that the FDC-PLL IC achieves state-of-the-art out-of-band phase noise performance.

The DCO's low-frequency noise is higher than predicted by circuit simulations, which caused the in-band phase noise of the FDC-PLL IC to be higher than expected. The $-1/f^3$ slope visible at frequencies below 30 kHz in the measured DCO phase noise spectrum shown in Fig. 12 indicates that $1/f$ noise in the DCO is the culprit [46]. As described above, the predicted FDC-PLL phase noise curve shown in Fig. 11 is a function of the measured phase noise of the DCO and no other sources of noise, yet it closely follows the FDC-PLL's measured phase noise, both within and outside of the FDC-PLL's bandwidth. This implies that the higher-than-expected in-band FDC-PLL phase noise is caused by the DCO.

Fig. 13 shows measured and predicted phase noise spectra for the FDC-PLL configured as a Type-I PLL and a Type-II PLL. Normally, the behavior of the FDC-PLL is analogous to a Type-II $\Delta\Sigma$-PLL. However, when the loop filter's integral path is disabled by setting K_I to zero in (1), the behavior of the FDC-PLL becomes analogous to a Type-I $\Delta\Sigma$-PLL. In particular, as with a $\Delta\Sigma$-PLL, the FDC-PLL's phase noise transfer function between the DCO and the FDC-PLL output has two zero-frequency zeros when configured in Type-II mode, but only one zero-frequency zero when configured in

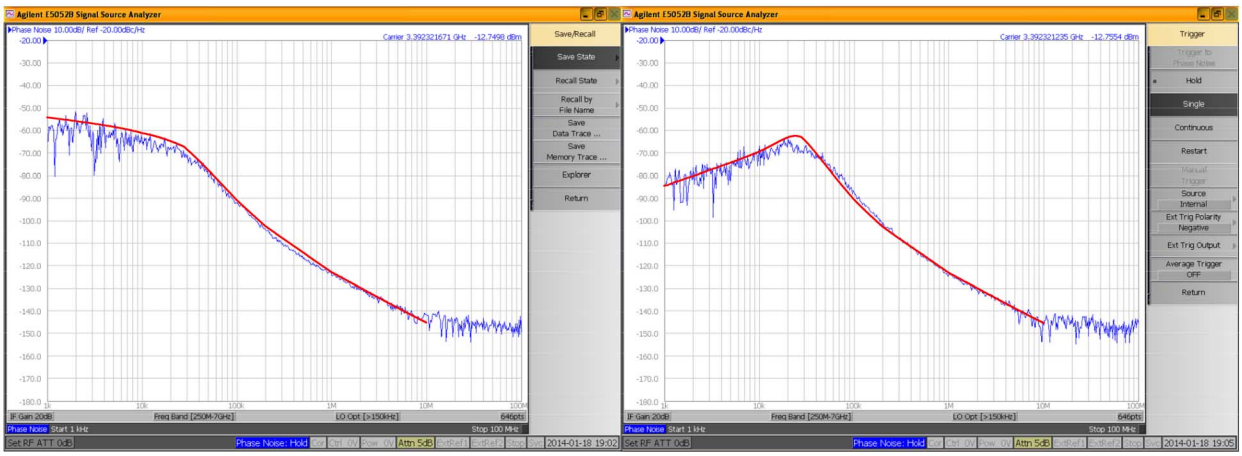

Fig. 13. Measured and theoretically predicted output phase noise spectra of the FDC-PLL configured in Type-I mode (left) and Type-II mode (right).

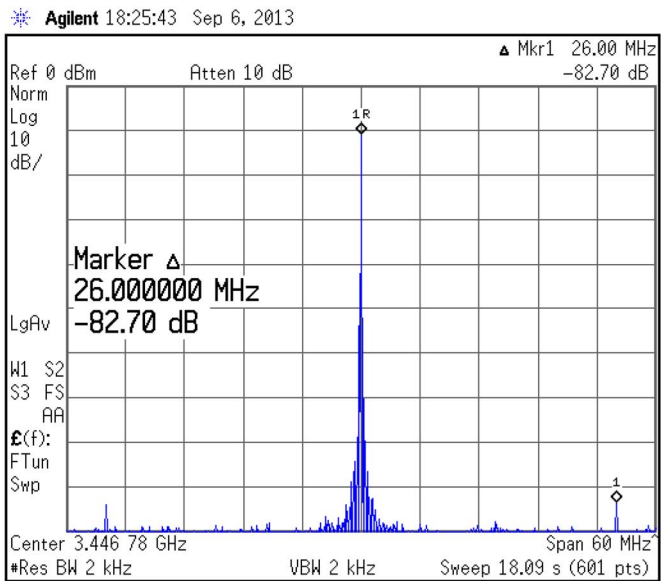

Fig. 14. Representative measured FDC-PLL output spectrum.

Type-I mode. The phase noise curves shown in Fig. 13 experimentally demonstrate these findings. The -10 dB/decade and $+10$ dB/decade slopes of the in-band portions of the phase noise spectra from the FDC-PLL configured in Type-I and Type-II modes, respectively, are the result of the -30 dB/decade slope of the DCO's phase noise below 30 kHz. This further supports the conclusion that the dominant contributor to the FDC-PLL's in-band phase noise is $1/f$ noise in the DCO. As with the results shown in Fig. 11, the predicted phase noise curves were generated by applying the theoretical transfer functions that the FDC-PLL imposes on the DCO's phase noise to a piecewise approximation of the measured free-running DCO phase noise spectrum, and they are in agreement with the measured FDC-PLL phase noise spectra in both cases.

Fig. 14 shows a representative measured FDC-PLL output spectrum. As indicated in the figure, the measured reference spur power is lower than -82 dBc, and this was found to be the case for all output frequencies tested.

Fractional spur powers were systematically measured at 100 different values of the fractional frequency word, α, between -0.5 and 0.5. Fig. 15 is a plot of the power of the largest fractional spur found for each such measurement versus the corresponding FDC-PLL frequency offset. As in a conventional $\Delta\Sigma$-PLL, the fractional spurs are largest inside the loop bandwidth and decrease with frequency outside the loop bandwidth, eventually dropping below the spectrum analyzer's measurement floor of -88 dBc. Inside the loop bandwidth, the measured fractional spurs powers range between -51 dBc and -43 dBc. While this in-band fractional spur performance is comparable to that reported for many published $\Delta\Sigma$-PLLs and TDC-PLLs, it is below that of a few of the best comparable TDC-PLLs as indicated in Table II and it is well below the best $\Delta\Sigma$-PLL in-band factional spur performance reported to date [39]. The FDC-PLL's fractional spurs had been expected to be lower than -60 dBc, but a mistake in the $\Delta\Sigma$ FDC's charge pump design reduced the charge pump output impedance to less than 25 kΩ, which behavioral simulations indicate is the cause of the discrepancy between expected and measured in-band fractional spur power.

Table II presents the FDC-PLL IC's measured performance along with that of comparable previously published state-of-the-art TDC-PLLs. The data show that the FDC-PLL IC achieves state-of-the-art out-of-band phase noise performance, occupies less circuit area than all of the comparable TDC-PLLs except for that presented in [20], and has best-of-class power consumption.

Appendix

This appendix presents a derivation of (9), the relative error of the capacitance step of the unit FCE shown in Fig. 7(a).

Let C_{tl}, C_{tr}, C_{bl}, and C_{br} be the top-left, top-right, bottom-left, and bottom-right capacitors in the FCE of Fig. 7(a). The ideal values of these capacitors in the absence of mismatches are

$$C_{tl} = C_{br} = C_F, \text{ and } C_{tr} = C_{bl} = C_F + \delta_F \qquad (10)$$

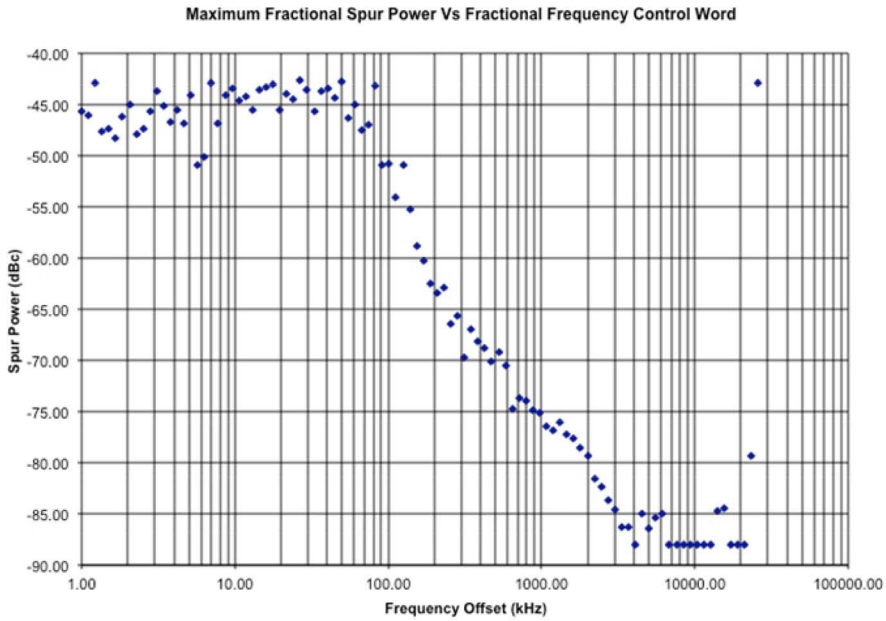

Fig. 15. Power levels of the largest measured fractional spurs for 100 logarithmically spaced frequency offsets between 0 and f_{ref}.

The capacitance of the FCE as seen across the inductor depends on whether the switch is open or closed. The difference in capacitance between these two cases is

$$C_{\delta F} = \frac{(C_{tl}+C_{bl})(C_{tr}+C_{br})}{C_{tl}+C_{bl}+C_{tr}+C_{br}} - \left[\frac{C_{tl}C_{tr}}{C_{tl}+C_{tr}} + \frac{C_{bl}C_{br}}{C_{bl}+C_{br}}\right] \tag{11}$$

Substituting (10) into (11) gives (8).

Taking partial derivatives of (11) with respect C_{tl}, C_{tr}, C_{bl}, and C_{br} and substituting (10) into the results gives

$$\frac{\partial C_{\delta F}}{\partial C_{tl}} = \frac{\partial C_{\delta F}}{\partial C_{br}} = \frac{1}{4} - \frac{(C_F+\delta_F)^2}{(2C_F+\delta_F)^2} \tag{12}$$

and

$$\frac{\partial C_{\delta F}}{\partial C_{tr}} = \frac{\partial C_{\delta F}}{\partial C_{bl}} = \frac{1}{4} - \frac{C_F^2}{(2C_F+\delta_F)^2} \tag{13}$$

Suppose that

$$C_F \gg \delta_F \tag{14}$$

and that mismatches incurred during IC fabrication cause the four FCE capacitors to deviate from their ideal values by zero-mean, uncorrelated errors with variance σ_F^2. It follows that the variance of $C_{\delta F}$ is given by

$$\sigma_{\delta F}^2 \cong \left[\left(\frac{\partial C_{\delta F}}{\partial C_{tl}}\right)^2 + \left(\frac{\partial C_{\delta F}}{\partial C_{br}}\right)^2 + \left(\frac{\partial C_{\delta F}}{\partial C_{tr}}\right)^2 + \left(\frac{\partial C_{\delta F}}{\partial C_{bl}}\right)^2\right]\sigma_F^2 \tag{15}$$

Substituting (12) and (13) into (15) and applying (14) gives

$$\sigma_{\delta F} \cong \frac{\delta_F}{2C_F}\sigma_F \tag{16}$$

The relative error of the FCE capacitance step can therefore be written as

$$\frac{\sigma_{\delta F}}{C_{\delta F}} \cong \frac{1}{\sqrt{C_{\delta F}}}\left[\frac{\delta_F}{2\sqrt{C_{\delta F}}}\left(\frac{\sigma_F}{C_F}\right)\right] \tag{17}$$

It follows from (8) and (14) that

$$\frac{1}{\sqrt{C_{\delta F}}} \cong \frac{2\sqrt{C_F}}{\delta_F} \tag{18}$$

Combining (17) and (18) gives (9).

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REFERENCES

[1] B. Miller and B. Conley, "A multiple modulator fractional divider," in *Proc. IEEE Symp. Frequency Control*, 1990, vol. 44, pp. 559–568.
[2] B. Miller and B. Conley, "A multiple modulator fractional divider," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 3, pp. 578–583, Jun. 1991.
[3] T. A. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.
[4] R. Best, *Phase-Locked Loops: Design, Simulation, Applications*, 6th ed. New York, NY, USA: McGraw-Hill, 2007.
[5] R. B. Staszewski, K. Muhammad, and D. Leipold *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.
[6] R. B. Staszewski, J. Wallberg, and S. Rezeq *et al.*, "All-digital PLL and GSM/EDGE transmitter in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 316–317.
[7] R. B. Staszewski, J. Wallberg, and S. Rezeq *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[8] K. Muhammad, H. Yo-Chuol, and T. L. Mayhugh *et al.*, "The first fully integrated quad-band GSM/GPRS receiver in a 90-nm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, Aug. 2006.

[9] R. Tonietto, E. Zuffetti, R. Castello, and I. Bietti, "A 3 MHz bandwidth low noise RF all digital PLL with 12 ps resolution time-to-digital converter," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2006, pp. 150–153.

[10] C. Weltin-Wu, E. Temporiti, D. Baldi, and F. Svelto, "A 3 GHz fractional-N all-digital PLL with precise time-to-digital converter calibration and mismatch correction," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 344–345.

[11] H. H. Chang, P.-Y. Wang, J.-H. C. Zhan, and H. Bing-Yu, "A fractional spur-free ADPLL with loop-gain calibration and phase-noise cancellation for GSM/GPRS/EDGE," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, vol. 606, pp. 200–201.

[12] M. Lee, M. E. Heidari, and A. A. Abidi, "A low-noise wideband digital phase-locked loop based on a coarse-fine time-to-digital converter with subpicosecond resolution," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2808–2816, Oct. 2009.

[13] V. Kratyuk, P. K. Hanumolu, K. Ok, U. Moon, and K. Mayaram, "A digital PLL with a stochastic time-to-digital converter," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, no. 8, pp. 1612–1621, Aug. 2009.

[14] M. S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800 MHz fractional-N digital PLL with embedded TDC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2819–2827, Dec. 2010.

[15] M. Zanuso, S. Levantino, C. Samori, and A. Lacaita, "A 3 MHz-BW 3.6 GHz digital fractional-N PLL with sub-gate-delay TDC, phase-interpolation divider, digital mismatch cancellation," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 476–477.

[16] J. Borremans, K. Vengattaramane, V. Giannini, B. Debaillie, W. V. Thillo, and J. Craninckx, "A 86 MHz-to-12 GHz digital-intensive phase-modulated PLL for software-defined radios, using a 6 fJ/Step TDC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2116–2129, Oct. 2010.

[17] S. K. Lee, Y. H. Seo, Y. Suh, H. J. Park, and J. Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 482–483.

[18] T. Tokairin, M. Okada, M. Kitsunezuka, M. Tadashi, and M. Fukaishi, "A 2.1-to-2.8-GHz low-phase-noise all-digital frequency synthesizer with a time-windowed time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2582–2590, Dec. 2010.

[19] K. Waheed, K. M. Sheba, R. B. Staszewski, F. Dulger, and S. D. Vamvakos, "Spurious free time-to-digital conversion in an ADPLL using short dithering sequences," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2010, pp. 1–4.

[20] E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto, "A 3.5 GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2723–2736, Dec. 2010.

[21] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9-to-4.0 GHz fractional-N digital PLL with bang-bang phase detector and 560 fs rms integrated jitter at 4.5 mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[22] G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 20Mb/s phase modulator based on a 3.6GHz digital PLL with -36 dB EVM at 5 mW power," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 342–343.

[23] J. Chen, L. Rong, F. Jonsson, G. Yang, and L.-R. Zheng, "The design of all-digital polar transmitter based on ADPLL and phase synchronized $\Delta\Sigma$ modulator," *IEEE J. Solid- State Circuits*, vol. 47, no. 5, pp. 1154–1164, May 2012.

[24] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, and R. Castello, "A Dither-less all digital PLL for cellular transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1908–1920, Aug. 2012.

[25] K. Takinami, R. Strandberg, P. C. P. Liang, G. L. G. de Mercey, T. Wong, and M. Hassibi, "A rotary-traveling-wave-oscillator-based all-digital PLL with a 32-phase embedded phase-to-digital converter in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 100–102.

[26] K. Euda, T. Uozumi, R. Endo, T. Nakamura, T. Heima, and H. Sato, "A digital PLL with two-step closed-locking for multi-mode/multi-band SAW-less transmitter," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2012, pp. 1–4.

[27] B. Shen, G. Unruh, M. Lugthart, C. H. Lee, and M. Chambers, "An 8.5 mW, 0.07 mm^2 ADPLL in 28 nm CMOS with sub-ps resolution TDC and $<$230 fs RMS Jitter," in *Symp. VLSI Circuits Dig.*, 2013, pp. C192–C193.

[28] C. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise, wide-BW 3.6 GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 340–341.

[29] D.-W. Jee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 2 GHz fractional-N digital PLL with 1 b noise shaping TDC," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 875–883, Apr. 2012.

[30] C.-W. Yao and A. L. Willson, "A 2.8–3.2-GHz fractional-N digital PLL with ADC-assisted TDC and inductively coupled fine-tuning DCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 698–710, Mar. 2013.

[31] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.

[32] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700 kHz bandwidth $\Sigma\Delta$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.

[33] S. E. Meninger and M. H. Perrott, "A 1 MHz bandwidth 3.6 GHz 0.18 μm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 966–980, Apr. 2006.

[34] M. Gupta and B. S. Song, "A 1.8 GHz spur cancelled fractional-N frequency synthesizer with LMS based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2842–2851, Dec. 2006.

[35] B. Zhang, P. E. Allen, and J. M. Huard, "A fast switching PLL frequency synthesizer with an on-chip passive discrete-time loop filter in 0.25- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 855–865, Jun. 2003.

[36] C. Park, O. Kim, and B. Kim, "A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 777–783, May 2001.

[37] Y.-C. Yang, S.-A. Yu, Y.-H. Liu, T. Wang, and S.-S. Lu, "A quantization noise suppression technique for $\Delta\Sigma$ fractional-N frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2500–2511, Nov. 2006.

[38] B. De Muer and M. S. J. Steyaert, "A CMOS monolithic $\Delta\Sigma$-controlled fractional-N frequency synthesizer for DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 835–844, Jul. 2002.

[39] K. Wang, A. Swaminathan, and I. Galton, "Spurious-tone suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2008.

[40] H. Hedayati, W. Khalil, and B. Bakkaloglu, "A 1 MHz bandwidth, 6 GHz 0.18 μm CMOS Type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications," *IEEE J. Solid- State Circuits*, vol. 44, no. 12, pp. 3244–3252, Dec. 2009.

[41] C. Venerus and I. Galton, "Delta-sigma FDC based fractional-N PLLs," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 5, pp. 1274–1285, May 2013.

[42] W. T. Bax and M. A. Copeland, "A GMSK modulator using a $\Delta\Sigma$ frequency discriminator-based synthesizer," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1218–1227, Aug. 2001.

[43] M. A. Ferriss and M. P. Flynn, "A 14 mW fractional-N PLL modulator with a digital phase detector and frequency switching scheme," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2464–2471, Nov. 2008.

[44] L. Li, M. P. Flynn, and M. A. Ferriss, "A 5.8 GHz digital Arbitrary phase-setting type II PLL in 65 nm CMOS with 2.25 ° resolution," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2012, pp. 317–320.

[45] M. Talegaonkar *et al.*, "A 4.4–5.4 GHz digital fractional-N PLL using $\Delta\Sigma$ frequency-to-digital converter," in *Symp. VLSI Circuits Dig.*, 2014.

[46] F. Gardner, *Phaselock Techniques*, 3rd ed. New York, NY, USA: Wiley, 2005.

[47] I. Galton and G. Zimmerman, "Combined RF phase extraction and digitization," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, 1993, vol. 2, pp. 1104–1107.

[48] R. D. Beards and M. A. Copeland, "An oversampling Delta-Sigma frequency discriminator," *IEEE Trans. Circuits Syst. II: Analog Digit. Process.*, vol. 41, no. 1, pp. 26–32, Jan. 1994.

[49] I. Galton, "Analog-input digital phase-locked loops for precise frequency and phase demodulation," *IEEE Trans. Circuits Syst. II: Analog Digit. Process.*, vol. 42, no. 10, pp. 621–630, Nov. 1995.

[50] I. Galton, W. Huff, P. Carbone, and E. Siragusa, "A delta-sigma PLL for 14b 50 kSample/s frequency-to-digital conversion of a 10 MHz FM signal," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2042–2053, Dec. 1998.

[51] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. New York, NY, USA: Wiley, 2005.

[52] I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Trans. Inf. Theory*, vol. 40, no. 3, pp. 848–859, May 1994.

[53] S. Pamarti, J. Welz, and I. Galton, "Statistics of the quantization noise in 1-bit dithered single-quantizer digital delta-sigma modulators," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 3, pp. 492–503, Mar. 2007.

[54] S. Pamarti and I. Galton, "LSB dithering in MASH Delta-Sigma D/A converters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 4, pp. 779–790, Apr. 2007.

[55] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009.

[56] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators—Analysis, design, measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.

[57] R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold, "A first RF digitally-controlled oscillator for mobile phones," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, 2005, pp. 119–122.

[58] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[59] L. Fanori, A. Liscidini, and R. Castello, "Capacitive degeneration in LC-tank oscillator for DCO fine-frequency tuning," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2737–2745, Dec. 2010.

[60] C.-M. Hung, R. B. Staszewski, N. Barton, L. Meng-Chang, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.

[61] G. Taylor and I. Galton, "A reconfigurable mostly-digital Delta-Sigma ADC with a worst-case FOM of 160 dB," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013.

[62] M. J. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[63] A. Hasting, *The Art of Analog Layout*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice Hall, 2005.

[64] K. L. Chan, N. Rakuljic, and I. Galton, "Segmented dynamic element matching for high-resolution digital-to-analog conversion," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 55, pp. 3383–3392, Dec. 2008.

[65] J. Welz, I. Galton, and E. Fogleman, "Simplified logic for first-order and second-order mismatch-shaping digital-to-analog converters," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 48, no. 11, pp. 1014–1028, Nov. 2001.

[66] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 44, no. 10, pp. 808–817, Nov. 1997.

[67] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.

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