25.1 A Highly-Digital Frequency Synthesizer Using Ring-Oscillator Frequency-to-Digital Conversion and Noise Cancellation

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Digital fractional-*N* PLLs are increasingly used in place of analog fractional-*N* PLLs as frequency synthesizers in wireless applications, because they avoid large analog loop filters and can tolerate device leakage and low supply voltages, which makes them better-suited to highly-scaled CMOS technology [1-6]. However, the phase noise and spurious tone performance of previously published digital PLLs is inferior to that of the best analog PLLs. This is because all fractional-*N* PLLs introduce quantization noise, and in prior digital PLLs this noise has higher power or spurious tones than in comparable analog PLLs. Digital PLLs based on ΔΣ frequency-to-digital conversion (FDC-PLLs) offer a potential solution to this problem in that their quantization noise ideally is equivalent to that of analog PLLs, but prior FDC-PLLs incorporate charge pumps and ADCs that have so far limited their performance and minimum supply voltages [7,8]. This paper presents an FDC-PLL that avoids these limitations by implementing the functionality of a charge pump and ADC with a simple dual-mode ring oscillator (DMRO) and digital logic. Also demonstrated is a new quantization noise cancellation (QNC) technique that relaxes the fundamental bandwidth versus quantization noise tradeoff inherent to most fractional-*N* PLLs. The new techniques enable state-of-the-art spurious tone performance and very low phase noise with a lower power dissipation and supply voltage than previously published state-of-the-art PLLs in the same class shown in Fig. 25.1.6.

The FDC-PLL output frequency is $f_{PLL}=(N+\alpha)f_{ref}$, where N is an integer, α is a fractional value between –½ and ½, and f_{ref} = 26MHz is the reference frequency. Its core (Figs. 25.1.1 and 25.1.2) consists of a ΔΣ FDC, a digital loop controller (DLC), and a digitally controlled oscillator (DCO). The ΔΣ FDC's DMRO (Fig. 25.1.3) switches between two frequencies, f_{low} and f_{high}, depending on the state of the top PFD output, $u(t)$. An analysis shows that for the correct choice of f_{low} and f_{high} the ΔΣ FDC is exactly equivalent to the 2nd-order ΔΣ modulator shown in Fig. 25.1.1, where $e_{PLL}[n]$ is the average frequency error of the PLL output over the nth reference period. As such, the ΔΣ FDC has the self-dithering advantage of a 2nd-order ΔΣ modulator [8]. In contrast, previously published ring-oscillator-based time-to-digital converters are only equivalent to 1st-order ΔΣ modulators, which are notorious for having large spurious tones and input-dependent quantization noise [2].

The 1st and 2nd accumulators in the FDC-PLL's equivalent 2nd-order ΔΣ modulator derive from the frequency-to-phase integrating behaviors of the multi-modulus divider and DMRO, respectively, and both ΔΣ modulator feedback loops derive from the ΔΣ FDC's $2-z^{-1}$ local feedback. The divider and $2-z^{-1}$ block are digital, so the ΔΣ modulator's first accumulator and outer feedback path are numerically ideal. The ΔΣ modulator's second accumulator is not inherently ideal, but it is surprisingly insensitive to non-ideal DMRO behavior. This can be understood by an analogy to charge pumps in analog PLLs. It is well known that non-ideal charge pump switching transients do not degrade analog PLL performance provided each current source has time to settle whenever it is turned on or off, and provided the rising and falling transient shapes are independent of the times at which the current source is turned on and off, respectively. For the same reasons, non-ideal DMRO frequency switching transients do not degrade the FDC-PLL performance provided the high and low durations of $u(t)$ each reference period are long enough for the transients to settle out, and the rising and falling transient shapes are independent of the times at which $u(t)$ goes high and low, respectively. Simulations indicate that these conditions occur to a high degree of accuracy provided the average high-duration of $u(t)$ per reference period is within a relatively wide range of acceptable values.

Ideally, $f_{high} - f_{low} = f_{PLL}$, but deviations from this ideal only change the gain of the second ΔΣ modulator accumulator, so the PLL performance is not highly sensitive to such deviations. The value of f_{low} sets the average high-duration of $u(t)$ each reference period so its value is not critical. Both f_{low} and f_{high} are set via serial port interface (SPI) control to values within 0.4 to 3.4GHz and 1.8 to 5.1GHz, respectively, with resolutions of approximately 5% whenever the PLL output frequency is changed.

If the average DMRO frequency were incommensurate with the reference frequency, its presence would likely cause fractional spurs. However, it can be verified that the ΔΣ FDC naturally locks the DMRO to an average frequency of Mf_{ref} where M is a positive integer in the ring phase calculator (Fig. 25.1.2) between 40 and 80 set via the SPI. Therefore, any spurious tones from the DMRO are indistinguishable from reference spurs, which, as indicated in Fig. 25.1.6, are very low.

The $y[n]$ output of the ring phase calculator (Fig. 25.1.1) is a 5-level 26MHz sequence with a mean of $-\alpha$ when the PLL is locked. The digital logic that generates $y[n]$ (Fig. 25.1.2) is a practical means of implementing the equivalent of counting DMRO cycles with an infinite-range counter, subtracting nM from the counter output each reference period where n = 0, 1, 2, …, and clipping the counter value as necessary (which only happens before the PLL locks) to keep $y[n]$ in the range {–2,–1,…, 2}. It can be verified that this exactly implements the behavior of the charge pump and 5-level ADC in the FDC-PLL described in [8].

The goal of QNC is to cancel most of the quantization noise in $y[n]$ prior to the loop filter so the PLL bandwidth can be increased significantly without increasing the PLL phase noise. To this end the phase decoder in Fig. 25.1.2 uses the 13 DMRO inverter outputs to obtain $-\hat{e}[n]$, which is an estimate of the DMRO's quantization error quantized to 1/26th of a DMRO cycle, i.e., 1/26th of the quantization step-size of $y[n]$. The DLC logic does the equivalent of adding $-\hat{e}[n]+2\hat{e}[n-1]-\hat{e}[n-2]$ to $y[n]$, which, given the above-mentioned ΔΣ modulator equivalence (Fig. 25.1.1), cancels most of its quantization noise.

The multi-modulus divider generates a $\frac{1}{8}f_{PLL}$ clock in addition to the output shown in Fig. 25.1.1. All the digital I/O and switching is retimed to this fast clock, to minimize reference spur coupling. Extensive clock gating minimizes the associated power dissipation. The DLC loop filter consists of a fixed-point multiplier, four IIR filters and a PI controller, configurable for type-I or II operation with a 1-to-300kHz bandwidth. The 8 LSBs of the 14b DLC output drive a 2nd-order digital ΔΣ modulator clocked at $\frac{1}{8}f_{PLL}$; the ΔΣ modulated LSBs in conjunction with the 6 MSBs drive the fine control port of the LC-DCO, whose topology is similar to that presented in [1].

Figures 25.1.4 to 25.1.6 present measured results for f_{PLL}≅3.5GHz and a 140kHz bandwidth. Figure 25.1.4 shows the measured phase noise with QNC enabled and disabled. QNC relies on the ΔΣ modulator equivalence described above, so the significant reduction in phase noise that occurs when QNC is enabled indicates that the ΔΣ FDC works as expected. Figure 25.1.5 shows a plot of the largest measured fractional spur over an extensive sweep of α. The fractional spurs are largest within the loop bandwidth, with a worst-case of –60dBc, and drop quickly out of band. The measured performance is summarized in Fig. 25.1.6 along with that of the best comparable PLLs. As indicated, the FDC-PLL has state-of-the-art spurious tone performance, excellent phase noise performance, and the lowest supply voltage and power dissipation among those shown in the table. This is enabled by the FDC-PLL's unique combination of a highly digital architecture and quantization noise equivalent to that of an analog PLL.

Acknowledgements:
The authors are grateful to STMicroelectronics for IC fabrication and fruitful discussions, Integrand Software for EMX access, NSF (Award 1343389) and Analog Devices for financial support, and Chris Mangelsdorf for helpful advice.

References:

[1] R. B. Staszewski, et al., "All-Digital PLL and GSM/EDGE Transmitter in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 316-317, Feb. 2005.

[2] C. Hsu, et. al., "A Low-Noise, Wide-BW 3.6GHz Digital ΔΣ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *ISSCC Dig. Tech. Papers*, pp. 340-341, Feb. 2008.

[3] H. H. Chang, et. al., "A Fractional Spur-Free ADPLL with Loop-Gain Calibration and Phase-Noise Cancellation for GSM/GPRS/EDGE," *ISSCC Dig. Tech. Papers*, pp. 200-201, Feb. 2008.

[4] C. Weltin-Wu, et. al., "A 3.5GHz Wideband ADPLL With Fractional Spur Suppression Through TDC Dithering and Feedforward Compensation," *ISSCC Dig. Tech. Papers*, pp. 468-469, Feb. 2010.

[5] K. Takinami, et. al., "A Rotary-Traveling-Wave-Oscillator-Based All-Digital PLL with a 32-Phase Embedded Phase-to-Digital Converter in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 100-101, Feb. 2011.

[6] L. Vercesi, et. al., "A Dither-Less All Digital PLL for Cellular Transmitters," *IEEE Custom Integrated Circuits Conf.*, pp. 1-8, Sept. 2011.

[7] W. T. Bax, M. A. Copeland, "A GMSK Modulator Using a ΔΣ Frequency Discriminator-Based Synthesizer," *IEEE J. Solid-State Circuits*, pp. 1218-1227, Aug. 2001.

[8] C. Venerus, I. Galton, "Delta-Sigma FDC Based Fractional-*N* PLLs," *IEEE Trans. Circuits and Systems-I*, pp. 1274-1285, May 2013.

 978-1-4799-6224-2/15/$31.00

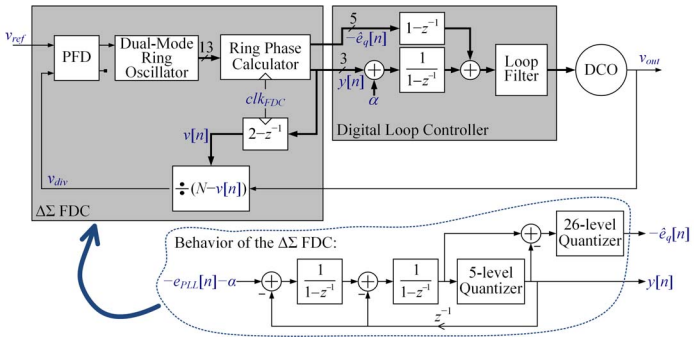

Figure 25.1.1: High-level block diagram of the FDC-PLL and equivalent signal processing behavior of the ΔΣ FDC.

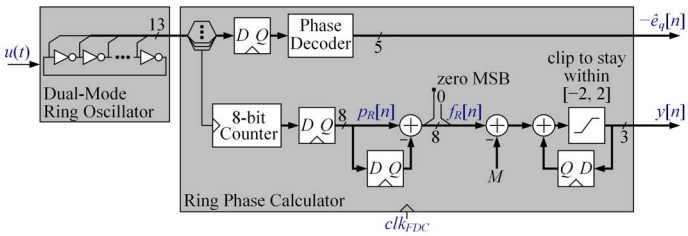

Figure 25.1.2: Functional details of the dual-mode ring oscillator (DMRO) and ring phase calculator.

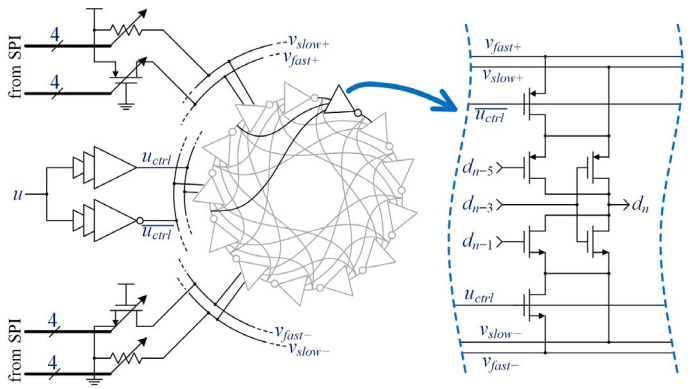

Figure 25.1.3: Circuit details of the dual-mode ring oscillator (DMRO).

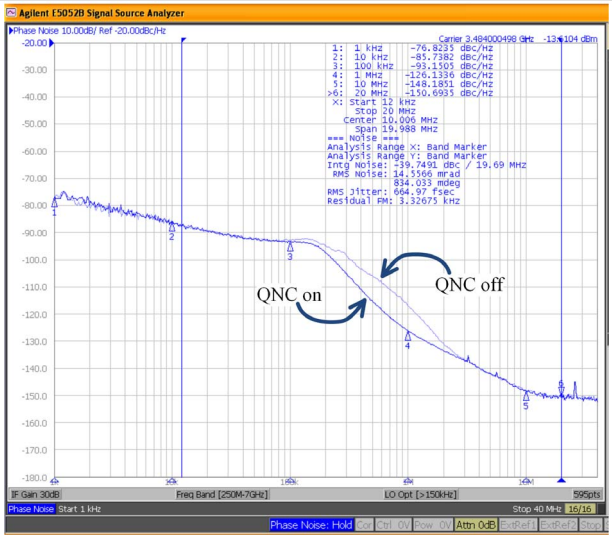

Figure 25.1.4: Measured FDC-PLL phase noise with and without quantization noise cancellation (QNC) for a bandwidth of 140kHz.

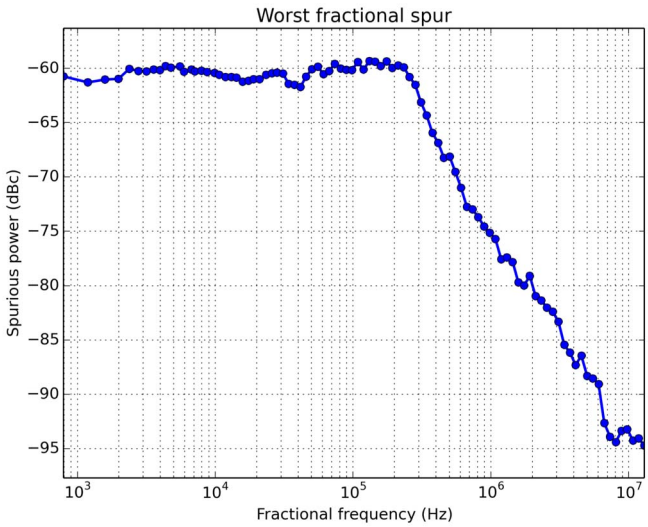

Figure 25.1.5: The largest measured fractional spurious tone as a function of the PLL's fractional frequency setting.

	[1]	[2]	[3]	[4]	[5]	[6]	This work
Technology	90 nm	130 nm	130 nm	65 nm	55 nm	65 nm	65 nm
Supply[1] (V)	1.2	1.5	Not Stated	1.2	1.5	1.5/1.2	1.0
Power Consumption[1] (mW)	Not Stated	39	>40[4]	8.7	41.6	45	15.6
Area (mm²)	Not Stated	0.95	0.86	0.44	0.7	0.6	0.35
Reference Frequency (MHz)	26	50	26	35	26	78	26
PLL Frequency (GHz)	3.6	3.7	3.6	3.5	1.8	4.0	3.5
Bandwidth (kHz)	40	500	50	3400	800	1000	140
In-band Phase Noise[2] (dBc/Hz)	-81@20kHz	-107@400kHz	-79@10kHz	-101@1MHz	-102@60kHz	-109@200kHz	-93@100kHz
Out-of-band Phase Noise[2] (dBc/Hz)	-117@1MHz[3] - -152@20MHz	- -131@3MHz -149@20MHz	-126@1MHz -136@3MHz -152@20MHz	- - -129@20MHz	- -122@3MHz -154@20MHz	- - -149@20MHz	-126@1MHz -138@3MHz -151@20MHz
In-band Fractional Spur (dBc)	Not Stated	-42	Not Stated	-58	-50	-40	-60
Reference Spur (dBc)	-92	-65	-84	-61	Not Stated	-56	-81

(1) Power and supply measurements are for core PLL circuitry, excluding RF output buffers
(2) Phase noise is normalized to a 3.5GHz PLL frequency
(3) Calculated by extending -20dB/decade phase noise slope from 400kHz measurement to 1MHz
(4) PLL draws 40mA from an unknown supply voltage in 130nm CMOS

Figure 25.1.6: Performance summary and comparison table.

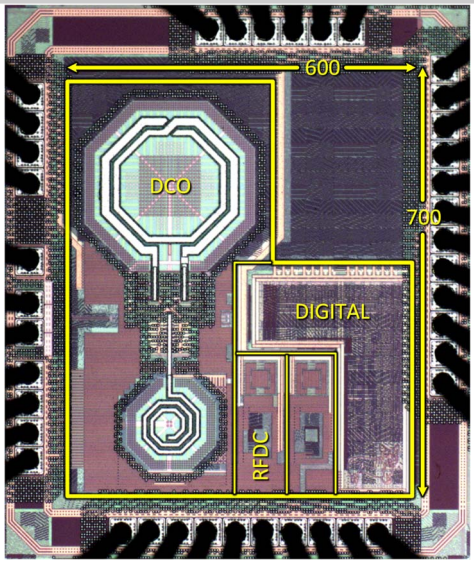

Figure 25.1.7: Die micrograph. Note Corgi in lower-right-hand corner.

978-1-4799-6224-2/15/$31.00