Suppression of Quantization-Induced Convergence Error in Pipelined ADCs With Harmonic Distortion Correction

Nevena Rakuljic, *Member, IEEE*, and Ian Galton, *Fellow, IEEE*

***Abstract*—Harmonic Distortion Correction (HDC) is one of two published digital background calibration techniques that compensate for residue amplifier nonlinearity in pipelined ADCs. The techniques make it possible to reduce the gains and bandwidths, and therefore the power dissipations, of the op-amps that make up the residue amplifiers without sacrificing pipelined ADC accuracy. Unfortunately, the previously published techniques fail to operate properly when they measure residue amplifier distortion for certain pipelined ADC input signals, most notably input signals with small peak-to-peak variations about certain constant values. This paper identifies the cause of the problem, quantifies its effects, and provides an all-digital solution applicable to the HDC technique.**

***Index Terms*—Digital background calibration, harmonic distortion correction, pipelined analog-to-digital conversion, residue amplifier nonlinearity.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) are widely used in applications that require greater accuracy than can be achieved practically by flash ADCs, and greater signal bandwidth than can be achieved practically by oversampling or successive approximation ADCs. With present IC technology, they are most commonly used in applications that require greater than 50 dB of signal to noise and distortion ratio (SNDR) and greater than 50 MHz of signal bandwidth.

The residue amplifiers in the first few stages of a pipelined ADC must have high linearity for the ADC to achieve a high SNDR. In a conventional pipelined ADC, this necessitates op-amps with high open-loop gains, high bandwidths, and relatively low output swings. Consequently, the op-amps tend to dominate the overall power dissipation in conventional pipelined ADCs.

Recently, digital background calibration techniques have been proposed that make it possible to reduce the performance and, hence, the power dissipation of the op-amps without sacrificing pipelined ADC accuracy [1]–[5]. The techniques use digital correlation algorithms to measure the residue amplifier distortion coefficients during normal ADC operation, and they use the measured coefficient values to digitally cancel much of the residue amplifier distortion. This allows higher-distortion op-amps to be tolerated without significantly degrading the overall pipelined ADC accuracy. The calibration circuitry is mostly digital and tends to dissipate relatively little power, so the net reduction in pipelined ADC power dissipation offered by the techniques can be significant.

Unfortunately, all of the previously published digital background calibration techniques fail to measure the residue amplifier distortion coefficients properly for certain pipelined ADC input signals. As explained in [4] and [5], the most robust of the techniques in this respect is the Harmonic Distortion Correction (HDC) technique. Nevertheless, for certain input signals, most notably those with small peak-to-peak variations about certain constant values, it too fails to accurately measure the residue amplifier distortion coefficients. Although it operates properly for the majority of pipelined ADC input signals, its failure to work properly even for a small class of input signals presents a problem in practice.

This paper identifies and quantifies the failure mechanism, and proposes a simple all-digital modification of the HDC technique that solves the problem. As explained in the paper, the problem arises because the small amount of quantization error introduced by the pipelined ADC corrupts the coefficient measurement process under certain conditions. The problem is subtle because the corruption occurs even when the variance of the quantization noise is much smaller than the dominant error sources in the pipelined ADC. Although the paper describes the problem in the context of the HDC technique, the problem also affects the other previously published digital calibration techniques, because the quantization error is always present during the coefficient measurement process regardless of the technique used.

The paper consists of three main sections. Section II reviews the HDC technique in the context of an example pipelined ADC architecture. Section III identifies and quantifies the HDC failure mechanism, and Section IV presents the proposed solution.

II. Background Information

A. Pipelined ADC and HDC Overview

Fig. 1 shows a six-stage, 14-b pipelined ADC example. The input to the pipelined ADC is a sequence of sampled analog voltages, $v_{in,1}(nT_s)$, where T_s is the sample interval. In practice each stage in a pipelined ADC contains delay elements, but

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The authors are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407 USA (e-mail: galton@ece.ucsd.edu).

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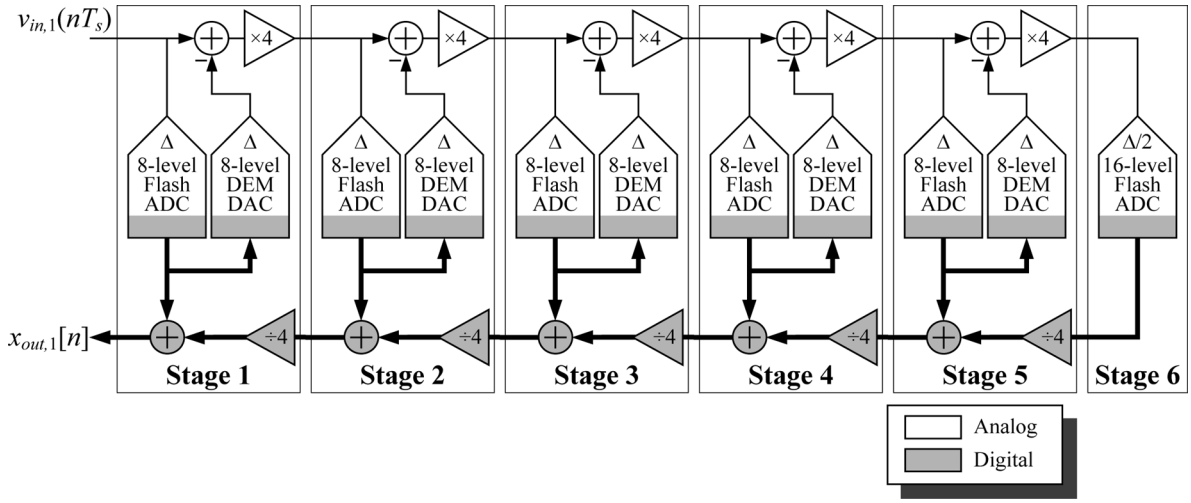

Fig. 1. Example pipelined ADC.

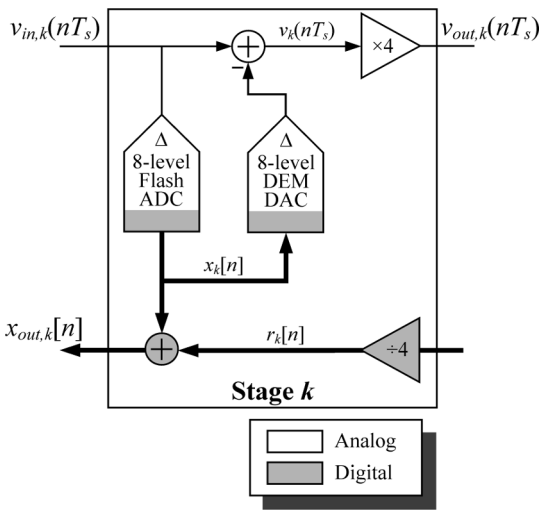

Fig. 2. The kth pipelined ADC stage, for $k = 1, \ldots, 5$, with labels that indicate variable names used throughout the paper.

the delay elements have been omitted in the pipelined ADC example of Fig. 1. This reduces the complexity of the notation presented in the paper without significantly affecting the results of the paper.

All but the last pipelined ADC stage in Fig. 1 have the form shown in Fig. 2. Each consists of an 8-level flash ADC with a nominal quantization step-size of Δ, an 8-level dynamic element matching (DEM) DAC, and a *residue amplifier*. The last stage of the pipelined ADC consists only of a 16-level flash ADC with a nominal quantization step-size of $\Delta/2$.

The output of the kth stage's flash ADC (flash ADC_k) is

$$x_k[n] = v_{in,k}\left(nT_s\right) + e_{ADC,k}[n] \tag{1}$$

where $v_{in,k}(nT_s)$ is the input sequence to flash ADC_k, and $e_{ADC,k}[n]$ is error introduced by flash ADC_k. This error is the output minus the input of flash ADC_k, with the least significant bit of the output taken to have a weight equal to the nominal quantization step-size of flash ADC_k. In the absence of non-ideal circuit behavior, $e_{ADC,k}[n]$ is just quantization error, and is bounded in magnitude by half of its nominal quantization step size.

The 8-level DAC in the kth stage (DAC_k) for $k = 1, 2, \ldots, 5$ converts $x_k[n]$ into analog format. The difference between the stage's input sequence and the DAC's output sequence, $v_k(nT_s)$, is called the stage's *residue*. It follows from (1) that in the absence of non-ideal circuit behavior the stage's residue is given by

$$v_k\left(nT_s\right) = -e_{ADC,k}[n], \tag{2}$$

and is bounded in magnitude by $\Delta/2$. Ideally, the kth stage's residue amplifier (RA_k) scales the residue linearly by a factor of 4, i.e.,

$$v_{out,k}\left(nT_s\right) = 4v_k\left(nT_s\right). \tag{3}$$

Therefore, the analog output of the kth pipeline stage is ideally bounded in magnitude by 2Δ, which is less than half the input range of the flash ADC in the subsequent pipeline stage. The extra input range, called *over-range margin*, is used to accommodate flash ADC errors that arise from non-ideal circuit behavior such as comparator offset voltages and resistor ladder component mismatches. These errors subsequently cancel in the digital path of the pipelined ADC assuming ideal circuit behavior except for flash ADC errors [6]–[8].

It follows from (1) and Fig. 2 that the digital output of the kth stage, for $k = 1, 2, \ldots, 5$, is given by

$$x_{out,k}[n] = v_{in,k}\left(nT_s\right) + e_{ADC,k}[n] + r_k[n] \tag{4}$$

where

$$r_k[n] = \frac{1}{4}\left(x_{k+1}[n] + r_{k+1}[n]\right). \tag{5}$$

is called the *digitized residue* of the kth stage. Recursively applying (1)–(5) with

$$v_{in,k+1}(nT_s) = v_{out,k}(nT_s) \tag{6}$$

indicates that the output of the pipelined ADC ideally is

$$x_{out,1}[n] = v_{in,1}\left(nT_s\right) + \frac{1}{4^5}e_{ADC,6}[n]. \tag{7}$$

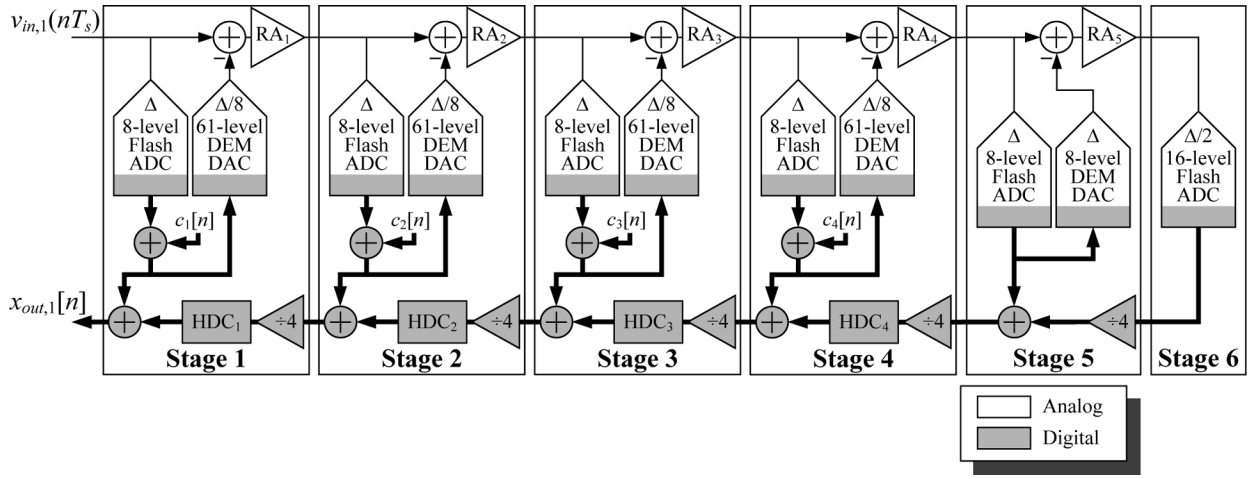

Fig. 3. The example pipelined ADC with HDC applied to the first four stages.

Therefore, in the absence of non-ideal circuit behavior the quantization error from all the flash ADCs except that in the last pipeline stage cancel, so the only quantization error that propagates to the pipelined ADC output is a scaled version of the last stage's quantization error. The pipelined ADC input range is bounded in magnitude by 4Δ and the scaled version of quantization error is bounded in magnitude by $(\Delta/4)/4^5$, so the pipelined ADC ideally performs 14-bit quantization.

Equations (2)–(7) describe the ideal pipelined ADC behavior. In practice, the output deviates from (7) because of non-ideal circuit behavior. In particular, practical residue amplifiers introduce gain error and nonlinear distortion. An often-realistic model of the kth residue amplifier that includes this non-ideal behavior is

$$v_{out,k}(nT_s) = 4\left[(1+\alpha_{1,k})\,v_k(nT_s) + \alpha_{3,k}v_k^3(nT_s)\right] \quad (8)$$

where $\alpha_{1,k}$ is a gain error coefficient, and $\alpha_{3,k}$ is a third-order nonlinear distortion coefficient [5]. If the pipelined ADC in Fig. 1 is ideal except with residue amplifiers that are well-modeled by (8), it follows from (1), (2), (4)–(7), and (8) that

$$x_{out,1}[n] = x_{out,1}[n]|_{\text{ideal}} + \underbrace{\sum_{k=1}^{5} 4^{1-k}\left[\alpha_{1,k}v_k(nT_s) + \alpha_{3,k}v_k^3(nT_s)\right]}_{\text{Distortion Terms}} \quad (9)$$

where $x_{out,1}[n]|_{\text{ideal}}$ is $x_{out,1}[n]$ as given by (7). The distortion terms in (9) are undesirable because typically they decrease both the SNDR and the spurious-free dynamic range (SFDR) of the pipelined ADC.

HDC can be applied to each stage of a pipelined ADC to digitally estimate and cancel the distortion terms [4], [5]. As indicated by (9) the distortion terms contributed by the residue amplifier in the kth pipeline stage are scaled by 4^{1-k}, so the residue amplifiers in the first few pipeline stages usually are the dominant sources of residue amplifier distortion in the pipelined ADC. Thus, in practice HDC usually is applied only to the first few pipeline stages.

Fig. 3 shows an example of the 14-b pipelined ADC with HDC applied to the first four stages and Fig. 4 shows the kth

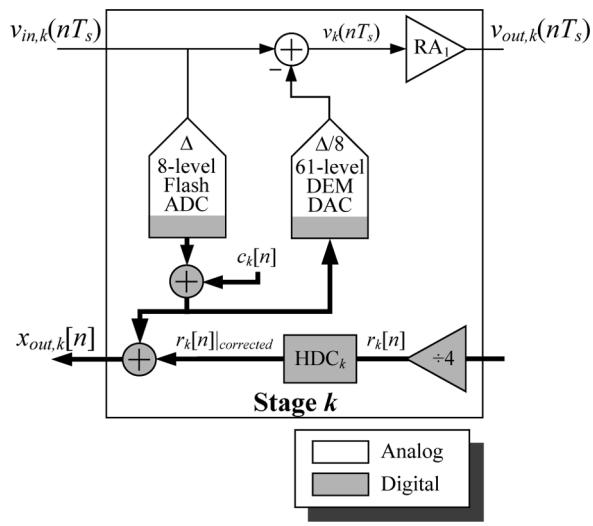

Fig. 4. The kth pipelined ADC stage with HDC for $k = 1, 2, 3, 4$, with labels that indicate variable names used throughout the paper.

of these stages in more detail. The implementation of HDC in the kth stage consists of the addition of a calibration sequence, $c_k[n]$, to the output of flash ADC_k, an increase in the resolution of DAC_k to accommodate the added sequence, and the addition of a digital logic block, labeled HDC_k in the figure. The kth stage's calibration sequence has the form

$$c_k[n] = \sum_{i=1}^{N} t_{i,k}[n] \quad (10)$$

where the $t_{i,k}[n]$ sequences are independent, 2-level, zero-mean, pseudorandom sequences that take on values of $\pm A$. In this paper $A = \Delta/16$ as in [5] and, for a reason explained shortly, $N = 4$, so DAC_k must have at least 61 output levels with a minimum step-size of $\Delta/8$ to accommodate $c_k[n]$.

The calibration sequence increases the maximum signal swing at the output of the residue amplifier, so it effectively decreases the over-range margin of the stage. Therefore, a design consideration is that A and N must be small enough that the remaining over-range margin is sufficient to accommodate the largest expected stage offset and flash ADC_k errors. In

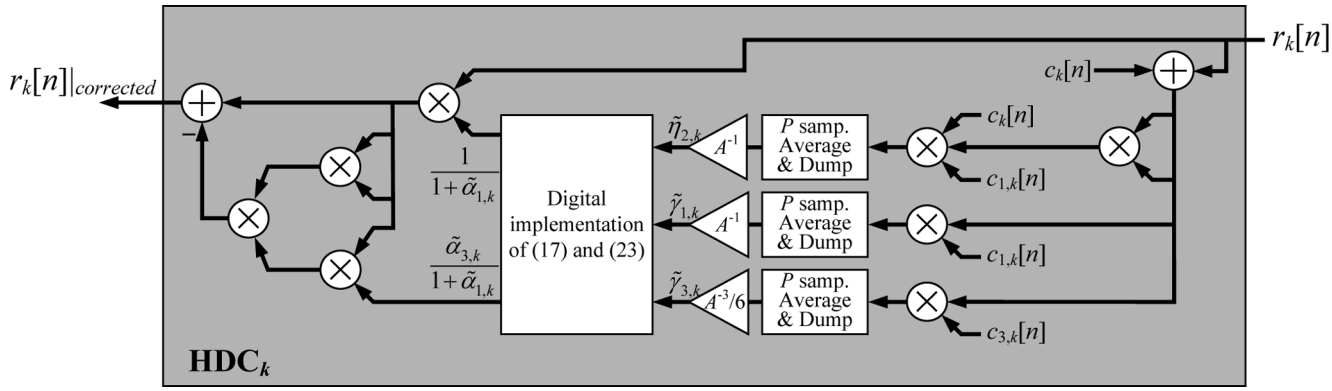

Fig. 5. Details of the HDC_k block.

the example design, half the over-range margin is used to accommodate the calibration sequence.

Ideally, each HDC_k block cancels error arising from $\alpha_{1,k}$ and $\alpha_{3,k}$ in the kth stage's residue amplifier. It follows from (2), (4), (7), and (9) that

$$r_k[n] = (1+\alpha_{1,k})\, v_k\,(nT_s) + \alpha_{3,k} v_k^3\,(nTs) + \frac{1}{4^5} e_{ADC,6}[n] + g_{k+1}\,(v_k\,(nT_s))\,, \quad (11)$$

for $k = 1, 2, 3,$ and 4, where the last term represents error caused by any non-ideal behavior of the stages subsequent to Stage k such as residue amplifier distortion in Stage 5. Therefore, the objectives of HDC applied to the kth stage can be viewed as estimating and canceling the terms proportional to $\alpha_{1,k}$ and $\alpha_{3,k}$ in (11).

It follows from (1) and Fig. 4 that

$$v_k\,(nT_s) = -e_{ADC,k}[n] - c_k[n]. \quad (12)$$

Fig. 5 with

$$c_{1,k}[n] = -\frac{t_{1,k}[n]}{A} \text{ and } c_{3,k}[n] = -\frac{t_{1,k}[n] t_{2,k}[n] t_{3,k}[n]}{A^3} \quad (13)$$

shows the details of the HDC_k block. To estimate the $\alpha_{1,k}$ and $\alpha_{3,k}$ coefficients, the HDC_k block first computes the time averages

$$\tilde{\gamma}_{1,k} = \frac{1}{A}\frac{1}{P}\sum_{n=m}^{m+P-1} (r_k[n] + c_k[n])\, c_{1,k}[n],$$
$$\tilde{\gamma}_{3,k} = \frac{1}{6A^3}\frac{1}{P}\sum_{n=m}^{m+P-1} (r_k[n] + c_k[n])\, c_{3,k}[n], \quad (14)$$

and

$$\tilde{\eta}_{2,k} = \frac{1}{A}\frac{1}{P}\sum_{n=m}^{m+P-1} (r_k[n] + c_k[n])^2\, c_k[n] c_{1,k}[n], \quad (15)$$

where m is the starting time index of the time averaging operations, and P is the number of averaged samples (e.g., $P = 2^{32}$ in [5])[1]. To the extent that the correlations of $c_{1,k}[n]$ and $c_{3,k}[n]$ with the last term (11) in can be neglected, it follows from (10)–(14), the statistical properties of the $t_{i,k}[n]$ sequences, and the Law of Large Numbers, that for $N = 4$

$$\tilde{\gamma}_{1,k} \cong \tilde{\alpha}_{1,k} + \left(10A^2 - \frac{3\tilde{\eta}_{2,k}}{(1+\tilde{\alpha}_{1,k})^2}\right)\tilde{\alpha}_{3,k}, \quad (16)$$

and

$$\tilde{\gamma}_{3,k} = \tilde{\alpha}_{3,k}, \quad (17)$$

where

$$\tilde{\alpha}_{1,k} \cong \alpha_{1,k} \quad \text{and} \quad \tilde{\alpha}_{3,k} \cong \alpha_{3,k} \quad (18)$$

to a high degree of accuracy provided P is large.

Combining (16) and (17) results in

$$\tilde{\gamma}_{1,k} \cong \tilde{\alpha}_{1,k} + \left(10A^2 - \frac{3\tilde{\eta}_{2,k}}{(1+\tilde{\alpha}_{1,k})^2}\right)\tilde{\gamma}_{3,k} \quad (19)$$

which is a cubic equation that can be solved to find $\tilde{\alpha}_{1,k}$ in terms of $\tilde{\gamma}_{1,k}$, $\tilde{\gamma}_{3,k}$ and $\tilde{\eta}_{2,k}$. A closed form solution exists, but it is complicated. An approximate but simpler solution can be obtained by viewing $\tilde{\alpha}_{1,k}$ as a function of $\tilde{\gamma}_{1,k}$, $\tilde{\gamma}_{3,k}$ and $\tilde{\eta}_{2,k}$ and using a Taylor series expansion around $\tilde{\gamma}_{3,k}$, i.e.,

$$\tilde{\alpha}_{1,k}\,(\tilde{\gamma}_{1,k}, \tilde{\gamma}_{3,k}, \tilde{\eta}_{2,k}) \cong \tilde{\alpha}_{1,k}\,(\tilde{\gamma}_{1,k}, 0, \tilde{\eta}_{2,k}) + \sum_{i=1}^{3} \frac{1}{k!}\frac{\partial^i \tilde{\alpha}_{1,k}}{\partial \tilde{\gamma}_{3,k}^i}\,(\tilde{\gamma}_{1,k}, 0, \tilde{\eta}_{2,k})\,\tilde{\gamma}_{3,k}^i \quad (20)$$

It follows from (19) that

$$\tilde{\alpha}_{1,k}\,(\tilde{\gamma}_{1,k}, 0, \tilde{\eta}_{2,k}) = \tilde{\gamma}_{1,k}. \quad (21)$$

Differentiating (19) with respect to $\tilde{\gamma}_{3,k}$ and substituting (21) into the result yields

$$\frac{\partial \tilde{\alpha}_{1,k}}{\partial \tilde{\gamma}_{3,k}}\,(\tilde{\gamma}_{1,k}, 0, \tilde{\eta}_{2,k}) = \frac{3\tilde{\eta}_{2,k}}{(1+\tilde{\gamma}_{1,k})^2} - 10A^2, \quad (22)$$

and continuing this process recursively yields the remaining two terms on the right side of (20). Substituting these results into (20) yields

$$\tilde{\alpha}_{1,k} \cong \tilde{\gamma}_{1,k} + \left(\frac{3\tilde{\eta}_{2,k}}{(1+\tilde{\gamma}_{1,k})^2} - 10A^2\right) \times \left(\tilde{\gamma}_{3,k} - \frac{6\tilde{\eta}_{2,k}}{(1+\tilde{\gamma}_{1,k})^3}\tilde{\gamma}_{3,k}^2 + \frac{63\tilde{\eta}_{2,k}^2 - 90A^2\tilde{\eta}_{2,k}(1+\tilde{\gamma}_{1,k})^2}{(1+\tilde{\gamma}_{1,k})^6}\tilde{\gamma}_{3,k}^3\right). \quad (23)$$

[1]Note that $\tilde{\eta}_{2,k}$ in (15) is different than the corresponding quantity in [4] and [5]. It can be verified that this version of $\tilde{\eta}_{2,k}$ avoids an approximation made in [4] and [5] and therefore yields slightly more accurate results than those obtained in [4] and [5].

The HDC_k block uses the estimates of $\alpha_{1,k}$ and $\alpha_{3,k}$ given by (23) and (17), respectively, to calculate the *corrected digitized residue*:

$$r_k[n]|_{corrected} = \frac{1}{1+\tilde{\alpha}_{1,k}} r_k[n] - \frac{\tilde{\alpha}_{3,k}}{(1+\tilde{\alpha}_{1,k})^4} r_k^3[n]. \quad (24)$$

It can be verified that this causes $x_{out,k}[n] \cong x_{out,k}[n]|_{\text{ideal}}$ [4].

The accuracy with which each HDC block estimates its nonlinearity coefficients depends, in part, on how well the subsequent HDC blocks have corrected the nonlinearity introduced by the residue amplifiers in their respective stages. Therefore, the HDC_k blocks for $k = 1$, 2, 3, and 4 perform their measurements of $\tilde{\alpha}_{1,k}$ and $\tilde{\alpha}_{3,k}$ sequentially and periodically, first for $k = 4$, then for $k = 3$, then for $k = 2$, and then for $k = 1$, after which the process repeats [5]. Each HDC block continually implements (24) with the most recent $\tilde{\alpha}_{1,k}$ and $\tilde{\alpha}_{3,k}$ values it measured.

III. Effect of Quantization Error on HDC Coefficient Estimation

The goal of HDC in each stage is to perfectly cancel the distortion terms introduced by that stage's residue amplifier. Unfortunately, the cancellation is never perfect in practice because the operations that the HDC_k blocks perform to estimate $\alpha_{1,k}$ and $\alpha_{3,k}$, and to cancel the nonlinear distortion terms involve approximations.

For example, suppose that the pipelined ADC of Fig. 3 is ideal except that the flash ADCs have threshold errors and the $\alpha_{1,1}$, $\alpha_{3,1}$, and $\alpha_{1,2}$ coefficients are non-zero. If the HDC blocks correctly measure $\tilde{\alpha}_{3,k} = 0$ for $k = 2$, 3, and 4, and $\tilde{\alpha}_{1,k} = 0$ for $k = 3$, and 4, then the only significant contribution to the last term in (11) with $k = 1$ occurs because of the HDC_2 block's imperfect estimation of $\alpha_{1,2}$. In this case it follows from (1), (5), (6), (8), (24) and Fig. 4, that (11) becomes

$$r_1[n] = (1+\alpha_{1,1})\, v_1(nT_s) + \alpha_{3,1} v_1^3(nT_s) + \frac{1}{4^5} e_{ADC,6}[n] + e_{HDC,2}[n] \quad (25)$$

where

$$e_{HDC,2}[n] = -\frac{\tilde{\alpha}_{1,2}}{4^5(1+\tilde{\alpha}_{1,2})} e_{ADC,6}[n] + \frac{\lambda_2}{4}\left(e_{ADC,2}[n] + c_2[n]\right), \quad (26)$$

and

$$\lambda_2 = \frac{(\tilde{\alpha}_{1,2} - \alpha_{1,2})}{(1+\tilde{\alpha}_{1,2})}. \quad (27)$$

The $e_{HDC,2}[n]$ term represents the error in $r_1[n]$ caused by the HDC_2 block's imperfect estimation of $\alpha_{1,2}$. It adds directly to the pipelined ADC output, but even if its mean squared value is below the noise floor of the pipelined ADC, it still can sometimes degrade the performance of the pipelined ADC by corrupting the HDC_1 block's estimates of $\alpha_{1,1}$ and $\alpha_{3,1}$. This happens because for some pipelined ADC input signals $e_{ADC,2}[n]$ is very strongly correlated with both $c_{1,1}[n]$ and $c_{3,1}[n]$.

For example, consider a special case of the above example wherein $\alpha_{1,1} = 0$, $\alpha_{3,1} = 0$, flash ADC_2 has just a single threshold error, $\lambda_2 = 0.001$ (which is consistent with the measured results presented in [5]), and the pipelined ADC's input sequence is $V_{in}(nT_s) = \Delta$ for all n. Given that $\alpha_{1,1} = 0$ and $\alpha_{3,1} = 0$, the ideal operation of the HDC_1 block would be to calculate $\tilde{\alpha}_{1,1} = 0$ and $\tilde{\alpha}_{3,1} = 0$ in which case it would have no effect on $r_1[n]$ and the only effect of the $e_{HDC,2}[n]$ term would be to decrease the pipelined ADC's SNDR by about 1.5 dB relative to its ideal (quantization noise only) value.

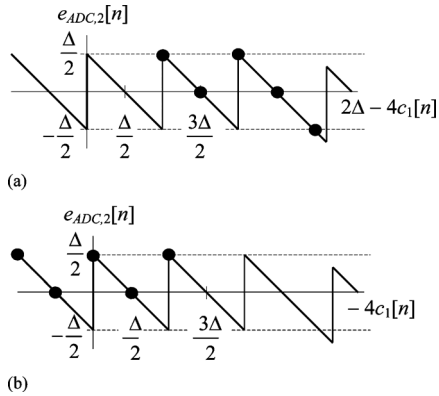

Fig. 6. The five values of $e_{ADC,2}[n]$ that occur when the input to flash ADC_2 is: (a) $2\Delta - 4c_1[n]$ and (b) $-4c_1[n]$ superimposed on a plot of the input-output characteristic of flash ADC_2 (which contains a single threshold error).

Unfortunately, the $e_{HDC,2}[n]$ term causes the HDC_1 block not to operate ideally for this example. The input to flash ADC_2 is $2\Delta - 4c_1[n]$, so $e_{ADC,2}[n]$ for each n takes on one of the five points shown in Fig. 6(a) (one of which is affected by the threshold error). The resulting correlations of $e_{ADC,2}[n]$ with $c_{1,1}[n]$ and $c_{3,1}[n]$ are both $-\Delta/16$ which causes the HDC_1 block to incorrectly calculate $\tilde{\alpha}_{1,1} \cong 0.0082$ and $\tilde{\alpha}_{3,1} \cong -0.17$ (via (14) and (23)). By implementing (24) with these incorrect estimates of $\alpha_{1,1}$ and $\alpha_{3,1}$, the HDC_1 block introduces significant nonlinear distortion in this case such that the pipelined ADC's SNDR is reduced by about 23 dB relative to its ideal value.

This problem is highly dependent upon the pipelined ADC's input sequence. For example, suppose that the example above is changed only in that $V_{in}(nT_s) = 0.5\Delta$ for all n. Then, the input to flash ADC_2 is $-4c_1[n]$, and the possible values of $e_{ADC,2}[n]$ are the five points shown in Fig. 6(b). The resulting correlations of $e_{ADC,2}[n]$ with $c_{1,1}[n]$ and $c_{3,1}[n]$ are both zero, so the HDC_1 block correctly measures $\tilde{\alpha}_{1,1} = 0$ and $\tilde{\alpha}_{3,1} = 0$ in this case. Thus, for this input sequence, the leakage of $e_{ADC,2}[n]$ into $r_1[n]$ does not lead to incorrect estimates of $\alpha_{1,1}$ and $\alpha_{3,1}$, so the pipelined ADC's SNDR is only degraded by approximately 1.5 dB from the presence of $e_{HDC,2}[n]$ in the output sequence.

Returning to the more general situation in which $\alpha_{1,1}$, $\alpha_{3,1}$, and $\alpha_{1,2}$ are non-zero, it is straightforward to verify that (16), (25), and (26) imply that the errors in the HDC_1 block's estimates of $\gamma_{1,1}$ and $\gamma_{3,1}$ caused by correlations of $e_{ADC,2}[n]$ with $c_{1,1}[n]$ and $c_{3,1}[n]$ have magnitudes that are bounded by

$$\frac{\lambda_2 e_{ADC,\max}}{4A}, \quad \text{and} \quad \frac{\lambda_2 e_{ADC,\max}}{24A^3}, \quad (28)$$

respectively, where $e_{ADC,\max}$ is the largest possible magnitude of $e_{ADC,k}[n]$ for all n and k. While the bounds given by (28)

are not tight, specific pipelined ADC input values are known to the authors for which the errors in the HDC_1 block's estimates of $\gamma_{1,1}$ and $\gamma_{3,1}$ have magnitudes that are larger than half those in (28).

Therefore, in the worst case scenarios the HDC_1 block's estimates of $\alpha_{1,1}$ and $\alpha_{3,1}$ are corrupted by error terms that depend on A^{-1} and A^{-3}. If these error terms have magnitudes that are significant relative to the magnitudes of $\alpha_{1,1}$ and $\alpha_{3,1}$, then the HDC_1 block at best will not cancel distortion from the first stage's residue amplifier accurately, and at worst can actually introduce extra distortion (as in the example described above). The error terms can be reduced by increasing A, but, as described in the previous section, increasing A uses up more of the over-range margin of the subsequent stage. This places a practical upper bound on A, so it is not always possible to make A large enough that the errors caused by correlations of $e_{ADC,2}[n]$ with $c_{1,1}[n]$ and $c_{3,1}[n]$ are negligible for all pipelined ADC input signals.

Similar results hold for the other HDC blocks. In general, for the worst case input signals the estimation process in each HDC block is highly sensitive to quantization error terms from subsequent stages that leak into its stage's digitized residue. For some ADC input sequences the error terms corrupt the HDC block's $\alpha_{i,k}$ coefficient estimates even when their average power is negligible compared to those of the other error sources in the pipelined ADC. In such cases the error terms do not significantly reduce the pipelined ADC SNDR directly, but rather they cause HDC blocks to introduce error that reduces the SNDR as result of the inaccurate estimates of the $\alpha_{i,k}$ coefficients.

A pipelined ADC converts each sample of its input sequence to a digital number independently of all prior input samples, and each sample of the correlation sequence is statistically independent of all prior correlation sequence samples by design, so the statistical expectation of the HDC estimation error caused by quantization error leakage at time n has no dependence on prior pipelined ADC input samples. Furthermore, a pipelined ADC implements a time-invariant discrete-time system and the calibration sequence is a stationary random process by design, so any dependence of the expectation of the estimation error on each pipelined ADC input sequence value must be independent of the sample time n. It follows that there is at least one input value that maximizes this estimation error expectation at any time n, so keeping the input signal constant at this worst case value for all sample times maximizes the effect of the problem. This is why the set of worst case pipelined ADC input sequences includes one or more constant sequences.

It follows that the full extent of the problem can be evaluated by considering the HDC coefficient estimation process for all constant input sequences. Furthermore, if the HDC technique is modified such that the HDC coefficients are estimated accurately for every constant pipelined ADC input sequence, it follows that the modification will also cause the coefficients to be estimated accurately for every non-constant pipelined ADC input sequence. Consequently, the simulation results presented in the remainder of this paper only consider cases in which the HDC blocks estimate their coefficients for constant pipelined ADC input sequences.

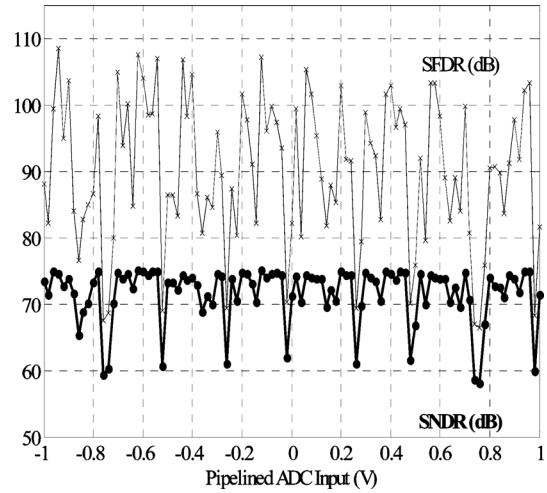

Fig. 7. Simulation results for pipelined ADC shown in Fig. 3 with $f_{in} = 0.39f_s$ and 0 dBFS sinusoidal input signal.

As explained in [5], the problem can be mitigated by using $N = 5$ $t_{i,k}[n]$ sequences in (10) instead of $N = 3$ as originally proposed in [4]. The two extra $t_{i,k}[n]$ sequences act as dither which tends to reduce the correlations of $e_{ADC,2}[n]$ with $c_{1,1}[n]$ and $c_{3,1}[n]$. Unfortunately, even with $N = 5$ the problem still occurs for pipelined ADC input signals that have small peak-to-peak variations about certain constant values.

Fig. 7 shows simulation results that illustrate the problem for the example pipelined ADC shown in Fig. 3 using calibration sequences given by (10) with $N = 5$. The simulated pipelined ADC includes DEM DACs and the DAC noise cancellation (DNC) technique as described in [5] with capacitor mismatches chosen such that the pipelined ADC's SNR would be limited to about 67 dB in the absence of other errors if DNC were disabled (DNC is not shown in Fig. 3). The flash ADC threshold errors were chosen randomly with a standard deviation of $\Delta/25$. The distortion coefficients of the first stage were chosen to be $\alpha_{1,1} = -0.085$ and $\alpha_{3,1} = -0.3$, and the remaining stages' distortion coefficients are similar and are consistent with the measured results reported in [5].

The SNDR and SFDR values shown in Fig. 7 correspond to a 0 dBFS sinusoidal input signal with a frequency of $0.39f_s$ where f_s is the input sample-rate of the pipelined ADC. Each pair of SNDR and SFDR values were obtained by simulating the pipelined ADC with the sinusoidal input sequence but with the HDC blocks using nonlinearity coefficients that were obtained from a previous simulation with a constant pipelined ADC input sequence. Each SNDR and SFDR value is plotted versus the amplitude of the constant input sequence for which the corresponding nonlinearity coefficients were estimated. As expected from the problem explanation above, there are significant reductions (of approximately 16 dB) in SNDR and SFDR when the HDC coefficients are measured for certain constant input signals.

As demonstrated by the examples described above, the extent to which the quantization error in each pipeline stage is correlated with $c_{1,k}[n]$ and $c_{3,k}[n]$ depends on the pipelined ADC's input sequence. Therefore, it makes sense that the accuracy of the HDC coefficient estimation process depends on

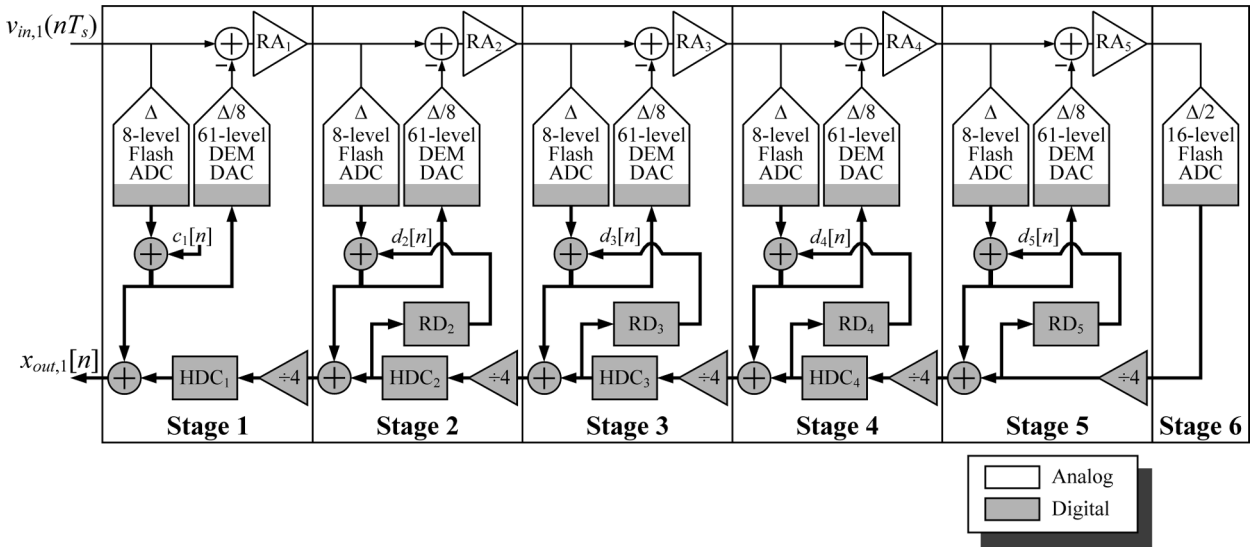

Fig. 8. Pipelined ADC configuration during estimation of $\alpha_{1,1}$ and $\alpha_{3,1}$ with HDC in the first stage and RD applied to the remaining stages.

the pipelined ADC's input sequence. This effect is exacerbated when the pipelined ADC's input sequence is such that the mean squared value of $e_{ADC,k}[n]$ is large during the coefficient estimation process, particularly for $k = 1$. In these cases $\tilde{\eta}_{2,k}$ is so large that the second term in the factor of $\tilde{\gamma}_{3,k}$ in (19) is dominant and effectively amplifies any error in $\tilde{\gamma}_{3,k}$. The authors have verified that the large dips in SNDR and SFDR shown in Fig. 7 correspond to these cases.

IV. Solution to the Quantization Error Problem

As described in Section II the HDC blocks estimate their nonlinearity coefficients sequentially, so only one HDC block in the pipelined ADC is in the process of estimating its stage's nonlinearity coefficients at any given time. Therefore, whenever the HDC_j block is in the process of estimating the $\alpha_{1,j}$ and $\alpha_{3,j}$ coefficients, the calibration sequences in the subsequent pipeline stages are not necessary, i.e., calibration sequence $c_k[n]$ need not be added to the output of flash ADC_k for any $k > j$.

The proposed solution to the problem described in the previous section is to replace the $c_k[n]$ sequences for $k = j + 1, j + 2, \ldots, 5$, where j is the number of the stage in which the nonlinearity coefficients are currently being estimated, by new sequences, $d_k[n]$, designed to cancel the unwanted correlations. In the example described in the previous section, the problem is that the HDC_1 block estimates $\alpha_{1,1}$ and $\alpha_{3,1}$ poorly when the pipelined ADC input signal is such that $e_{ADC,2}[n]$ in (26) is correlated with either $c_{1,1}[n]$ or $c_{3,1}[n]$. In general the problem is that the HDC_j block estimates $\alpha_{1,j}$ and $\alpha_{3,j}$ poorly when the pipelined ADC input signal is such that $e_{ADC,k}[n]$ is correlated with either $c_{1,j}[n]$ or $c_{3,j}[n]$ for any $k > j$. This problem can be avoided if the $d_k[n]$ sequences satisfy

$$\frac{1}{P}\sum_{n=m}^{m+P-1}\left(e_{ADC,k}[n] + d_k[n]\right)c_{3,j}[n] \to 0 \tag{29}$$

and

$$\frac{1}{P}\sum_{n=m}^{m+P-1}\left(e_{ADC,k}[n] + d_k[n]\right)c_{1,j}[n] \to 0, \tag{30}$$

in probability as $P \to \infty$ for $k = j + 1, j + 2, \ldots, 5$.

A. Implementation Details

This sub-section describes the implementation details of the proposed solution. A detailed explanation of why it works, and, therefore, the motivation underlying its design, is deferred to Sections IV-B and IV-C.

Fig. 8 shows the example pipelined ADC described previously with HDC applied to the first four stages for the case in which the HDC_1 block is in the process of estimating $\alpha_{1,1}$ and $\alpha_{3,1}$. The blocks labeled RD_k, for $k = 2$, 3, 4, and 5, are called *residue decorrelator* (RD) blocks because they generate the above-mentioned $d_k[n]$ sequences. Whenever the HDC_j block for $j \neq 1$ is in the process of estimating $\alpha_{1,j}$ and $\alpha_{3,j}$, the block diagram changes from that shown in Fig. 8 only in that $c_k[n]$ is added to the output of flash ADC_k in place of $d_k[n]$ for $k = 2, 3, \ldots, j$.[2]

Fig. 9 shows a block diagram of the RD_k block configured for the case in which the HDC_j block with $j < k$ is in the process of estimating $\alpha_{1,j}$ and $\alpha_{3,j}$. The function h shown in the figure is defined as

$$h(x) = \begin{cases} 1, & \text{if } x > 0, \\ -1, & \text{if } x < 0, \\ 0, & \text{if } x = 0. \end{cases} \tag{31}$$

The HDC blocks are the same as described in Section II, except they use different correlation sequences than given by (13) as described below. The calibration sequences are as given by (10) with $N = 4$.

The modified correlation sequences used in both the HDC and RD blocks are

$$c_{1,j}[n] = \begin{cases} -\frac{1}{4}\frac{c_j[n]}{A}, & \text{if } c_j[n] \neq 0, \\ c_a[n], & \text{if } c_j[n] = 0 \text{ and } t_{1,j}[n] = t_{2,j}[n], \\ c_b[n], & \text{otherwise}, \end{cases} \tag{32}$$

[2]While adding $c_k[n]$ to the output of flash ADC_k for $k < j$ is not absolutely necessary, it is done anyway to dither the flash ADCs. This reduces the unwanted correlations, thereby slightly improving the accuracy of the HDC correlations.

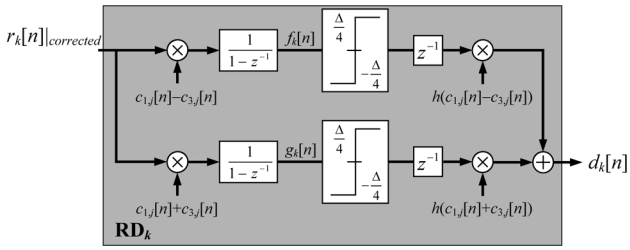

Fig. 9. Details of the RD_k block.

and

$$c_{3,j}[n] = \begin{cases} -\frac{1}{4}\frac{s_j[n]}{A^3} & \text{if } c_j[n] \neq 0, \\ c_a[n], & \text{if } c_j[n] = 0 \text{ and } t_{1,j}[n] = t_{2,j}[n], \\ -c_b[n], & \text{otherwise,} \end{cases} \tag{33}$$

where

$$s_j[n] = t_{1,j}[n]t_{2,j}[n]t_{3,j}[n] + t_{1,j}[n]t_{2,j}[n]t_{4,j}[n] + t_{2,j}[n]t_{3,j}[n]t_{4,j}[n] + t_{1,j}[n]t_{3,j}[n]t_{4,j}[n], \tag{34}$$

and $c_a[n]$ and $c_b[n]$ are two-level zero-mean pseudorandom sequences that take on values of $\pm B$ and are independent from each other and from $c_j[n]$. The constant B must satisfy

$$B \geq \frac{4e_{ADC,\max}}{\Delta} - 1. \tag{35}$$

Therefore, when $e_{ADC,\max} = \Delta/2$ (i.e., in the absence of non-ideal circuit behavior), $B = 1$ is acceptable, but in practice B must be somewhat greater than one to accommodate the maximum anticipated non-ideal flash ADC errors. Any value of B that satisfies (35) will work, but increasing B increases the HDC convergence time, so B should be chosen as small as possible subject to the constraint of (35).

The RD block solution described above involves only digital circuitry, and the expected area and power dissipation of the circuitry are small compared to those of the digital circuitry required by the HDC technique without the RD block solution. Therefore, the RD block solution is not expected to contribute significantly to the overall circuit area or power dissipation of typical pipelined ADCs to which it would be applied.

B. Theory of Operation

As depicted in Fig. 8, each RD_k block operates on the output of the HDC_k block and generates the $d_k[n]$ sequence. As explained below, it forms a feedback loop which adaptively adjusts $d_k[n]$ such that the correlations of the HDC_k block's output sequence with $c_{1,j}[n]$ and $c_{3,j}[n]$ converge to zero. The output of the HDC_k block satisfies

$$r_k[n]|_{corrected} \cong -e_{ADC,k}[n] - d_k[n] \tag{36}$$

to a high degree of accuracy, so this causes (29) and (30) to be satisfied with a high degree of accuracy.

It follows from (36) and Fig. 9 that the outputs of the top and bottom accumulators in the RD_k block can be written as

$$f_k[n] \cong -\sum_{i=0}^{n} \left(e_{ADC,k}[i] + d_k[i]\right)\left(c_{1,j}[i] - c_{3,j}[i]\right) \tag{37}$$

and

$$g_k[n] \cong -\sum_{i=0}^{n} \left(e_{ADC,k}[i] + d_k[i]\right)\left(c_{1,j}[i] + c_{3,j}[i]\right). \tag{38}$$

As explained below, the RD_k block chooses the $d_k[n]$ sequence to ensure that both $f_k[n]$ and $g_k[n]$ are bounded in probability for all n. This implies that

$$\frac{1}{n}\left(f_k[n] - g_k[n]\right) \to 0 \tag{39}$$

and

$$\frac{1}{n}\left(f_k[n] + g_k[n]\right) \to 0 \tag{40}$$

in probability as $n \to \infty$, and therefore that both (29) and (30) hold.

Table I shows the $t_{i,j}[n]/A$ values along with the corresponding values of $c_j[n]/A$, $c_{1,j}[n]$, $c_{3,j}[n]$, and $c_{1,j}[n] \pm c_{3,j}[n]$, for each of the 16 possible sets values that $t_{1,j}[n]$, $t_{2,j}[n]$, $t_{3,j}[n]$, $t_{4,j}[n]$ can take on. By definition, each of the 16 possible sets occurs with a probability of 1/16. In the following, several observations are made from Table I to show that (39) and (40) hold in probability as $n \to \infty$.

Table I indicates that one or the other of $c_{1,j}[n] + c_{3,j}[n]$ and $c_{1,j}[n] - c_{3,j}[n]$ is guaranteed to be zero at each time index n, so it can be seen from Fig. 9 that only one of $f_k[n]$ and $g_k[n]$ changes each time n is incremented. Consequently, for each value of n, $d_k[n]$ influences $f_k[n]$ but has no effect on $g_k[n]$ if $c_{1,j}[n] - c_{3,j}[n]$ is nonzero, or *vice versa* if $c_{1,j}[n] + c_{3,j}[n]$ is nonzero. This is why it is possible for $d_k[n]$ to keep both $f_k[n]$ and $g_k[n]$ bounded; each RD block implements two feedback loops that are interlaced with each other such that no crosstalk occurs between them.

It follows from Fig. 9, (31), and (36) that

$$f_k[n] = f_k[n-1] - e_{ADC,k}[n]\left(c_{1,j}[n] - c_{3,j}[n]\right) - \frac{\Delta}{4}\mathrm{sgn}\left\{f_k(n-1)\right\}\left|c_{1,j}[n] - c_{3,j}[n]\right|, \tag{41}$$

and

$$g_k[n] = g_k[n-1] - e_{ADC,k}[n]\left(c_{1,j}[n] + c_{3,j}[n]\right) - \frac{\Delta}{4}\mathrm{sgn}\left\{g_k(n-1)\right\}\left|c_{1,j}[n] + c_{3,j}[n]\right|, \tag{42}$$

where $\mathrm{sgn}\{x\} = 1$ if $x \geq 0$ and $\mathrm{sgn}\{x\} = -1$ otherwise. The last terms in (41) and (42) correspond to $d_k[n](c_{1,j}[n] - c_{3,j}[n])$ and $d_k[n](c_{1,j}[n] + c_{3,j}[n])$, respectively. For each n, one of these terms is zero and the other has the opposite sign of the corresponding value of $f_k[n-1]$ or $g_k[n-1]$.

To show that this ensures $f_k[n]$ and $g_k[n]$ are bounded in probability for all n, it remains to show that in each of (41) and (42) the average magnitude of the last term is at least as large as that of the term proportional to $e_{ADC,k}[n]$. That is, for (41) it remains to show that

$$\frac{\Delta}{4}\mathrm{E}\left\{\left|c_{1,j}[n] - c_{3,j}[n]\right| \middle| c_{1,j}[n] - c_{3,j}[n] \neq 0\right\} \tag{43}$$

TABLE I
ALL POSSIBLE SETS OF VALUES THAT $t_{1,j}[n]/A, t_{2,j}[n]/A, t_{3,j}[n]/A, t_{4,j}[n]/A$ CAN TAKE ON ALONG WITH THE CORRESPONDING VALUES OF $c_j[n]/A$, $c_{1,j}[n]$, $c_{3,j}[n]$, AND $c_{1,j}[n] \pm c_{3,j}[n]$

$t_{1,j}[n]/A$	$t_{2,j}[n]/A$	$t_{3,j}[n]/A$	$t_{4,j}[n]/A$	$c_j[n]/A$	$c_{1,j}[n]$	$c_{3,j}[n]$	$c_{1,j}[n] + c_{3,j}[n]$	$c_{1,j}[n] - c_{3,j}[n]$
−1	−1	−1	−1	−4	1	1	2	0
−1	−1	−1	1	−2	1/2	−1/2	0	1
−1	−1	1	−1	−2	1/2	−1/2	0	1
−1	−1	1	1	0	$c_a[n]$	$c_a[n]$	$2c_a[n]$	0
−1	1	−1	−1	−2	1/2	−1/2	0	1
−1	1	−1	1	0	$c_b[n]$	$-c_b[n]$	0	$2c_b[n]$
−1	1	1	−1	0	$c_b[n]$	$-c_b[n]$	0	$2c_b[n]$
−1	1	1	1	2	−1/2	1/2	0	−1
1	−1	−1	−1	−2	1/2	−1/2	0	1
1	−1	−1	1	0	$c_b[n]$	$-c_b[n]$	0	$2c_b[n]$
1	−1	1	−1	0	$c_b[n]$	$-c_b[n]$	0	$2c_b[n]$
1	−1	1	1	2	−1/2	1/2	0	−1
1	1	−1	−1	0	$c_a[n]$	$c_a[n]$	$2c_a[n]$	0
1	1	−1	1	2	−1/2	1/2	0	−1
1	1	1	−1	2	−1/2	1/2	0	−1
1	1	1	1	4	−1	−1	−2	0

is at least as large as

$$\left|\mathrm{E}\left\{e_{ADC,k}[n](c_{1,j}[n]-c_{3,j}[n])\middle|c_{1,j}[n]-c_{3,j}[n]\neq 0\right\}\right| \tag{44}$$

and for (42) it remains to show that

$$\frac{\Delta}{4}\mathrm{E}\left\{\left|c_{1,j}[n]+c_{3,j}[n]\right|\middle|c_{1,j}[n]+c_{3,j}[n]\neq 0\right\} \tag{45}$$

is at least as large as

$$\left|\mathrm{E}\left\{e_{ADC,k}[n]\,(c_{1,j}[n]+c_{3,j}[n])\middle|c_{1,j}[n]+c_{3,j}[n]\neq 0\right\}\right|. \tag{46}$$

As mentioned above each row of Table I corresponds to one of the 16 possible sets of values that $t_{1,j}[n]$, $t_{2,j}[n]$, $t_{3,j}[n]$, $t_{4,j}[n]$ can take on, so the rows correspond to mutually exclusive events that each occur with a probability of 1/16. Therefore, Table I implies that (43) evaluates to $(2/3)\cdot\Delta(1+B)/4$ and (45) evaluates to $\Delta(1+B)/4$.

Table I indicates that the correlation sequences contain $c_a[n]$ and $c_b[n]$ only when the calibration sequence is zero. This implies that the input sequence to the flash ADC in the $(j+1)$th stage is statistically independent of $c_a[n]$ and $c_b[n]$, so $e_{ADC,j+1}[n]$ is also statistically independent of $c_a[n]$ and $c_b[n]$. Since $c_a[n]$ and $c_b[n]$ are both zero-mean sequences, it follows that the correlations of $e_{ADC,j+1}[n]$ with the correlation sequences are both zero. Therefore, Table I implies that (44) and (46) must be no larger than $(2/3)e_{ADC,\max}$ and $e_{ADC,\max}$, respectively.

It follows that (43) and (45) are at least as large as both (44) and (46) if $\Delta(1+B)/4 \geq e_{ADC,\max}$, which is equivalent to (35). Therefore, (29) and (30) are satisfied in probability as $P\rightarrow\infty$ for $k=j+1, j+2,\ldots,5$ by the solution described in Section IV-A.

C. Calibration Sequence Choice

As described in Section II, the number, N, of two-level sequences added to form the calibration sequence $c_j[n]$ must be at least as large as the highest order of nonlinear distortion to be cancelled by the HDC algorithm. Therefore, the minimum possible value of N is 3 when the residue amplifiers are well-modeled by (8).

However, if $N=3$ were used with the solution presented in Section IV-B, the magnitude of $d_k[n]$ would have had to be $e_{ADC,\max}$ to ensure full cancellation of the unwanted correlation terms for all pipelined ADC input signals. Since $e_{ADC,\max}$ is greater than $\Delta/2$ in practice, such $d_k[n]$ sequences would exceed the over-range margin of the pipeline stages.

The solution proposed in Section IV-B uses $N=4$ to avoid this problem. With $N=4$ the calibration sequence, $c_j[n]$, is zero 6/16 of the time (see Table I), and whenever this happens $e_{ADC,j+1}[n]$ is uncorrelated with the correlation sequences as explained in Section IV-B. However, as shown in Section IV-B, the $d_{j+1}[n]$ sequence is correlated with the correlation sequences regardless of whether the calibration sequence is zero, which makes it possible to operate properly with $d_k[n]$ sequences that have a magnitude of only $\Delta/4$. Therefore, the $d_k[n]$ sequences use exactly the same portion of the over-range margin as the calibration sequences.

D. Simulation Results

Fig. 10 shows computer simulation results that are identical to those which produced the data shown in Fig. 7, except that the simulated pipelined ADC was enhanced with the modified calibration sequences and RD blocks as described above. As in Fig. 7, the SNDR and SFDR values shown in Fig. 10 correspond to a 0 dBFS sinusoidal input signal with frequency of $0.39f_s$. Each pair of SNDR and SFDR values were obtained by simulating the enhanced pipelined ADC with the sinusoidal input sequence but with the HDC blocks using $\alpha_{1,k}$ and $\alpha_{3,k}$ coefficients that were obtained previously by simulating the pipelined

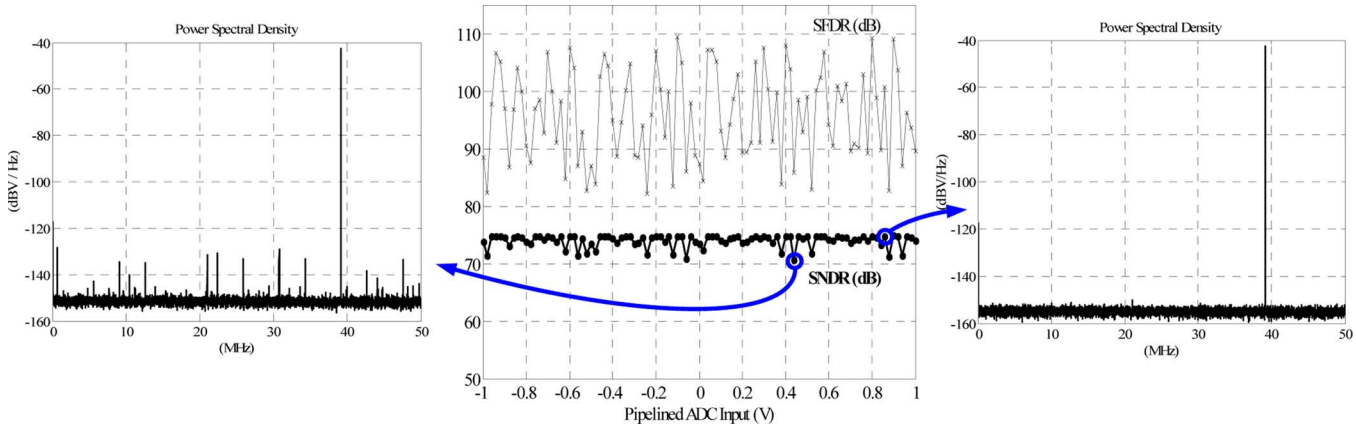

Fig. 10. Simulation results for pipelined ADC shown in Fig. 8 with $f_{in} = 0.39 f_s$ and 0 dBFS sinusoidal input signal and with representative power spectral density plots of the output.

ADC with a constant input. Each SNDR and SFDR value is plotted versus the input sequence for which $\alpha_{1,k}$ and $\alpha_{3,k}$ coefficients were estimated.

A comparison of Figs. 7 and 10 indicates that the proposed technique improves the worst case SNDR and SFDR values by 12.6 dB and 15.8 dB, respectively. Numerous other simulation experiments performed by the authors have yielded quantitatively similar results. The proposed technique involves several approximations as described above, so it does not completely eliminate the variability of the SNDR and SFDR with the input signal, but it greatly reduces the variability as intended.

As explained in Section III, accurate nonlinearity coefficient estimation for all constant input sequences implies accurate coefficient convergence for all non-constant input sequences too. Therefore, the results support the assertion that the solution to the quantization-induced convergence error problem presented in this paper enables correct operation of the HDC_k blocks regardless of the pipelined ADC input signal.

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Nevena Rakuljic (M'06) received the B.S., M.S., and Ph.D. degrees from the University of California, San Diego, in 2006, 2009, and 2012, respectively.

From 2006 to 2012, she was a member of the Integrated Signal Processing Group, where she worked on dynamic element matching for multibit DACs and digital calibration techniques for pipelined ADCs. Currently, she is with Analog Devices, Inc.

Ian Galton (M'92–SM'09–F'11) received the Sc.B. degree from Brown University, Providence, RI, in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1989 and 1992, respectively, all in electrical engineering.

Since 1996 he has been a Professor of Electrical Engineering at the University of California, San Diego, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996 he was with UC Irvine, and prior to 1989 he was with Acuson and Mead Data Central. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters and phase-locked loops. In addition to his academic research, he regularly consults at several semiconductor companies and teaches industry-oriented short courses on the design of mixed-signal integrated circuits.

Dr. Galton is a Fellow of the IEEE, and has served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.