Delta-Sigma FDC Based Fractional-N PLLs

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***Abstract*—Fractional-N phase-locked loop frequency synthesizers based on time-to-digital converters (TDC-PLLs) have been proposed to reduce the area and linearity requirements of conventional PLLs based on delta-sigma modulation and charge pumps ($\Delta\Sigma$-PLLs). Although TDC-PLLs with good performance have been demonstrated, TDC quantization noise has so far kept their phase noise and spurious tone performance below that of the best comparable $\Delta\Sigma$-PLLs. An alternative approach is to use a delta-sigma frequency-to-digital converter ($\Delta\Sigma$ FDC) in place of a TDC to retain the benefits of TDC-PLLs and $\Delta\Sigma$-PLLs. This paper proposes a practical $\Delta\Sigma$ FDC based PLL in which the quantization noise is equivalent to that of a $\Delta\Sigma$-PLL. It presents a linearized model of the PLL, design criteria to avoid spurious tones in the $\Delta\Sigma$ FDC quantization noise, and a design methodology for choosing the loop parameters in terms of standard PLL target specifications.**

***Index Terms*—Delta-sigma, fractional-N, frequency discriminator, frequency synthesizers, phase-locked loop, phase noise, PLL.**

I. Introduction

DELTA-SIGMA modulator based fractional-N phase-locked loops ($\Delta\Sigma$-PLLs) of the type shown in Fig. 1 are widely used as local oscillator frequency synthesizers in wireless communication systems because they offer excellent spectral purity with virtually unlimited frequency tuning resolution [1]–[4]. Unfortunately, to achieve the performance necessary for most wireless applications a $\Delta\Sigma$-PLL requires a highly-linear charge pump and large loop filter capacitance, often on the order of hundreds of pico-Farads. Typically, this necessitates an off-chip loop filter, which increases the pin count, circuit footprint, and overall system cost. Furthermore, in highly-scaled CMOS technology, low voltage headroom on the input node of the voltage controlled oscillator (VCO) necessitates tradeoffs that limit performance. Reducing the voltage swing requires an increase in the VCO gain which tends to increase the phase noise, yet increasing the voltage swing for a given supply voltage reduces charge pump linearity which increases spurious tones.

Recently, fractional-N PLLs have been proposed that exploit digital signal processing to avoid these problems [5]–[10]. They use a time-to-digital converter (TDC), a digital loop filter, and a digitally controlled oscillator (DCO) in place of a divider, phase-frequency detector (PFD), charge pump, analog loop filter, and VCO. The TDC generates a quantized estimate of the instantaneous phase of the DCO at each positive edge of the reference oscillator. The difference between the calculated instantaneous phase of an ideal oscillator running at the desired output frequency and the TDC output is digitally lowpass filtered and the resulting digital sequence controls the DCO.

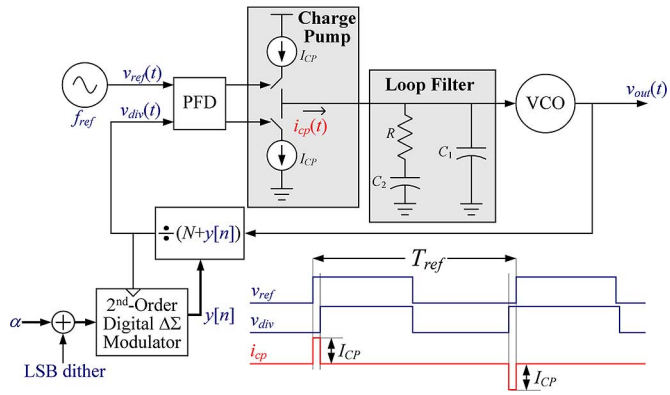

Fig. 1. A delta-sigma modulator based fractional-N PLL ($\Delta\Sigma$-PLL).

Although such TDC-based PLLs (TDC-PLLs) have been demonstrated to have very good performance, TDC quantization noise has so far kept their phase noise and spurious tone performance below those of the best comparable $\Delta\Sigma$-PLLs. TDC quantization noise is relatively coarse and, unlike quantization noise in $\Delta\Sigma$-PLLs, it is not highpass shaped so it is not as well suppressed by the PLL.

An alternative approach that offers the advantages of both $\Delta\Sigma$-PLLs and TDC-PLLs is to use a delta-sigma frequency-to-digital converter ($\Delta\Sigma$ FDC) in place of a TDC [11]–[14]. Such $\Delta\Sigma$ FDC based fractional-N PLLs (FDC-PLLs) have been proposed in which the $\Delta\Sigma$ FDC performs 1-bit quantization and the DCO is implemented as a DAC followed by a VCO [15], [16]. It is likely that improved performance can be achieved in future FDC-PLLs by using the type of high-performance DCOs developed for TDC-PLLs and, as quantified in this paper, by avoiding 1-bit quantization in the $\Delta\Sigma$ FDC.

This paper proposes a practical FDC-PLL architecture and proves that its quantization noise performance is equivalent to that of a $\Delta\Sigma$-PLL with a second-order delta-sigma modulator. It shows that 5-level quantization in the $\Delta\Sigma$ FDC is both necessary and sufficient to avoid spurious tones that would otherwise be caused by quantizer overloading. It derives a linearized model that accurately predicts the transfer functions imposed by the FDC-PLL on its component noise sources, and provides a design methodology based on the model for choosing the loop parameters in terms of standard PLL target specifications.

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II. Background Information

A. Phase Noise in Fractional-N PLLs

The instantaneous frequency of the reference oscillator in Hz is

$$f_{\rm ref} + \psi_{\rm ref}(t) \tag{1}$$

where $f_{\rm ref}$ is the nominal reference frequency, and $\psi_{\rm ref}(t)$ is the reference oscillator's instantaneous frequency error. The reference oscillator's instantaneous phase in cycles relative to an initial time, t_0, is the integral of (1) from time t_0 to time t:

$$p_{\rm ref}(t) = (t - t_0)f_{\rm ref} + \theta_{\rm ref}(t) \tag{2}$$

where

$$\theta_{\rm ref}(t) = \int_{t_0}^{t} \psi_{\rm ref}(u)du \tag{3}$$

is the reference oscillator's instantaneous phase noise in cycles.

A fractional-N PLL generates a periodic output signal with an average frequency of $(N+\alpha)f_{\rm ref}$, where N is an integer and α is a fractional value with a magnitude less than 1. Therefore, its instantaneous output frequency in Hz can be written as

$$f_{\rm PLL}(t) = (N + \alpha)f_{\rm ref} + \psi_{\rm PLL}(t) \tag{4}$$

where $\psi_{\rm PLL}(t)$ is its instantaneous frequency error. The PLL's instantaneous output phase in cycles relative to time t_0 is the integral of (4) from time t_0 to time t:

$$p_{\rm PLL}(t) = (t - t_0)(N + \alpha)f_{\rm ref} + \theta_{\rm PLL}(t) \tag{5}$$

where

$$\theta_{\rm PLL}(t) = \int_{t_0}^{t} \psi_{\rm PLL}(u)du \tag{6}$$

is the PLL's instantaneous phase noise in cycles.

A fractional-N PLL must control its output frequency such that $\psi_{\rm PLL}(t)$ has zero mean and the power spectral density (PSD) of $\theta_{\rm PLL}(t)$ is within acceptable limits for the desired application. As described below, the $\Delta\Sigma$-PLL and the FDC-PLL each do this by estimating a phase error sequence proportional to

$$-\theta_{\rm PLL}(t) + (N + \alpha)\theta_{\rm ref}(t) \tag{7}$$

sampled at the reference frequency, passing the estimated phase error sequence through their loop filter, and using the output of the loop filter to control the output frequency of their VCO or DCO. The feedback ensures that $\psi_{\rm PLL}(t)$ has zero mean (provided that $\psi_{\rm ref}(t)$ has zero mean), and the characteristics of the loop filter, the DC loop gain, and the accuracy with which (7) is estimated determine the spectral properties of $\theta_{\rm PLL}(t)$.

B. $\Delta\Sigma$ Fractional-N PLLs

A typical $\Delta\Sigma$-PLL is shown in Fig. 1. It consists of a PFD, a charge pump, an analog loop filter, a VCO, a frequency divider, and a second-order digital delta-sigma modulator clocked by the divider output.

The divider output is a two-level signal in which the nth and $(n+1)$th rising edges are separated by $N + y[n]$ VCO periods, where $y[n]$ is an integer-valued sequence from the delta-sigma modulator. As indicated in the figure for the case where the PLL is locked, if the nth rising edge of the reference signal, $v_{\rm ref}(t)$, occurs before that of the divider output, $v_{\rm div}(t)$, the charge pump generates a current pulse of nominal amplitude $I_{\rm CP}$ and duration equal to the time difference between the two edges. Otherwise, the pulse has the same magnitude and duration, but its polarity is reversed.

The input to the delta-sigma modulator is α plus pseudo-random least significant bit dither, $d[n]$, so its output has the form $y[n] = \alpha + d[n] + e_{\Delta\Sigma}[n]$, where $e_{\Delta\Sigma}[n]$ is second-order highpass shaped delta-sigma quantization noise. As proven in [17], the dither prevents $e_{\Delta\Sigma}[n]$ from containing spurious tones that would otherwise show up as spurious tones in the $\Delta\Sigma$-PLL's output.

As shown in [18], the net charge delivered to the loop filter by the charge pump's current pulse each reference period is proportional to the sum of a phase error term and first-order highpass shaped delta-sigma quantization noise. The phase error term is

$$-\theta_{\rm PLL}(\tau_n) + (N + \alpha)\theta_{\rm ref}(t_n) \tag{8}$$

where t_n and τ_n, are the times of the positive-going zero-crossings of $v_{\rm ref}(t)$ and $v_{\rm div}(t)$, respectively, corresponding to the nth charge pump pulse.

The loop bandwidth of the $\Delta\Sigma$-PLL is designed to be low enough that the delta-sigma quantization noise is largely suppressed by the lowpass filtering operation of the loop. Hence, the average output frequency settles to $(N + \alpha)f_{\rm ref}$, as desired, with the delta-sigma quantization noise contributing only a small amount of phase noise.

III. Overview of the FDC-PLL

A. System Description

The proposed FDC-PLL is shown in Fig. 2. It consists of three main components: a $\Delta\Sigma$ FDC, a digital loop controller, and a DCO. The digital loop controller is clocked and the output of the digital loop controller is latched into the DCO on each rising edge of the reference signal.

The $\Delta\Sigma$ FDC consists of a PFD, charge pump, integrating capacitor, 5-level ADC, $2 - z^{-1}$ digital block, and multi-modulus divider. The PFD and charge pump are the same as those in a $\Delta\Sigma$-PLL. As in a $\Delta\Sigma$-PLL, when the FDC-PLL is locked the magnitude of the difference between the time of each rising edge of $v_{\rm div}(t)$ and the time of the corresponding rising edge $v_{\rm ref}(t)$ is a small fraction of the reference oscillator period, $T_{\rm ref}$. Therefore, the charge pump generates a relatively narrow (compared to $T_{\rm ref}$) positive or negative pulse of current around the time of each rising edge of $v_{\rm ref}(t)$. The 5-level ADC is clocked with a delayed version of the reset signal within the PFD, such that it samples the capacitor voltage shortly after each charge pump current pulse settles to zero. The divider in the FDC-PLL is identical to that in a $\Delta\Sigma$-PLL, but its modulus is varied by $v[n] = 2y[n] - y[n-1]$ instead of $y[n]$.

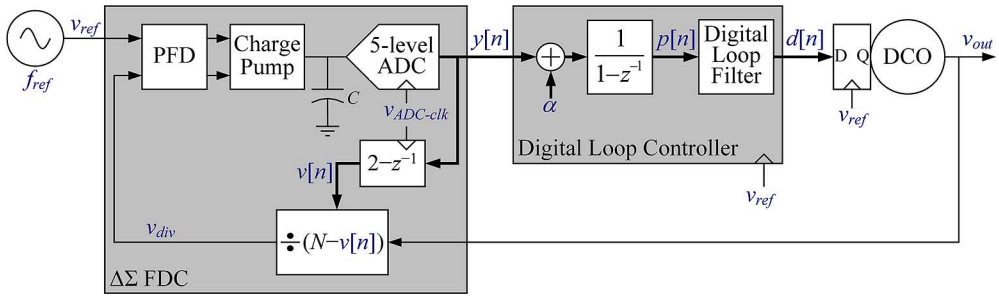

Fig. 2. A delta-sigma FDC based fractional-N PLL (FDC-PLL).

By design, α is restricted to the range

$$-\frac{1}{2} \leq \alpha \leq \frac{1}{2} \tag{9}$$

and the charge pump current, $I_{\rm CP}$, ideally satisfies

$$I_{\rm CP} = (N+\alpha) f_{\rm ref} C \Delta \tag{10}$$

where Δ is the step-size of the 5-level ADC.[1]

As shown in the Appendix, the $\Delta\Sigma$ FDC implicitly implements second-order delta-sigma modulation. In particular, $y[n] + \alpha$ is a measure of the PLL's frequency error plus second-order highpass shaped ADC quantization noise, so it averages to zero when the average DCO frequency is $(N+\alpha) f_{\rm ref}$.

The accumulator in the digital loop controller converts the PLL's frequency error to phase error and reduces the second-order highpass shaped ADC quantization noise to first-order highpass shaped ADC quantization noise. Specifically, as shown in Section IV the output of the accumulator, $p[n]$, consists of the phase error term given by (8) plus first-order highpass shaped ADC quantization noise. Therefore, the properties of $p[n]$ are very similar to those of the sequence of charge pulses delivered by the charge pump to the analog loop filter in the $\Delta\Sigma$-PLL of Fig. 1. Accordingly, the digital loop filter in the FDC-PLL performs the same function as the analog loop filter in the $\Delta\Sigma$-PLL. It suppresses out-of-band quantization noise and circuit error, and sets the loop dynamics.

The DCO is an analog oscillator with a means for the frequency to be controlled by a digital sequence, in this case the output of the digital loop filter, $d[n]$. Depending on the transfer function of the digital loop filter, the required DCO frequency change corresponding to the minimum step-size of $d[n]$ can be very small. A common method of implementing a DCO with a very small minimum frequency step is to quantize $d[n]$ with a digital delta-sigma modulator clocked at a rate much higher than the reference frequency, where the clock signal is obtained by dividing the PLL output signal by a small integer [19]. For each value of $d[n]$, the delta-sigma modulator generates multiple output values with a minimum step-size greater than that of $d[n]$ which are used to modulate the frequency of the DCO. The natural lowpass filtering imposed by the DCO suppresses much of the quantization noise introduced by the delta-sigma modulator, so the effective minimum frequency step of the DCO is that of $d[n]$ at the cost of additive phase noise.

In this paper, any quantization of $d[n]$ performed by the DCO as described above is considered to happen within the DCO, so it is not shown explicitly in Fig. 2. Accordingly, the *DCO phase noise* is defined to be the sum of the phase noise caused by analog oscillator noise and any phase noise caused by quantizing $d[n]$ within the DCO.

B. Digital Loop Filter

Given that the digital loop filter in the FDC-PLL plays the role of the analog loop filter in the $\Delta\Sigma$-PLL, it is reasonable to design the digital loop filter such that it has comparable filtering characteristics to the analog loop filter shown in Fig. 1. This can be achieved with a digital loop filter transfer function of

$$L(z) = L_{\rm PI}(z) L_{\rm LPF}(z) \tag{11}$$

where

$$L_{\rm PI}(z) = K_P + K_I \frac{1}{1-z^{-1}} \tag{12}$$

K_P and K_I are constants called the *proportional path gain* and *integral path gain*, respectively, and $L_{\rm LPF}(z)$ is an all-pole lowpass filter section described shortly [20]. The $L_{\rm PI}(z)$ portion of the filter is often called a proportional-integral filter and is sufficient to obtain a stable feedback system. The $L_{\rm LPF}(z)$ portion of the filter provides attenuation above the PLL bandwidth to reduce phase noise.

Such a digital loop filter has comparable filtering characteristics to the analog loop filter shown in Fig. 1 if $L_{\rm LPF}(z)$ contains a single pole. Unfortunately, neither filter rolls off very sharply with frequency.

In the $\Delta\Sigma$-PLL this problem is often addressed by adding an extra pole outside the PLL bandwidth. Usually, no more than one extra pole is added, though, because of the increased area and power consumption associated with adding multiple extra poles.

In contrast, the incremental area and power consumption associated with adding multiple extra poles to a digital filter tend to be modest. Therefore, the loop filter used in the FDC-PLL analyzed in this paper has a transfer function given by (11) with

$$L_{\rm LPF}(z) = \prod_{i=0}^{3} \frac{\lambda_i}{1-(1-\lambda_i)z^{-1}} \tag{13}$$

[1]As demonstrated in Section IV, deviations of the charge pump current sources on the order of several percent do not significantly degrade the performance of the FDC-PLL. Therefore, since α typically has a magnitude much smaller than N, usually it is reasonable to set $I_{\rm CP} = N f_{\rm ref} C \Delta$.

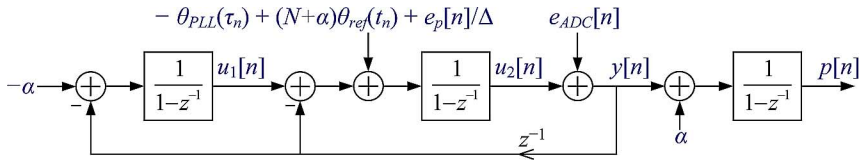

Fig. 3. The implicit second-order delta-sigma modulator implemented by the $\Delta\Sigma$ FDC followed by the α adder and accumulator of the digital loop controller.

where $1-\lambda_i$ for $i=0,1,2$, and 3 are real poles. A design procedure for selecting K_P, K_I, and λ_i for $i=0,1,2$, and 3 in terms of the desired loop bandwidth and phase margin is presented in Section IV.

C. $\Delta\Sigma$-PLL and FDC-PLL Capacitance Comparison

It is mentioned in the Introduction that the capacitance in the loop filter of the $\Delta\Sigma$-PLL tends to be large, often on the order of hundreds of pico-Farads. To sufficiently suppress the delta-sigma quantization error, the loop bandwidth of a fractional-N PLL is usually a small fraction (e.g., several hundredths) of the reference frequency. With the analog loop filter shown in Fig. 1, the loop bandwidth is proportional to $RI_{\rm CP}$, and the total capacitance is approximately inversely proportional to R. Therefore, for any given loop bandwidth, C_1 and C_2 can be reduced by simultaneously increasing R and decreasing $I_{\rm CP}$. Unfortunately, decreasing $I_{\rm CP}$ tends to increase the PLL's phase noise because the loop gain of the $\Delta\Sigma$-PLL's linearized model is proportional to $I_{\rm CP}$ [18]. This places a lower bound on $I_{\rm CP}$ for any given application, which, in turn, typically dictates a large total capacitance when the loop bandwidth is small.

In contrast, as shown in Section IV the loop bandwidth of the FDC-PLL is independent of $I_{\rm CP}$ and C, and the overall phase noise is not a strong function of either $I_{\rm CP}$ or C, so C can be much smaller than the loop filter capacitance in a comparable $\Delta\Sigma$-PLL. For example, $C=1.25$ pF in the FDC-PLL design example presented in Section IV.

IV. The FDC-PLL Linearized Model

A. Model Derivation

It is proven in the Appendix that the $\Delta\Sigma$ FDC behaves as the second-order delta-sigma modulator shown in Fig. 3 along with the α adder and accumulator of the digital loop controller. It is further shown that the output of the accumulator can be written as

$$p[n] = -\theta_{\rm PLL}(\tau_n) + (N+\alpha)\theta_{\rm ref}(t_n) + \frac{e_p[n]}{\Delta} + e_{\Delta\Sigma 1}[n] \quad (14)$$

neglecting a possible constant offset, where $e_p[n]$ represents the combined error from noise and other non-ideal circuit behavior in the charge pump, PFD, and divider,

$$e_{\Delta\Sigma 1}[n] = e_{\rm ADC}[n] - e_{\rm ADC}[n-1] \quad (15)$$

and $e_{\rm ADC}[n]$ is the sum of quantization noise and any additional error from non-ideal circuit behavior in the ADC. As explained in the Appendix, a five-level ADC is necessary and sufficient to ensure that the delta-sigma modulator does not overload when the PLL is locked, which would introduce spurious tones.

The output of the loop filter, $d[n]$, is latched into the DCO on each positive-going zero-crossing of $v_{\rm ref}(t)$, so $d[n-1]$ is applied to the DCO during the time interval $t_n < t \le t_{n+1}$ for each positive integer n. It is assumed that the DCO's control word latency is negligible, so its instantaneous frequency during each time interval $t_n < t \le t_{n+1}$ is

$$f_{\rm PLL}(t) = f_c + K_{\rm DCO} d[n-1] + \psi_{\rm DCO}(t) \quad (16)$$

where f_c is the nominal center frequency of the DCO in Hz, $K_{\rm DCO}$ is the DCO gain in Hz, and $\psi_{\rm DCO}(t)$ is the DCO's instantaneous frequency error.[2] It follows from (4) and (16) that during the time interval $t_n < t \le t_{n+1}$ the FDC-PLL's instantaneous frequency error can be written as

$$\psi_{\rm PLL}(t) = f_c - (N+\alpha) f_{\rm ref} + K_{\rm DCO} d[n-1] + \psi_{\rm DCO}(t) \quad (17)$$

The ideal output frequency when the FDC-PLL is locked is $(N+\alpha)f_{\rm ref}$, so $d[n]$ can be written as

$$d[n] = \frac{1}{K_{\rm DCO}}[(N+\alpha)f_{\rm ref} - f_c] + f[n] \quad (18)$$

where $f[n]$ is the zero-mean component of $d[n]$. It follows from (17) and (18) that

$$\psi_{\rm PLL}(t) = K_{\rm DCO} f[n-1] + \psi_{\rm DCO}(t) \quad (19)$$

during the time interval $t_n < t \le t_{n+1}$ for each positive integer n.

Integrating (19) from time t_0 to t where $t_n < t \le t_{n+1}$ gives

$$\theta_{\rm PLL}(t) = K_{\rm DCO} \sum_{k=1}^{n-1} (t_{k+1} - t_k) f[k-1] + K_{\rm DCO} f[n-1](t - t_n) + \theta_{\rm DCO}(t) \quad (20)$$

where

$$\theta_{\rm DCO}(t) = \int_{t_0}^{t} \psi_{\rm DCO}(u)\,du \quad (21)$$

is the instantaneous phase noise introduced by the DCO. Typical reference oscillators have high spectral purity, so

$$t_{k+1} - t_k \cong T_{\rm ref} \quad (22)$$

[2]The *DCO Gain* is defined as the amount by which the DCO frequency changes when $d[n]$ changes by unity.

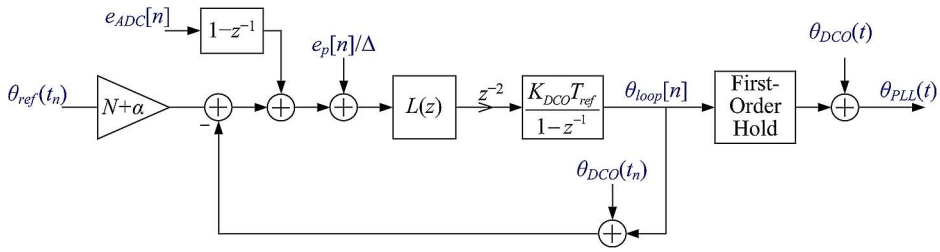

Fig. 4. Phase noise model of the FDC-PLL.

holds to a high degree of accuracy. Hence, (20) implies that $\theta_{\rm PLL}(t)$ can be written as

$$\theta_{\rm PLL}(t) = K_{\rm DCO}T_{\rm ref}\sum_{k=1}^{n-1} f[k-1] + K_{\rm DCO}f[n-1](t-t_n) + \theta_{\rm DCO}(t) \quad (23)$$

for $t_n < t \le t_{n+1}$ which can be rewritten as

$$\theta_{\rm PLL}(t) = \theta_{\rm DCO}(t) + (\theta_{\rm loop}[n+1] - \theta_{\rm loop}[n])\frac{(t-t_n)}{T_{\rm ref}} + \theta_{\rm loop}[n] \quad (24)$$

where

$$\theta_{\rm loop}[n] = K_{\rm DCO}T_{\rm ref}\sum_{k=1}^{n-1} f[k-1]. \quad (25)$$

The second and third term in (24) represent a linear interpolation between the nth and $(n+1)$th samples of $\theta_{\rm loop}[n]$. This type of interpolation is called *first-order hold* interpolation [21]. To extend (24) to hold for any $t > t_0$, the first-order hold component can be written as a sequence of triangular time pulses with amplitudes $\theta_{\rm loop}[n]$, i.e.,

$$\theta_{\rm PLL}(t) = \theta_{\rm DCO}(t) + \sum_{n=0}^{\infty}\theta_{\rm loop}[n]h_{\rm tri}(t - nT_{\rm ref} - t_0) \quad (26)$$

for arbitrary $t > t_0$, where

$$h_{\rm tri}(t) = \begin{cases} 1 - \frac{|t|}{T_{\rm ref}} & \text{if } |t| < T_{\rm ref}, \\ 0 & \text{otherwise.} \end{cases} \quad (27)$$

The bandwidth of a practical PLL is much smaller than the reciprocal of the maximum magnitude of the difference between τ_n and t_n, so

$$\theta_{\rm PLL}(\tau_n) \cong \theta_{\rm PLL}(t_n) \quad (28)$$

holds to a high degree of accuracy. Hence (24) yields

$$\theta_{\rm PLL}(\tau_n) \cong \theta_{\rm DCO}(t_n) + \theta_{\rm loop}[n]. \quad (29)$$

Combining (14), (15), (25), (26), and (29) results in the linearized model shown in Fig. 4 where the sample-rate of the discrete-time blocks and the first-order hold interpolator is $f_{\rm ref}$. The discrete-time portion of the model implements the FDC-PLL's feedback system and generates $\theta_{\rm loop}[n]$, which is linearly interpolated by the first-order hold block as described above.

It follows from Fig. 4 that the discrete-time loop gain of the FDC-PLL is

$$T(z) = K_{\rm DCO}T_{\rm ref}L(z)\frac{z^{-2}}{1-z^{-1}} \quad (30)$$

and the various FDC-PLL discrete-time transfer functions are

$$\frac{\theta_{\rm loop}}{\theta_{\rm ref}}(z) = (N+\alpha)\frac{T(z)}{1+T(z)} \quad (31)$$

$$\frac{\theta_{\rm loop}}{\theta_{\rm DCO}}(z) = -\frac{T(z)}{1+T(z)} \quad (32)$$

$$\frac{\theta_{\rm loop}}{e_{\rm ADC}}(z) = (1-z^{-1})\frac{T(z)}{1+T(z)} \quad (33)$$

and

$$\frac{\theta_{\rm loop}}{e_p}(z) = \frac{1}{\Delta}\left(\frac{T(z)}{1+T(z)}\right). \quad (34)$$

These equations describe the loop dynamics of the FDC-PLL.

B. Phase Noise PSD Calculation

It is assumed that the noise signals $\theta_{\rm ref}(t_n)$, $e_{\rm ADC}[n]$, $e_p[n]$, and $\theta_{\rm DCO}(t)$ can be modeled as uncorrelated, zero-mean, wide-sense stationary random processes, so the PSD of $\theta_{\rm PLL}(t)$ is the sum of PSD components that each correspond to one of the noise signals. Likewise, the discrete-time PSD of $\theta_{\rm loop}[n]$ is the sum of the discrete-time PSD components that each correspond to one of the noise signals.

It follows from (31) that the component of the discrete-time PSD of $\theta_{\rm loop}[n]$ corresponding to $\theta_{\rm ref}(t_n)$ is

$$S_{\theta_{\rm ref}}(e^{j2\pi T_{\rm ref}f})\left|(N+\alpha)\frac{T(e^{j2\pi T_{\rm ref}f})}{1+T(e^{j2\pi T_{\rm ref}f})}\right|^2 \quad (35)$$

where $S_{\theta_{\rm ref}}(e^{j2\pi T_{\rm ref}f})$ is the discrete-time PSD of $\theta_{\rm ref}(t_n)$. The continuous-time Fourier transform of the output of a first-order hold interpolator with input $u[n]$ and sample-rate $f_{\rm ref}$ is

$$U(e^{j2\pi T_{\rm ref}f})T_{\rm ref}\left[\frac{\sin(\pi T_{\rm ref}f)}{\pi T_{\rm ref}f}\right]^2 \quad (36)$$

where $U(e^{j2\pi T_{\rm ref} f})$ is the discrete-time Fourier transform of $u[n]$ [21]. Therefore, the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to $\theta_{\rm ref}(t_n)$ is

$$S_{\theta_{\rm ref}}(e^{j2\pi T_{\rm ref} f}) T_{\rm ref} \left| \frac{(N+\alpha) T(e^{j2\pi T_{\rm ref} f})}{1 + T(e^{j2\pi T_{\rm ref} f})} \right|^2 \times \left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f} \right]^4. \quad (37)$$

By similar reasoning, the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to $e_p[n]$ is

$$S_{e_p}(e^{j2\pi T_{\rm ref} f}) \frac{T_{\rm ref}}{\Delta^2} \left| \frac{T(e^{j2\pi T_{\rm ref} f})}{1 + T(e^{j2\pi T_{\rm ref} f})} \right|^2 \left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f} \right]^4 \quad (38)$$

where $S_{e_p}(e^{j2\pi T_{\rm ref} f})$ is the discrete-time PSD of $e_p[n]$.

As described in the Appendix, $e_{\rm ADC}[n]$ is asymptotically white and uniformly distributed between -0.5 and 0.5, so the discrete-time PSD of $e_{\rm ADC}[n]$ is 1/12. It follows from reasoning similar to that which led to (37) and (38) that the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to $e_{\rm ADC}[n]$ is

$$\frac{T_{\rm ref}}{3} \sin^2(\pi T_{\rm ref} f) \left| \frac{T(e^{j2\pi T_{\rm ref} f})}{1 + T(e^{j2\pi T_{\rm ref} f})} \right|^2 \left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f} \right]^4 \quad (39)$$

in units of cycles squared per Hz. If the desired units of the PSD are radians squared per Hz, then (39) must be scaled by $4\pi^2$.

The component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to DCO phase noise depends on both $\theta_{\rm DCO}(t)$ and $\theta_{\rm DCO}(t_n)$, which are obviously correlated. Consequently, the effects of $\theta_{\rm DCO}(t)$ and $\theta_{\rm DCO}(t_n)$ must be considered together when calculating the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to DCO noise.

The component of $\theta_{\rm loop}[n]$ corresponding to DCO noise is $\theta_{\rm DCO}(t_n)$ filtered by the discrete-time lowpass transfer function (32). As implied by (36), the first-order hold interpolator imposes a continuous-time lowpass filtering operation on this signal component that rolls off in frequency at 40 dB per decade. As shown in Fig. 4, $\theta_{\rm DCO}(t)$ is added to the output of the first-order hold interpolator and for a typical DCO the PSD of $\theta_{\rm DCO}(t)$ rolls off in frequency by no more than 20 dB per decade (except at low frequencies where $1/f$ noise is significant). Therefore, in calculating the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to DCO noise, the output of the first-order hold interpolator can be neglected for frequencies above $f_{\rm ref}/2$ with a high degree of accuracy.

It follows that the effect of adding $\theta_{\rm DCO}(t_n)$ in the feedback loop of Fig. 4 is practically equivalent to adding $\theta_{\rm DCO}(t)$ filtered by

$$-\frac{T(e^{j2\pi T_{\rm ref} f})}{1 + T(e^{j2\pi T_{\rm ref} f})} \left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f} \right]^2 \quad (40)$$

to the output of the first-order hold interpolator. This result relies on the reasonable assumption that aliasing error in $\theta_{\rm DCO}(t_n)$ within the passband of (32) is negligible. It follows that the component of the PSD of $\theta_{\rm PLL}(t)$ corresponding to DCO noise is

$$S_{\theta_{\rm DCO}}(f) \left| 1 - \frac{T(e^{j2\pi T_{\rm ref} f})}{1 + T(e^{j2\pi T_{\rm ref} f})} \left[\frac{\sin(\pi T_{\rm ref} f)}{\pi T_{\rm ref} f} \right]^2 \right|^2 \quad (41)$$

where $S_{\theta_{\rm DCO}}(f)$ is the continuous-time PSD of $\theta_{\rm DCO}(t)$.

The PSD of $\theta_{\rm PLL}(t)$ from all of the FDC-PLL noise sources is the sum of (37), (38), (39), and (41). Typically, estimates of $S_{\theta_{\rm ref}}(e^{j2\pi T_{\rm ref} f})$, $S_{e_p}(e^{j2\pi T_{\rm ref} f})$, and $S_{\theta_{\rm DCO}}(f)$ are obtained via circuit simulation. As described in Section II, the DCO phase noise is the combination of phase noise introduced by the underlying analog oscillator and any quantization of $d[n]$, so circuit simulations used to estimate the DCO phase noise PSD must include any such quantization noise.

C. Loop Filter Design

The loop filter transfer function, $L(z)$, determines the FDC-PLL's loop bandwidth, phase margin, and noise filtering characteristics. In analogy to a conventional $\Delta\Sigma$-PLL, the FDC-PLL's phase noise consists of highpass filtered DCO noise, i.e., (41), and lowpass filtered noise from the reference oscillator, ADC, divider, PFD, and charge pump, i.e., (37)–(39). The design objective for $L(z)$ is to strike a compromise among these noise filtering operations appropriate to the application's requirements while maintaining a given desired loop bandwidth and phase margin.

In a $\Delta\Sigma$-PLL, having a zero-frequency pole in the loop filter ensures the charge pump output current pulse sequence has zero mean, which simplifies the design of both the charge pump and PFD [4]. In contrast, the delta-sigma modulator relationship derived in the Appendix implies that in the FDC-PLL the charge pump output current pulse sequence has zero mean regardless of whether the loop filter has a zero-frequency pole. Therefore, a major reason for having a zero-frequency loop filter pole in $\Delta\Sigma$-PLLs does not apply to the FDC-PLL.

Nevertheless, there are still advantages to having a zero-frequency pole in an FDC-PLL's loop filter. One advantage is that it causes the transfer function portion of (41) to have a second zero-frequency zero. DCO phase noise typically has a PSD proportional to $1/f^3$ for $0 < f < f_c$ where f_c is the frequency below which $1/f$ noise is significant. Having two zero-frequency zeros in the transfer function portion of (41) prevents the portion of the PSD proportional to $1/f^3$ from contributing significantly to the overall FDC-PLL phase noise. Another advantage is that the zero-frequency pole eliminates the dependence of $\theta_{\rm PLL}(t)$ on the DCO's center frequency and gain, which both vary with process, supply voltage, and temperature.

The primary disadvantage of having a zero-frequency pole in the loop filter is that it introduces negative phase into the loop gain which limits the achievable sharpness of the filter's transition band for a given phase margin. Therefore, in some applications not having a zero-frequency pole in the loop filter may offer an advantage with respect to minimizing phase noise.

Unlike the case of an analog PLL, there is a great deal of flexibility in the choice of $L(z)$, regardless of whether it has a zero-frequency pole. The remainder of this section evaluates the practical choice of $L(z)$ given by (11) with (12) and (13), which includes a zero-frequency pole.

A reasonable design procedure is to first choose values of K_P and K_I via the equations derived below that result in the desired loop bandwidth and phase margin to the extent that

$$|L_{\rm LPF}(e^{j2\pi T_{\rm ref} f_u})|^2 \cong 1 \quad \text{and} \quad 2\pi T_{\rm ref} f_u \ll 1 \tag{42}$$

where f_u is the unity-gain frequency of the FDC-PLL's loop gain. This requires that the poles of $L_{\rm LPF}(z)$ be initially chosen such that

$$2\pi T_{\rm ref} f_u \ll \lambda_i < 1. \tag{43}$$

Then a trial and error procedure can be used in which the λ_i values are reduced to improve noise suppression while the K_P and K_I values are adjusted to maintain the desired loop bandwidth and phase margin.

By definition, the unity gain frequency of the FDC-PLL's loop gain, f_u, satisfies

$$|T(e^{j2\pi T_{\rm ref} f_u})|^2 = 1. \tag{44}$$

It can be verified from (12), (30), and (42) that

$$f_u \cong \frac{K_{\rm DCO}}{2\pi}\sqrt{\frac{K}{2}}\sqrt{1+\sqrt{1+\frac{4K_I^2}{(K_{\rm DCO}T_{\rm ref})^2K^2}}} \tag{45}$$

where

$$K \triangleq K_P(K_P + K_I). \tag{46}$$

Typically, $K_P \gg K_I$ in which case (45) reduces to

$$f_u \cong \frac{K_{\rm DCO}K_P}{2\pi} \tag{47}$$

Furthermore,

$$\left|\frac{T(e^{j2\pi T_{\rm ref} f_u})}{1+T(e^{j2\pi T_{\rm ref} f_u})}\right|^2 \left[\frac{\sin(\pi T_{\rm ref} f_u)}{\pi T_{\rm ref} f_u}\right]^4 \cong \frac{1}{2} \tag{48}$$

given $2\pi T_{\rm ref} f_u \ll 1$, so the FDC-PLL's loop bandwidth, $f_{\rm BW}$, is approximately given by

$$f_{\rm BW} \cong f_u. \tag{49}$$

The FDC-PLL's phase margin in radians is

$$PM = \pi + \measuredangle T(e^{j2\pi T_{\rm ref} f_u}). \tag{50}$$

With (11), (12), (30), (42), and (45), this can be written as

$$PM = \pi + \tan^{-1}\left(\frac{K_P \sin(2\pi T_{\rm ref} f_u)}{K_I + K_P[1-\cos(2\pi T_{\rm ref} f_u)]}\right) - 2\tan^{-1}\left(\frac{\sin(2\pi T_{\rm ref} f_u)}{1-\cos(2\pi T_{\rm ref} f_u)}\right) - 4\pi T_{\rm ref} f_u. \tag{51}$$

TABLE I
PARAMETERS AND EVALUATION SETTINGS OF THE EXAMPLE FDC-PLL DESIGN

Design Parameters and Evaluation Settings	Value
f_{ref}	26 MHz
f_{PLL}	3588.026 MHz
N	138
α	0.001
K_{DCO}	24 kHz
V_{DD}	1.0 V
Δ	80 mV
ADC Input Range	0.3-0.7 V
C	1.25 pF
I_{CP}	359 μA
I_{OC}	$-I_{CP}$
T_{OC}	2 ns
T_{DZ}	1 ns
K_P	$2^{-7}f_{ref}/K_{DCO}$
K_I	$2^{-17}f_{ref}/K_{DCO}$
$\lambda_0, \lambda_1, \lambda_2, \lambda_3$	$2^{-2}, 2^{-2}, 2^{-3}, 2^{-4}$
Loop-filter Word Width	32 bits
DCO Input Word Width	14 bits
DCO's ΔΣ Modulator Input Word Width	8 bits
DCO's ΔΣ Modulator Update Rate	$f_{PLL}/16$

It follows from the above analysis that for fixed $K_{\rm DCO}$ and $T_{\rm ref}$ the loop bandwidth depends primarily on K_P and for fixed $K_{\rm DCO}, T_{\rm ref}$, and loop bandwidth the phase margin depends primarily on K_I. Therefore, it is straightforward to choose K_I and K_P using (47), (49), and (51) to achieve a desired loop bandwidth and phase margin provided (42) holds. Then, a trial and error process can be applied in which the λ_i values are reduced to improve phase noise suppression and K_I and K_P are increased to maintain the desired loop bandwidth and phase margin. The trial and error process is guided by plotting (37), (38), (39), and (41) at each iteration.

V. DESIGN EXAMPLE

The design methodology described above has been applied to select the example FDC-PLL design parameters presented in Table I. This section applies the linearized model to calculate the example FDC-PLL's expected performance with realistic input noise levels, and compares the calculated performance to the performance predicted by computer simulation. The example was chosen because it is suitable for use as a carrier synthesizer for the widely-used GSM mobile handset standard and facilitates comparison with previously published TDC-based PLLs [7], [10].

To apply the linearized model to calculate the FDC-PLL's output phase noise PSD, i.e., the PSD of $\theta_{\rm PLL}(t)$, the PSDs of the input noise sources $\theta_{\rm DCO}(t)$, $\theta_{\rm ref}(t_n)$, and $e_p[n]$ must be known or estimated. In this example, the input noise sources are estimated to be in line with what can be achieved in a 65 nm CMOS process with a 1 V power supply. The simulated DCO is identical to that presented in [19], so $\theta_{\rm DCO}(t)$, which includes both DCO quantization noise and analog noise, is taken to have

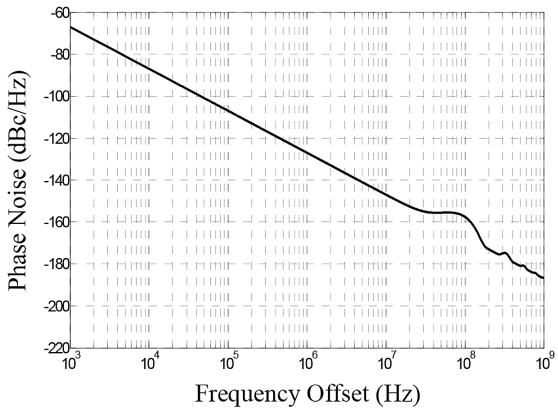

Fig. 5. PSD of $\theta_{\rm DCO}(t)$ used in the design and simulation of the FDC-PLL example.

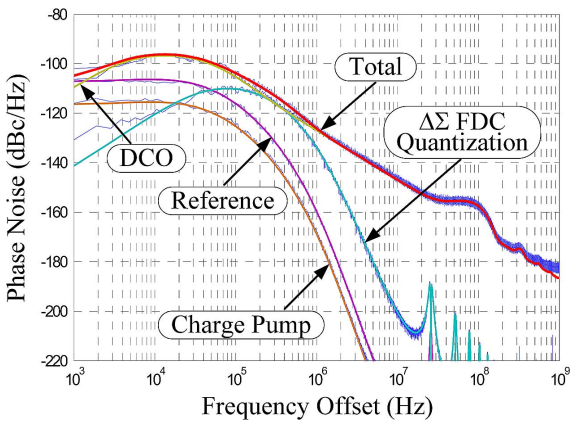

Fig. 6. Calculated PSD plots (smooth curves) and simulated PSD plots (jagged curves) of the FDC-PLL output phase noise resulting from each of the noise sources individually and all together.

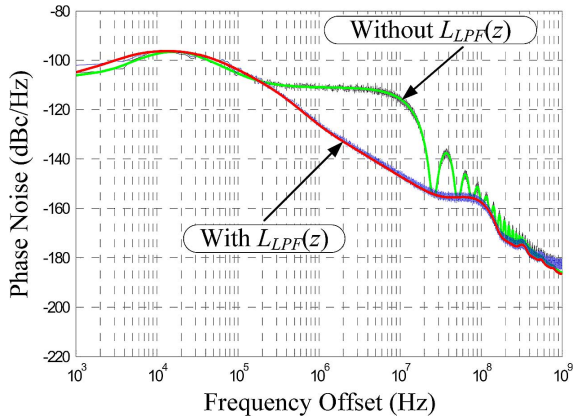

Fig. 7. Calculated and simulated PSD plots of the FDC-PLL output phase noise with all noise sources with and without the $L_{\rm LPF}(z)$ portion of the loop filter.

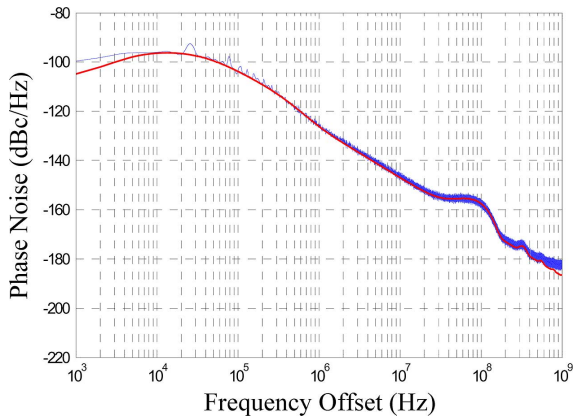

Fig. 8. Calculated PSD plot of the FDC-PLL output phase noise with all noise sources, and the corresponding simulated PSD with several non-ideal circuit effects taken into account in addition to noise.

a PSD consistent with the results presented in [19] as shown in Fig. 5. The $\theta_{\rm ref}(t_n)$ and $e_p[n]$ input noise source levels were estimated via periodic steady-state (PSS) circuit simulations of transistor-level reference buffer, divider, PFD, and charge pump circuits.

PSS simulation of the reference buffer indicates that $\theta_{\rm ref}(t)$ can be modeled as white noise with a PSD level of -150 dBc/Hz. Therefore, the discrete-time PSD level of $\theta_{\rm ref}(t_n)$ is $-150 - 10\log_{10}(T_{\rm ref}) = -76$ dBc.

Simulations indicate that $e_p[n]$ is dominated by the charge pump, which has the form of the single-ended design presented in [22]. The quantization step-size of the ADC is 80 mV. Its input voltage, and, therefore, the output voltage of the charge pump, ranges from 0.3 V to 0.7 V. The choices of C and $I_{\rm CP}$ are related via (10), and for this example design they are 1.25 pF and 359 μA, respectively. Additionally, $I_{\rm OC} = -I_{\rm CP}$ ($I_{\rm OC}$ is defined in the Appendix) and $T_{\rm OC} = 2$ ns. PSS simulations of the charge pump and offset current circuitry indicate that $e_p[n]$ can be modeled as white noise with a discrete-time PSD level of -64 dBV.

All the PSD plots in Figs. 6 through 8 were obtained with the input noise source levels described above. The calculated PSD plots shown in the figures where obtained via (37), (38), (39), and (41). The simulated PSD plots shown in the figures where obtained via an event-driven C-language simulator. The simulator calculates the times of successive events, which include the positive-going zero crossings of $v_{\rm ref}(t)$, $v_{\rm div}(t)$, and $v_{\rm out}(t)$, the sample times of the 5-level ADC, and the desired output sample times of the $\theta_{\rm PLL}(t)$. Each event time is calculated as a function of the FDC-PLL's state variables, and the state variables are updated at each event time.

Fig. 6 shows the simulated and calculated PSD of $\theta_{\rm PLL}(t)$ for several cases.[3] In one of the cases all of the noise sources presented above are considered together. In each of the other cases, only one of the noise sources is considered with all the other noise sources set to zero. Therefore, the figure shows how each noise source contributes to the total FDC-PLL output phase noise.

Fig. 7 shows the simulated and calculated PSD of $\theta_{\rm PLL}(t)$ for two cases to demonstrate the effect of the $L_{\rm LPF}(z)$ portion of the FDC-PLL's loop filter. One case is that shown in Fig. 6 for all the noise sources acting together. The other case differs only in that the simulation and calculations were made with $L_{\rm LPF}(z)$ effectively disabled by setting its λ_i coefficients to 1, and K_I and K_P adjusted to maintain approximately the same phase margin and bandwidth as the first case.

Fig. 8 shows the effect of typical non-ideal circuit behavior. The smooth curve is the same calculated PSD of $\theta_{\rm PLL}(t)$ shown

[3]In each plot, the smooth curves represent the calculated PSDs, and the jagged curves represent simulated PSDs.

in Fig. 6 for all the noise sources acting together. The jagged curve is the corresponding simulated PSD but with several non-ideal circuit effects taken into account in addition to noise. The non-ideal circuit effects involve the charge pump, offset current, sampling capacitor, and 5-level ADC. The magnitudes of the positive and negative charge pump current sources were increased and decreased, respectively, by 5%, and the offset current magnitude was decreased by 5%. A capacitor leakage current of -200 nA per reference period was introduced. Randomly chosen errors of 10 mV, -5 mV, 6 mV, and -8 mV, respectively, were introduced into the ADC threshold voltages. The errors were made larger than would be expected in practice to demonstrate the robustness of the FDC-PLL architecture.

The simulated and calculated results presented in Figs. 6 and 7 demonstrate that the linearized model accurately predicts the expected phase noise performance of the example FDC-PLL for the considered evaluation settings. Furthermore, the simulation results presented in Fig. 8 suggest that the FDC-PLL is robust with respect to non-ideal circuit behavior. Numerous additional FDC-PLL design parameters and evaluation cases considered by the authors have yielded consistently positive results.

APPENDIX

This Appendix proves that the $\Delta\Sigma$ FDC followed by the α adder and accumulator in the digital loop controller perform the signal processing operations shown in Fig. 3. It also applies known delta-sigma modulator results to draw various conclusions about the quantization noise introduced by the 5-level ADC.

The derivation consists of four parts. The first two parts derive expressions for the positive-going zero-crossing times of the reference oscillator and the divider output, respectively. The third part derives an expression for the voltage across the capacitor at the output of the charge pump. The fourth part combines the results of the previous parts to show that the ADC's quantization noise is that of a second-order delta-sigma modulator.

A. Reference Oscillator Zero-Crossing Time Derivation

Recall that t_k, for $k = 0, 1, 2, \ldots$, are the times of consecutive positive-going zero-crossings of the reference oscillator signal, $v_{\rm ref}(t)$. The phase in cycles of an oscillator at each of its positive-going zero crossings is integer-valued, so the definition of t_k implies that the phase of the reference oscillator at time t_k is

$$p_{\rm ref}(t_k) = k \tag{52}$$

for all non-negative integers k.

Exactly one reference oscillator cycle occurs during the time interval $t_{k-1} < t \leq t_k$, so it follows from (2) and (52) that

$$t_k - t_{k-1} = \frac{1 - \psi_{\rm ref}[k]}{f_{\rm ref}} \tag{53}$$

where

$$\psi_{\rm ref}[k] = \theta_{\rm ref}(t_k) - \theta_{\rm ref}(t_{k-1}) \tag{54}$$

is the change in the reference oscillator's instantaneous phase noise in cycles between times t_{k-1} and t_k.[4] Summing (53) from $k = 1$ through any positive integer n yields

$$t_n = t_0 + \frac{1}{f_{\rm ref}} \sum_{k=1}^{n} (1 - \psi_{\rm ref}[k]). \tag{55}$$

B. Divider Output Zero-Crossing Time Derivation

Recall that τ_k, for each $k = 0, 1, 2, \ldots$, is the time of the positive-going zero-crossing of the FDC-PLL's output signal, $v_{\rm out}(t)$, that triggers the kth rising edge of the divider output, $v_{\rm div}(t)$. Without loss of generality, assume that τ_k is indexed such that

$$p_{\rm PLL}(\tau_0) = 0. \tag{56}$$

The kth output value of the 5-level ADC, $y[k]$, is a digitized sample of the charge pump capacitor voltage sampled after time τ_k, but well before time τ_{k+1}, and it follows from Fig. 2 that

$$v[k] = 2y[k] - y[k-1]. \tag{57}$$

Therefore, the kth sample of $v[k]$ is available prior to time τ_{k+1}. The divider modulus is immediately updated when the sample is available such that exactly $N - v[k]$ DCO cycles occur during the time interval $\tau_k < t \leq \tau_{k+1}$. The definition of τ_k implies that

$$p_{\rm PLL}(\tau_k) - p_{\rm PLL}(\tau_{k-1}) = N - v[k-1]. \tag{58}$$

It follows from (5) and (58) that

$$\tau_k - \tau_{k-1} = \frac{N - v[k-1] - \psi_{\rm PLL}[k]}{(N+\alpha) f_{\rm ref}} \tag{59}$$

where

$$\psi_{\rm PLL}[k] = \theta_{\rm PLL}(\tau_k) - \theta_{\rm PLL}(\tau_{k-1}) \tag{60}$$

is the change in the FDC-PLL's instantaneous output phase noise in cycles over the interval $\tau_{k-1} < t \leq \tau_k$. Summing (59) from $k = 1$ through any positive integer n yields

$$\tau_n = \tau_0 + \frac{1}{(N+\alpha) f_{\rm ref}} \sum_{k=1}^{n} (N - v[k-1] - \psi_{\rm PLL}[k]). \tag{61}$$

C. Charge Pump Output Derivation

Subtracting (55) from (61) gives

$$\tau_n - t_n = \tau_0 - t_0 + \frac{1}{(N+\alpha) f_{\rm ref}} \sum_{k=1}^{n} (x[k] - v[k-1]) \tag{62}$$

[4]Note that $\psi_{\rm ref}[n]$ is a different function than $\psi_{\rm ref}(t)$, but they are related in that $\psi_{\rm ref}[n]$ is proportional to the average of $\psi_{\rm ref}(t)$ over the nth reference period. The functions $\psi_{\rm PLL}[n]$ and $\psi_{\rm PLL}(t)$ are similarly distinct.

where

$$x[k] = -\alpha - \psi_{\rm PLL}[k] + (N+\alpha)\psi_{\rm ref}[k]. \tag{63}$$

The $-\alpha$ term in $x[n]$ can be interpreted as the phase change in cycles over one reference period of an ideal oscillator of frequency $Nf_{\rm ref}$ minus that of the ideal output of the FDC-PLL. The definitions of $\psi_{\rm ref}[k]$ and $\psi_{\rm PLL}[k]$ imply that the average value of $x[k]+\alpha$ is zero when the FDC-PLL is locked, and that $(x[k]+\alpha)/T_{\rm ref}$ is a measure of the average over the kth reference period of the difference between $(N+\alpha)$ times the instantaneous frequency of the reference oscillator and the instantaneous frequency of the output signal.

It follows from (5) and (56) that

$$\tau_0 - t_0 = -\frac{\theta_{\rm PLL}(\tau_0)}{(N+\alpha)f_{\rm ref}}. \tag{64}$$

Substituting (57) and (64) into (62) gives

$$\begin{aligned}(\tau_n - t_n)(N+\alpha)f_{\rm ref} &= -y[n-1] \\ &+ \sum_{k=1}^{n}(x[k]-y[k-1]) \\ &+ y[-1] - \theta_{\rm PLL}(\tau_0).\end{aligned} \tag{65}$$

Suppose the FDC-PLL is locked for all $t \geq t_0$ so that

$$|\tau_n - t_n| < T_{\rm ref} \tag{66}$$

for all $n \geq 0$, where $T_{\rm ref} = 1/f_{\rm ref}$ is the nominal period of the reference oscillator. If the PFD and charge pump are as shown in Fig. 1, then in the absence of non-ideal circuit behavior the output of the charge pump is a sequence of current pulses given by

$$i_{\rm cp}(t) = \begin{cases} I_{\rm CP} & \text{when } t_n \leq t \leq \tau_n \\ -I_{\rm CP} & \text{when } \tau_n \leq t \leq t_n \\ 0 & \text{otherwise} \end{cases} \tag{67}$$

for all positive integers n. An additional current pulse of fixed duration and fixed (positive or negative) amplitude may also be included in $i_{\rm cp}(t)$ each reference period to reduce nonlinear distortion introduced by the PFD and charge pump [23], [24].

The ADC samples the capacitor voltage each reference period shortly after the charge pump current sources settle to zero. Let $V_c[n]$ be the voltage sampled by the ADC during the nth reference period minus the midscale voltage of the ADC (i.e., $V_c[n]=0$ corresponds to the middle of the ADC's input range). The operation of the charge pump implies that

$$V_c[n] = V_c[n-1] + (\tau_n - t_n)\frac{I_{\rm CP}}{C} + T_{\rm OC}\frac{I_{\rm OC}}{C} + e_p[n] \tag{68}$$

where $T_{\rm OC}$ and $I_{\rm OC}$ are the duration and amplitude, respectively, of the additional current pulse if it is used (otherwise $I_{\rm OC}=0$), and $e_p[n]$ represents the combined error from noise and other non-ideal circuit behavior in the charge pump, PFD, and divider. Each sample of $e_p[n]$ is the result of error in the amount of charge in the current pulses integrated onto the capacitor during the nth reference period.

Substituting (10) and (65) into (68) results in

$$\begin{aligned}\frac{V_c[n]}{\Delta} = \frac{V_c[n-1]}{\Delta} - y[n-1] + \sum_{k=1}^{n}(x[k]-y[k-1]) \\ + y[-1] - \theta_{\rm PLL}(\tau_0) + \theta_{\rm offset} + \frac{e_p[n]}{\Delta}\end{aligned} \tag{69}$$

where

$$\theta_{\rm offset} = T_{\rm OC}\frac{I_{\rm OC}}{C\Delta}. \tag{70}$$

D. Delta-Sigma Modulator Equivalence and Implications

The output of the ADC, $y[n]$, can take on values from the set $\{-2,-1,0,1,2\}$ and can be written as

$$y[n] = \frac{1}{\Delta}V_c[n] + e_{\rm ADC}[n] \tag{71}$$

where $e_{\rm ADC}[n]$ is the sum of quantization noise and any additional error from non-ideal circuit behavior in the ADC. The ADC has only five levels, so its quantization is very coarse. Therefore, it is assumed that the only non-negligible component of $e_{\rm ADC}[n]$ is quantization noise, so the nth output sample of the ADC is taken to be $V_c[n]/\Delta$ rounded to the nearest integer when

$$-2.5\Delta \leq V_c[n] < 2.5\Delta \tag{72}$$

and -2 or 2, respectively, when $V_c[n]$ is less than -2.5Δ, or greater than or equal to 2.5Δ.

Equations (69) and (71) are equivalent to the block diagram shown in Fig. 3 to the left of the α adder for $n=1,2,3,\ldots$, where

$$u_2[n] = \frac{V_c[n]}{\Delta} \tag{73}$$

and the initial condition on $u_1[n]$ is

$$u_1[0] = y[-1] - \theta_{\rm PLL}(\tau_0) + \theta_{\rm offset}. \tag{74}$$

The block diagram has the well-known form of a second-order delta-sigma modulator, so its output can be written as

$$y[n] = x[n] + \frac{e_p[n] - e_p[n-1]}{\Delta} + e_{\Delta\Sigma 2}[n] \tag{75}$$

where

$$e_{\Delta\Sigma 2}[n] = e_{\rm ADC}[n] - 2e_{\rm ADC}[n-1] + e_{\rm ADC}[n-2] \tag{76}$$

is second-order highpass shaped quantization noise [25], [26].

If (72) is satisfied for a given integer n, then $e_{\rm ADC}[n]$ is the quantization noise caused by rounding $u_2[n]$ to the nearest integer. In this case the delta-sigma modulator is said to be non-overloading at time n. Otherwise, the delta-sigma modulator is said to be overloaded at time n. If the delta-sigma modulator is non-overloading for all $n=1,2,3,\ldots$, then $e_{\rm ADC}[n]$ is asymptotically white and uniformly distributed between -0.5 and 0.5 under the realistic assumption that $x[n]$ contains a small amount

of independent random noise [27]. In contrast, if the delta-sigma modulator becomes overloaded, then $e_{\rm ADC}[n]$ becomes correlated with $x[n]$, its variance increases, and it often contains spurious tones. Hence, for best phase noise performance it is desirable to keep the delta-sigma modulator non-overloading once the FDC-PLL is locked.

Sufficient conditions for the delta-sigma modulator to be non-overloading for $n = 1, 2, 3, \ldots$ are that it is non-overloading for $n = 1$ and $n = 2$, and

$$\left| x[n] + \frac{e_p[n] - e_p[n-1]}{\Delta} \right| \leq 1 \tag{77}$$

for $n = 3, 4, 5, \ldots$. The proof of this result is as follows. It can be verified from Fig. 3 that

$$u_2[k] = x[k] + \frac{e_p[k] - e_p[k-1]}{\Delta} - 2e_{\rm ADC}[k-1] + e_{\rm ADC}[k-2] \tag{78}$$

If the delta-sigma modulator is non-overloading for $n = k-1$ and $n = k-2$, then $e_{\rm ADC}[k-1]$ and $e_{\rm ADC}[k-2]$ are each bounded in magnitude by 0.5, so (73) and (78) imply that

$$|V_c[k]| \leq \left(\left| x[k] + \frac{e_p[k] - e_p[k-1]}{\Delta} \right| + 1.5 \right) \Delta. \tag{79}$$

This implies that (72) is satisfied and therefore that the delta-sigma modulator is non-overloading for $n = k$ provided (77) holds for $n = k$. The result follows from induction.

It follows from (63) that (77) is satisfied for any α in the range given by (9) if

$$\left| \frac{e_p[n] - e_p[n-1]}{\Delta} - \psi_{\rm PLL}[n] + (N+\alpha)\psi_{\rm ref}[n] \right| \leq \frac{1}{2}. \tag{80}$$

Frequency synthesizers usually are designed to have low phase noise, so the left side of (80) is expected to be far less than 1/2 in practice. Furthermore, in most practical cases the magnitude of α is much larger than the left side of (80). In such cases it can be verified that only four of the five ADC levels are exercised once the FDC-PLL is locked. Thus, the five ADC levels are easily sufficient to ensure that the delta-sigma modulator remains non-overloading once the FDC-PLL is locked, which also ensures that $e_{\rm ADC}[n]$ does not contain spurious tones induced by quantizer overloading.

Nevertheless, it can be verified from well-known delta-sigma modulator properties, that when the magnitude of α is 0.5, four ADC levels would only be sufficient to ensure that the delta-sigma modulator remains non-overloading in the absence of any noise other than quantization noise. Therefore, in practice five ADC levels are necessary to avoid overloading for values of α with magnitudes close to 0.5.

Substituting (63) into (75) gives

$$y[n] + \alpha = -\psi_{\rm PLL}[n] + (N+\alpha)\psi_{\rm ref}[n] + \frac{e_p[n] - e_p[n-1]}{\Delta} + e_{\Delta\Sigma 2}[n]. \tag{81}$$

This sequence is accumulated prior to the loop filter, so the input to the loop filter can be written as (14) neglecting a possible offset that depends on the initial value of the accumulator output.

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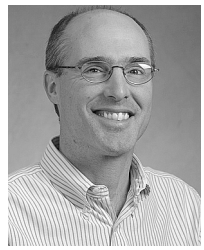

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