A Reconfigurable Mostly-Digital Delta-Sigma ADC With a Worst-Case FOM of 160 dB

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***Abstract*—This paper presents a second-generation mostly-digital background-calibrated oversampling ADC based on voltage-controlled ring oscillators (VCROs). Its performance is in line with the best $\Delta\Sigma$ modulator ADCs published to date, but it occupies much less circuit area, is reconfigurable, and consists mainly of digital circuitry. Enhancements relative to the first-generation version include digitally background-calibrated open-loop V/I conversion in the VCRO to increase ADC bandwidth and enable operation from a single low-voltage power supply, quadrature coupled ring oscillators to reduce quantization noise, digital over-range correction to improve dynamic range and enable graceful overload behavior, and various circuit-level improvements. The ADC occupies 0.075 mm^2 in a 65 nm CMOS process and operates from a single 0.9–1.2 V supply. Its sample-rate is tunable from 1.3 to 2.4 GHz over which the SNDR spans 70–75 dB, the bandwidth spans 5–37.5 MHz, and the minimum SNDR+ 10log(bandwidth/power dissipation) figure of merit (FOM) is 160 dB.**

***Index Terms*—ADC, continuous-time delta-sigma modulator, delta-sigma modulator, VCO ADC.**

I. Introduction

OVERSAMPLING ADCs based on continuous-time delta-sigma ($\Delta\Sigma$) modulators are widely used in applications such as digital wireless receivers that must accurately digitize a relatively narrow-band desired signal in the presence of potentially large out-of-band interfering signals. By sampling at a much higher rate than the desired signal's bandwidth and performing quantization noise shaping, a $\Delta\Sigma$ modulator can digitize the desired signal with high accuracy and the interfering signals with low accuracy but sufficient linearity that they can be removed by subsequent digital filtering. Continuous-time $\Delta\Sigma$ modulators with sample-rates in excess of several hundred megahertz have been shown to be particularly efficient in such applications because they allow much of the interference filtering to be done in the digital domain [1]–[6].

Unfortunately, conventional high-performance $\Delta\Sigma$ modulators require high-quality analog integrators and reference voltage sources, high-linearity feedback DACs, fast comparators, and low-jitter clock sources, all of which are increasingly difficult to design as CMOS technology is scaled and further optimized for digital circuitry. This has motivated the development of voltage-controlled ring oscillator (VCRO) based oversampling ADCs as alternatives to continuous-time $\Delta\Sigma$ modulator ADCs [7]–[13]. Such ADCs offer the high sample-rates and noise-shaping benefits of continuous-time $\Delta\Sigma$ modulator ADCs, but they consist mostly of digital components so their performance tends to improve with CMOS technology scaling.

This paper presents the highest-performance VCRO-based oversampling ADC integrated circuit (IC) published to date [14]. It does not use signal-path op-amps, analog integrators, feedback DACs, comparators, or reference voltages, so its performance is set by the speed of its digital circuitry. Unlike conventional continuous-time $\Delta\Sigma$ modulator ADCs, both its supply voltage and sample-rate can be scaled dynamically to reduce power dissipation in trade for reduced signal bandwidth or conversion accuracy.

It is a second-generation version of the oversampling ADC presented in [13]. Its maximum bandwidth has been increased and operation from a single low-voltage power supply enabled by replacing the op-amp based V/I conversion in the VCRO of the first-generation version by digitally background-calibrated open-loop V/I conversion. Its quantization noise floor has been reduced by replacing the ring oscillators in the first-generation version by quadrature-coupled ring oscillators. Its dynamic range has been increased and graceful overload behavior enabled by a digital over-range correction technique. The paper describes these techniques and additional circuit-level improvements relative to the first-generation version in detail.

II. Architecture Overview

The IC contains two oversampling ADCs. A simplified high-level diagram of one of the ADCs is shown in Fig. 1. It consists of three blocks: a *signal converter*, a *calibration unit*, and a digital *decimation filter*. Together, the signal converter and calibration unit generate a digital output sequence similar to that of a dithered, continuous-time, first-order $\Delta\Sigma$ modulator, so their combination is referred to as a $\Delta\Sigma$ modulator despite the unconventional architecture. The decimation filter is a conventional second-order cascaded integrator-comb (CIC) decimation filter [15].

The IC was tested with the transformer-based differential driver circuit shown in Fig. 2(a). In applications such as a wireless receiver, the ADC would likely be integrated along with the

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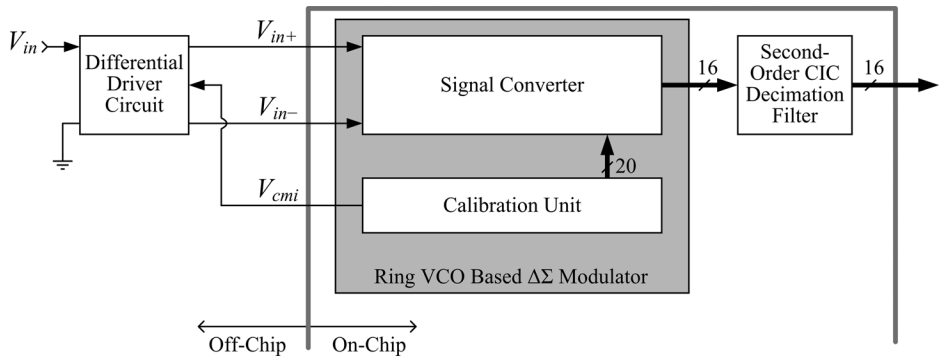

Fig. 1. Simplified high-level diagram of one of the two oversampling ADCs on the IC.

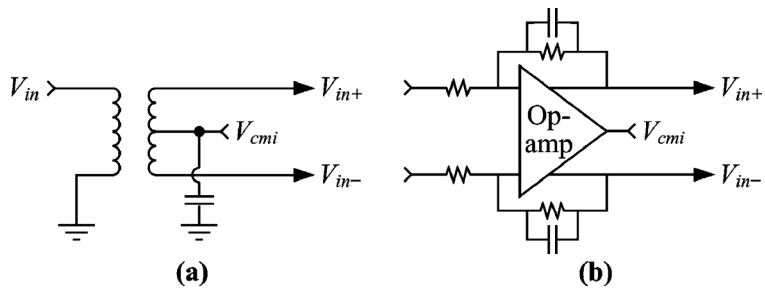

Fig. 2. Differential driver circuits: a) the transformer driver circuit used to test the IC and b) a driver circuit appropriate for system-on-chip applications.

down-conversion circuitry in which case a differential driver circuit similar to that shown in Fig. 2(b) would be appropriate.

As mentioned in the introduction, the $\Delta\Sigma$ modulator is a second-generation version of that presented in [13]. The remainder of this section briefly reviews the aspects of the architecture and its functionality that are common to both generations and indicates high-level differences between the two generations. The new enhancements implemented in the second-generation version are then described in detail in Section III.

A. Delta-Sigma Modulator High-Level Description

As shown in Fig. 3 the signal converter contains four signal paths. Each signal path consists of a voltage-to-current converter (V/I) circuit, a 14-element current controlled ring oscillator (ICRO), and digital logic components clocked at the $\Delta\Sigma$ modulator's output sample-rate, f_s. The digital logic consists of a ring sampler, a phase decoder, a $1 - z^{-1}$ block, an over-range corrector (ORC) block, and a nonlinearity corrector (NLC) block. The ring sampler consists of 28 D flip-flops that sample the pseudo-differential ICRO outputs on each f_s-rate clock edge, and the phase decoder is combinatorial logic that maps the sampled outputs to phase measurements. The $1 - z^{-1}$ block converts the phase measurements to frequency measurements and, as described in Section III, the ORC block corrects for $1-z^{-1}$ block output roll-overs caused by large input signals. The NLC block is an f_s-rate look-up table that compensates for nonlinearity introduced by the V/I circuit and ICRO. As described below the calibration unit continuously measures the nonlinearity and reloads the look-up table with new data every few hundred milliseconds.

The signal converter contains a linear feedback shift register (LFSR) that generates a pseudo-random 4-level white noise dither sequence which drives two nominally identical differential current DACs. Each DAC output is connected to the ICRO input terminal in one of the signal paths thereby adding or subtracting the dither sequence to or from the positive or negative input signal in the current domain. As shown in [13], the ICRO, ring sampler, phase decoder, and $1 - z^{-1}$ block together implement the *functionality* of a first-order $\Delta\Sigma$ modulator, and the dither causes the quantization noise to be essentially free of spurious tones.

The four signal paths are grouped into a pair of *pseudo-differential signal paths* that both operate on the same differential input signal. The $\Delta\Sigma$ modulator output is the sum of the two pseudo-differential signal path outputs. The only difference between the two pseudo-differential signal paths is the polarity with which the dither sequences are added. Therefore, summing the pseudo-differential signal path outputs doubles the desired signal component amplitude, cancels the dither components to the extent that the pseudo-differential signal paths are well matched, and causes the components corresponding to quantization noise to add in power (circuit noise causes the quantization noise from each signal path to be uncorrelated).

As shown in Fig. 4, the calibration unit consists of a signal path replica, a calibration source, a nonlinearity coefficient calculator, and a VCO center frequency controller. The signal path replica contains a copy of one of the signal converter's signal paths minus the ORC and NLC blocks, and an extra V/I circuit to provide a dummy input for the calibration source. As described in Section III, the calibration source sets the common-mode voltage of both the signal converter and the signal path

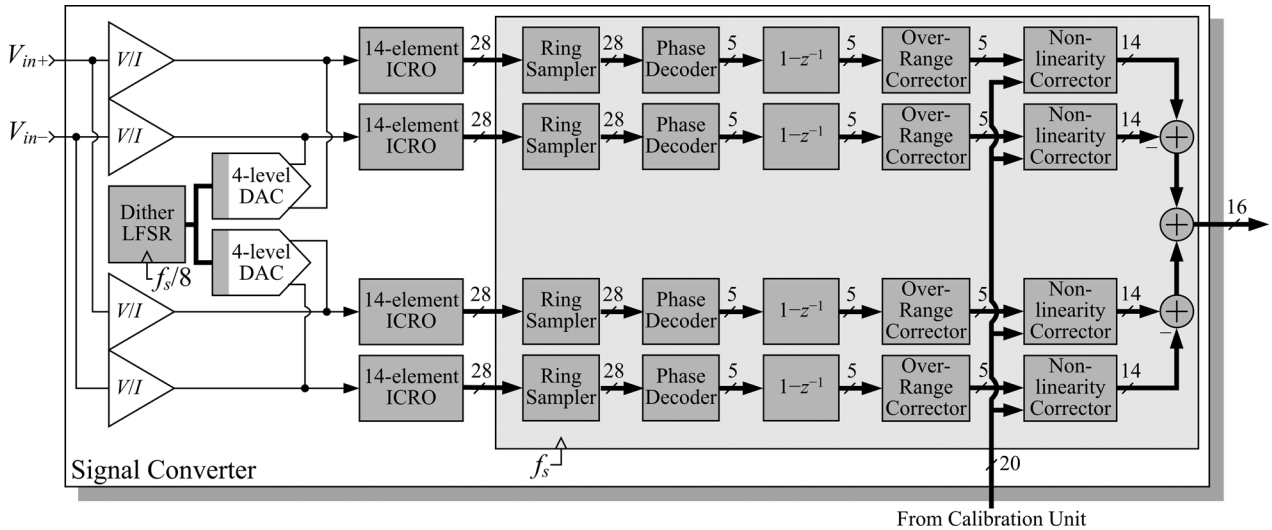

Fig. 3. High-level diagram of the signal converter.

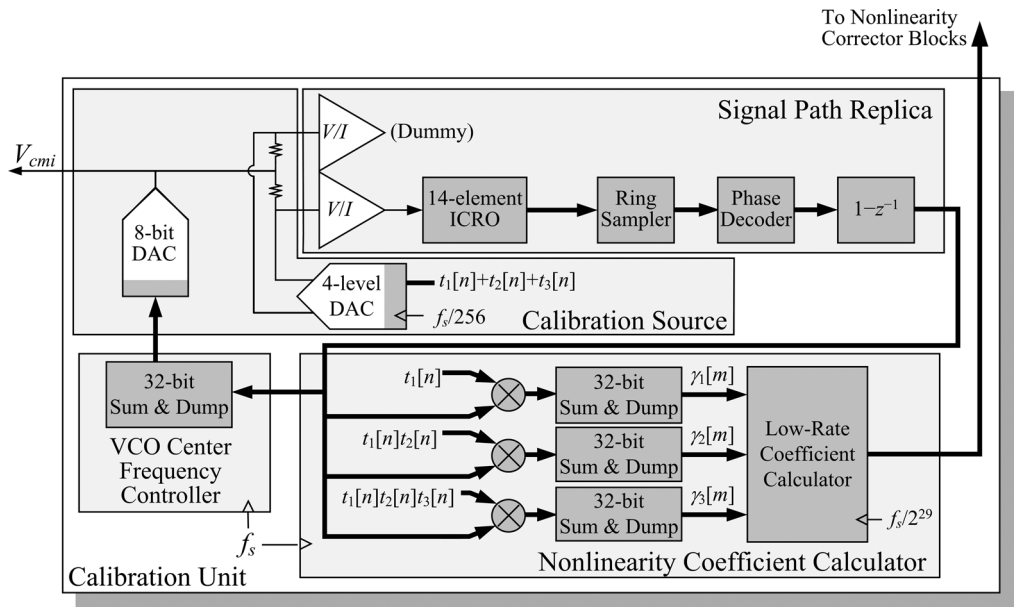

Fig. 4. High-level diagram of the calibration unit.

replica to V_{cmi}, and it sets the differential-mode voltage of the signal path replica to the sum of three two-level pseudo-random sequences, $t_1[n]$, $t_2[n]$, and $t_3[n]$.

The nonlinearity coefficient calculator and the VCO center frequency controller have the same functionality as those in [13]. As described in [13] the nonlinearity coefficient calculator continually measures the nonlinearity of the signal path replica to generate new NLC look-up table data, and the VCO center frequency controller generates a digital measure of the difference between the desired mid-scale frequency, f_s, and the center frequency of the ICRO. The calibration source adjusts V_{cmi} in a low-bandwidth feedback loop so as to zero the output of the VCO center frequency controller, thereby setting the mid-scale frequency of all the ICROs approximately to f_s. Continually updating the NLC block data and the mid-scale frequency of the ICROs re-optimizes the $\Delta\Sigma$ modulator to track changes in temperature and output sample-rate, f_s (thereby enabling reconfigurability).

As described in Section III, the V/I circuit, calibration source, ICRO, and ORC blocks are new and various additional circuit and layout improvements have been applied in the second-generation version of the $\Delta\Sigma$ modulator. Along with moving from the TSMC 65 nm LP CMOS process to the faster G+ process, these enhancements enable an improved FOM, operation from a single 0.9–1.2 V supply, and a doubling of the maximum sample-rate and bandwidth relative to [13].

B. Signal Processing Overview

Despite these differences, it follows from reasoning similar to that presented in [13] that the signal converter performs the signal processing operations shown in Fig. 5, wherein each pseudo-differential signal path is represented by the

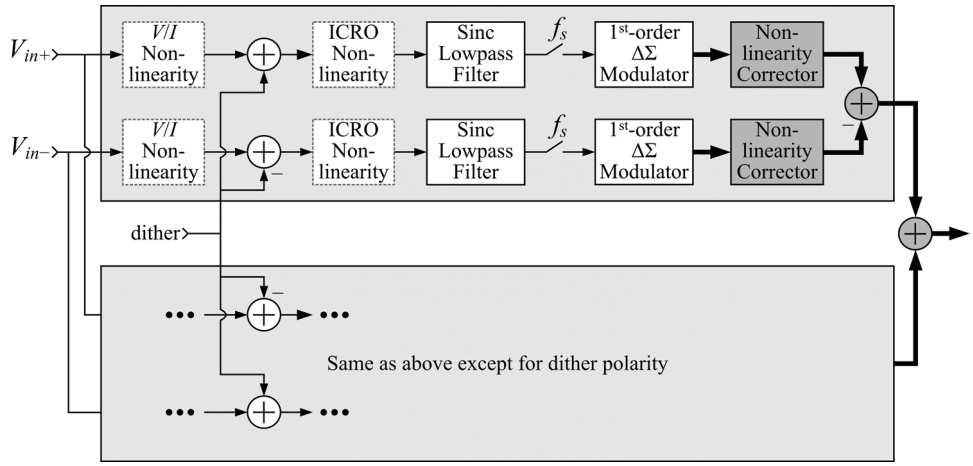

Fig. 5. Equivalent signal processing performed by the signal converter.

components in one of the two large grey boxes driven by the differential input signal. The NLC blocks and subsequent adders are the same as those shown in Fig. 3, whereas the other blocks in Fig. 5 describe the *behavior* of the signal paths prior to the NLC blocks.

Each cascade of a V/I circuit and ICRO in the signal converter implements a voltage controlled oscillator (VCO). A change in current, Δi, at the input of any of the ICROs causes the ICRO's output frequency to change by $K_{ICRO}\Delta i/2\pi$, where K_{ICRO} is the ICRO gain in units of radians per second per amp. Therefore, a change in voltage, Δv, at the input of each V/I circuit causes the corresponding ICRO's output frequency to change by $K_{ICRO}G_{V/I}\Delta v/2\pi$, where $G_{V/I}$ is the transconductance of the V/I converter. Ideally, both K_{ICRO} and $G_{V/I}$ are independent of Δi and Δv, respectively, but in practice this is not the case so both the V/I circuit and the ICRO introduce nonlinear distortion.

The blocks with dashed boundaries represent the nonlinear distortion introduced by the V/I circuits and the ICROs. The dither is added positively or negatively after each V/I circuit nonlinearity and before each ICRO nonlinearity, and the output of each ICRO nonlinearity drives a lowpass continuous-time sinc filter with transfer function

$$H_c(f) = K_{VCO}e^{-j\pi T_s f}\frac{\sin(\pi T_s f)}{\pi f} \tag{1}$$

where $T_s = 1/f_s$, and K_{VCO} is the VCO gain defined as $K_{ICRO}G_{V/I}$ when $V_{in+} = V_{in-} = V_{cmi}$. The output of each filter is sampled at a rate of f_s, and the resulting sequence is passed through a first-order 5-bit $\Delta\Sigma$ modulator.

III. New Signal Processing and Circuit Enhancements

A. The Open-Loop V/I Circuit and its Implications

V/I conversion in each pseudo-differential signal path in the first-generation $\Delta\Sigma$ modulator presented in [13] is performed by a fully differential op-amp feedback circuit with sufficiently high linearity that it is not necessary for the subsequent NLC blocks to compensate for its nonlinear distortion. This allows the $t_1[n] + t_2[n] + t_3[n]$ signal in the calibration unit to be added directly to the signal path replica's ICRO input in the current domain, which simplifies the design of the calibration source. Unfortunately, the first-generation V/I circuit requires a 2.5 V supply and a high-performance op-amp to achieve the necessary linearity, headroom, and SNR, whereas the other components in the $\Delta\Sigma$ modulator operate from a 1.2 V supply.

Each copy of the V/I circuit in the second-generation $\Delta\Sigma$ modulator is a non-differential source-degenerated common source amplifier as shown in Fig. 6. It operates from the same 0.9 V to 1.2 V supply as the rest of the $\Delta\Sigma$ modulator and the pair of V/I circuit copies in each pseudo-differential signal path has a higher bandwidth, lower noise floor, and lower power dissipation than the V/I circuit in [13]. Unfortunately, it introduces nonlinear distortion that must be corrected by the subsequent NLC block and the pseudo-differential design maximizes differential-mode input voltage headroom at the expense of a narrow usable common mode input voltage range. These issues complicate the design of the calibration unit as described in Section III-B.

The use of a nonlinear V/I circuit in the $\Delta\Sigma$ modulator raises an additional potential problem relating to dither intermodulation error. It is not practical to add wide-bandwidth voltage signals with high precision in open-loop circuits, so the dither signals are added to the signal converter's ICRO inputs in the current domain. Therefore, as indicated in Fig. 5 the input signal is subjected to the combined nonlinearity of the V/I circuit and ICRO whereas the dither is subjected only to the nonlinearity of the ICRO. The NLC blocks correct for the nonlinearity seen by the input signal, but cannot be made also to correct for the nonlinearity seen by the dither. It can be verified that this introduces intermodulation products of the signal and dither in each signal path.

The ICRO has very strong second-order distortion, so the most significant intermodulation product is the direct product of the dither term and the signal term. Fortunately, the signal converter's four signal path structure is such that this term is cancelled in the $\Delta\Sigma$ modulator output up to the matching accuracy of the signal paths [16]. Extensive simulations and exper-

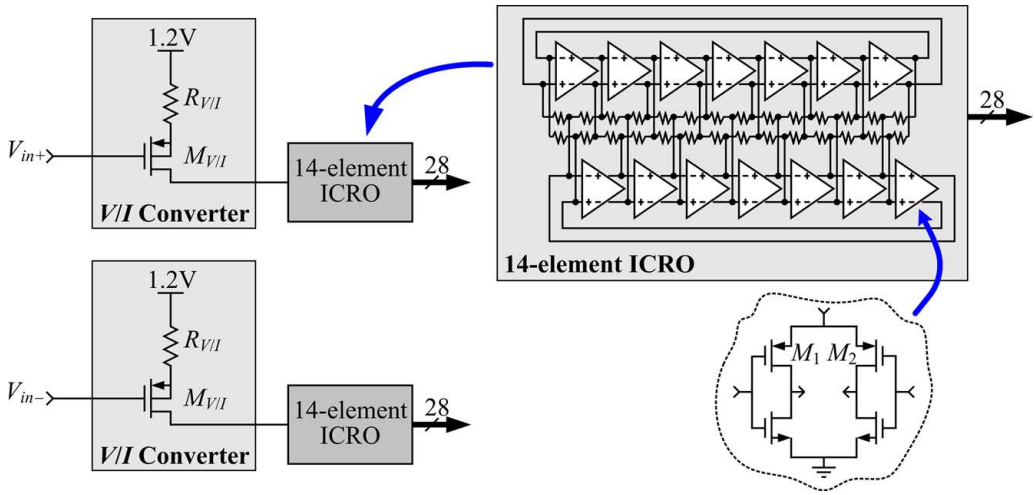

Fig. 6. V/I circuit and ICRO details.

imental results indicate that the residual intermodulation term from imperfect path matching and the higher-order intermodulation terms that are not cancelled by the structure are well below the noise floor of the $\Delta\Sigma$ modulator.

This is a significant advantage of the four signal path structure. A signal converter that consists of just two signal paths with a differential-mode input signal and common mode dither would have the self-cancelling dither property of the four signal path structure, but it would not cancel the intermodulation term described above [16].

V/I Circuit Details: The transistor in each V/I circuit is a thin-oxide pMOS device with a nominal transconductance of $10^{-2}\ \Omega^{-1}$ and a nominal threshold voltage magnitude of 320 mV. The source degeneration resistor has a nominal resistance of 310 Ω. At the maximum f_s of 2.4 GHz, the V/I circuit's transconductance, $G_{V/I}$, is $2.2 \cdot 10^{-3}\ \Omega^{-1}$ which corresponds to a full-scale ADC differential input signal swing of 800 mV. Both $G_{V/I}$ and the signal swing decrease with ICRO frequency, which (optionally) allows the supply voltage to be scaled with f_s. In this design f_s is tunable from 1.3 GHz to 2.4 GHz which corresponds to a supply voltage range of 0.9 V to 1.2 V. The design is such that the necessary input bias voltage (which is supplied by the calibration unit as described in Section III-B) is roughly half the scaled supply voltage.

Simulations indicate that even though the V/I circuit noise is much lower than that of the first-generation design, it still is much higher than the ICRO noise. The input referred noise contributions from the transistors and resistors of the four V/I circuit copies in the $\Delta\Sigma$ modulator simulated with $f_s = 2.4$ GHz are 5.4 $\mathrm{nV/Hz^{1/2}}$ and 2.9 $\mathrm{nV/Hz^{1/2}}$, respectively, and the $1/f$ noise corner of the transistors occurs at roughly 400 kHz.

Simulations indicate that the V/I circuit introduces strong second-order distortion but relatively weak higher-order distortion. For example, with $f_s = 2.4$ GHz and a nearly full-scale 250 kHz sinusoidal input signal, the second, third, and fourth harmonics at the output of the V/I circuit are at -29 dBc, -43 dBc and -60 dBc respectively. Interestingly, the ICRO introduces distortion with similar magnitudes but opposite signs so the distortion introduced by the V/I circuit and ICRO together is lower than that of just the V/I circuit. For example, under the same simulated conditions described above, the second, third, and fourth harmonics at the output of the cascade of the V/I circuit and ICRO are at -35 dBc, -49 dBc and -66 dBc, respectively.

The NLC blocks only correct for second-order and third-order static distortion, so the V/I circuit nonlinearity must be well-modeled as a Taylor series in which only the first three terms are significant. This requires that the V/I circuit transistor be kept well in saturation with sufficient source degeneration. Unfortunately, the small headroom budget limited the amount of resistor degeneration that could be used, so the Taylor series approximation starts to break down when the input signal exceeds -3 dB full scale (dBFS). Therefore, the SNDR of the $\Delta\Sigma$ modulator tends to peak when the input signal reaches -3 dBFS.

B. The Calibration Unit's Calibration Source

The requirement that the NLC blocks correct for V/I circuit nonlinear distortion and the use of pseudo-differential V/I conversion both complicate the calibration source relative to its counterpart in the first-generation $\Delta\Sigma$ modulator. In the first-generation $\Delta\Sigma$ modulator the calibration source is a simple non-differential four-level current DAC connected to the input of the signal path replica's ICRO. In the second-generation $\Delta\Sigma$ modulator the calibration source must drive the signal path replica's V/I circuits with the $t_1[n] + t_2[n] + t_3[n]$ signal in the form of a differential voltage and it must generate a common-mode voltage, V_{cmi}, for all of the $\Delta\Sigma$ modulator's V/I circuits.

As shown in Fig. 7 the second-generation calibration source contains three current-steering cells. Each current steering cell steers its current, I_{cal}, to its left or right output depending on whether its one-bit input sequence is high or low, respectively. Each one-bit input sequence represents one of the two-level sequences $t_1[n]$, $t_2[n]$, or $t_3[n]$. The right and left outputs of the current steering cells are all connected to the right and left $4R_{V/I}$ resistors, respectively, so the differential voltage across

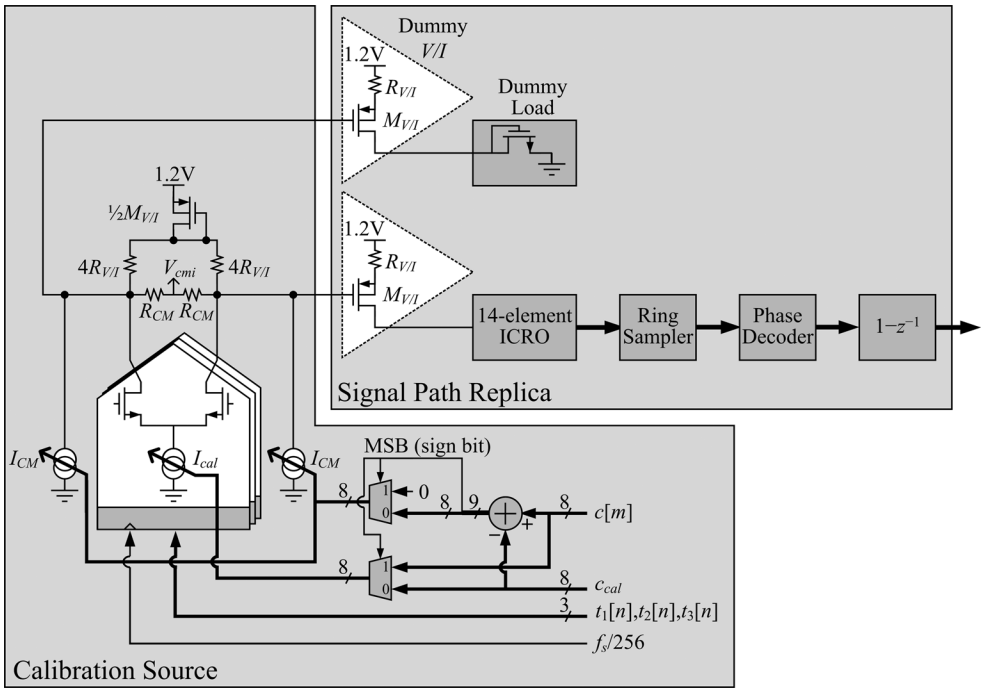

Fig. 7. Details of the calibration source in the calibration unit.

the current steering cell right and left outputs represents the $t_1[n] + t_2[n] + t_3[n]$ signal.

The R_{CM} resistors, which are much larger than the $4R_{V/I}$ resistors, are used to sense the common-mode voltage, V_{cmi}, of the $t_1[n] + t_2[n] + t_3[n]$ signal. This voltage is provided to the differential driver circuit as shown in Figs. 1 and 2 to set the common-mode input voltage of the V/I circuits in the signal converter.

The diode connected pMOS transistor labeled $1/2M_{V/I}$ has the same length and half the width of $M_{V/I}$. Its dimensions and the size of the resistors to which it is connected were chosen to mimic the stack-up of the V/I circuit such that the mid-scale current through each copy of the V/I circuit mirrors that through the $1/2M_{V/I}$ transistor.

The I_{cal} and I_{CM} current sources are each made up of eight output-connected power-of-two weighted current sources that are each turned off or on by a bit in the corresponding 8-bit bus shown in the figure. The component current sources in the two I_{CM} current sources are each half the size of the corresponding component current sources in the I_{cal} current source. The 8-bit value, c_{cal}, sets the differential amplitude of the $t_1[n] + t_2[n] + t_3[n]$ signal. Changing c_{cal} adjusts both I_{cal} and I_{CM} such that V_{cmi} remains nearly unchanged.

The $c[m]$ sequence is the output of the VCO center frequency controller, which is the 8 most-significant bits (MSBs) of the VCO center frequency controller's sum and dump accumulator at the time of the last dump operation. It controls the common mode voltage of the $t_1[n] + t_2[n] + t_3[n]$ signal, and, therefore, V_{cmi}, to adjust the center frequency of all the ICROs to approximately f_s via the feedback operation described in Section II. The multiplexers in the calibration source set the I_{CM} control bus to zero and the I_{cal} control bus to $c[m]$ in the event that $c[m] - c_{cal}$ temporarily goes negative while the feedback loop is settling.

Dither is not used in the signal path replica because it would have increased the correlation time necessary to achieve accurate NLC look-up table data. Instead, the random nature of the $t_1[n] + t_2[n] + t_3[n]$ signal is relied upon to dither the signal path replica. Simulations indicate that this works well provided the differential amplitude of the $t_1[n] + t_2[n] + t_3[n]$ signal is between 40% and 100% of the signal path replica's full-scale input. Therefore, c_{cal} must be chosen to keep the $t_1[n] + t_2[n] + t_3[n]$ signal within this range over expected process, supply voltage, and temperature (PVT) variations. Extensive simulations indicate that a relatively wide range of c_{cal} values satisfy this requirement, although on the IC it can be set via the serial port to provide testing flexibility.

C. Over-Range Correction

A disadvantage of conventional $\Delta\Sigma$ ADCs, particularly in applications involving automatic gain control, is that they go unstable with long recovery times if their input no-overload ranges are exceeded. Often this problem is addressed by keeping the amplitude of the input signal sufficiently small that even the occasional large transient does not exceed the input no-overload range. While this avoids the overload problem, it tends to waste the $\Delta\Sigma$ ADC's dynamic range because most of the time the input signal spans a range that is much smaller than the input no-overload range.

An analogous problem occurs in the first-generation $\Delta\Sigma$ modulator presented in [13]: the $1 - z^{-1}$ block outputs roll-over from their maximum to minimum values or vice versa when the input no-overload range is exceeded. Although the $\Delta\Sigma$ modulator does not take time to recover after such roll-overs,

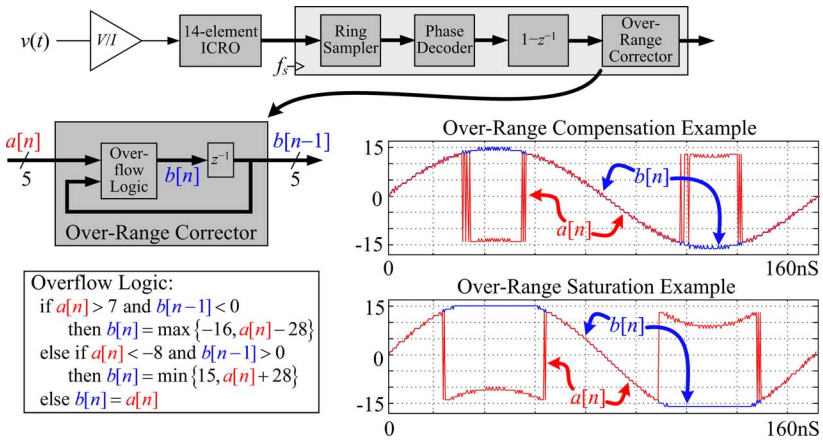

Fig. 8. Over-range corrector block details.

the decimation filter following the $\Delta\Sigma$ modulator is disturbed by the roll-overs and the resulting transient takes time to die out.

As described below, the ORC blocks in the second-generation $\Delta\Sigma$ modulator eliminate this problem. They extend the input no-overload range beyond that of the first generation $\Delta\Sigma$ modulator and cause the output to clip for signals outside the widened no-overload range.

The Roll-Over Problem: During the nth f_s-rate clock interval each ring sampler samples the preceding ICRO's inverter outputs, and the subsequent phase decoder maps the sampled bits into a number, $p[n]$, that represents a quantized version of the ICRO phase modulo-2π. Each ICRO has 14 delay elements, so $p[n]$ can be any number in the range $\{0, 1, 2, \ldots, 27\}$, where a phase of π radians corresponds to $p[n] = 14$ and the phase quantization step-size is $2\pi/28$. To account for the modulo-2π operation, each $1 - z^{-1}$ block generates its output as

$$a[n] = \begin{cases} p[n] - p[n-1], & \text{if } -14 \le p[n] - p[n-1] \le 13, \\ p[n] - p[n-1] + 28, & \text{if } p[n] - p[n-1] < -14, \\ p[n] - p[n-1] - 28, & \text{otherwise.} \end{cases} \tag{2}$$

Thus, the range of $a[n]$ is $\{-14, -13, -12, \ldots, 13\}$ where -14 represents a phase change of $-\pi$.

Provided the ICRO's average frequency over the nth clock interval is greater than or equal to $0.5f_s$ and less than $1.5f_s$ then $a[n]$ is a quantized representation of ICRO's phase change minus 2π. For example, if the ICRO frequency is $0.5f_s$ over the nth clock interval then $a[n]$ is -14 which indicates that the phase change over the $1/f_s$ clock interval minus 2π is $-\pi$.

In contrast, if the ICRO's average frequency over the nth clock interval is less than $0.5f_s$ or greater than or equal to $1.5f_s$ then the phase change represented by $a[n]$ is incorrect by a non-zero multiple of 2π. For example, if the ICRO frequency is Kf_s over the nth clock interval where K is any positive integer, then $a[n]$ is zero regardless of K whereas the true phase change over the clock interval minus 2π is $2\pi\ (K-1)$.

In the first-generation $\Delta\Sigma$ modulator the input no-overload range is defined as the maximum input voltage range for which all the ICROs have frequencies below $1.5f_s$ but not below $0.5f_s$. Therefore, the $1 - z^{-1}$ block outputs only roll-over and cause error if the input no-overload range is exceeded.

1) Over-Range Corrector Blocks: By extending the line of reasoning outlined above it follows that $a[n] + 28$ or $a[n] - 28$ represents the ICRO's phase change over the nth clock interval minus 2π when the ICRO's average frequency over the clock interval is between $1.5f_s$ and $2.5f_s$ or less than $0.5f_s$, respectively. The ORC blocks exploit this result to compensate for roll-over events.

The details of each ORC block are shown in Fig. 8. The input-referred dither level in the signal converter is approximately -26 dBFS, so the instantaneous frequency of each ICRO in the signal converter is dominated by the input signal over most of the input no-overload range. It can be verified that even with relaxed anti-alias filtering prior to the $\Delta\Sigma$ modulator, e.g., a single pole at $f_s/(4\pi)$, the ICRO's instantaneous frequency over the nth clock period is less than $0.5f_s$ when and only when $a[n] < -8$ and $a[n-1] > 0$. In such cases the ORC block sets its output to the minimum of 15 and $a[n] + 28$, which is equivalent to correcting the roll-over error and then clipping the result to 15 if necessary. Similarly, the ICRO's instantaneous frequency over the nth clock period is greater than or equal to $1.5f_s$ and less than $2.5f_s$ when and only when $a[n] > 7$ and $a[n-1] < 0$. In such cases the ORC block sets its output to the maximum of -16 and $a[n] - 28$, which is equivalent to correcting the roll-over error and then clipping the result to -16 if necessary.

Therefore, as illustrated by the simulated ORC block input and output sequences shown in Fig. 8 the output of each ORC block, $b[n]$, is a 5-bit sequence that differs from $a[n]$ only in clock intervals during which a $1 - z^{-1}$ block roll-over event occurs. In the absence of a roll-over event $b[n]$ ranges from -14 to 13. When a roll-over event occurs the ORC block corrects the error down to a minimum value of -16 or a maximum value of 15 after which it clips. The clipping represents a graceful overload behavior that avoids the roll-over problem described above.

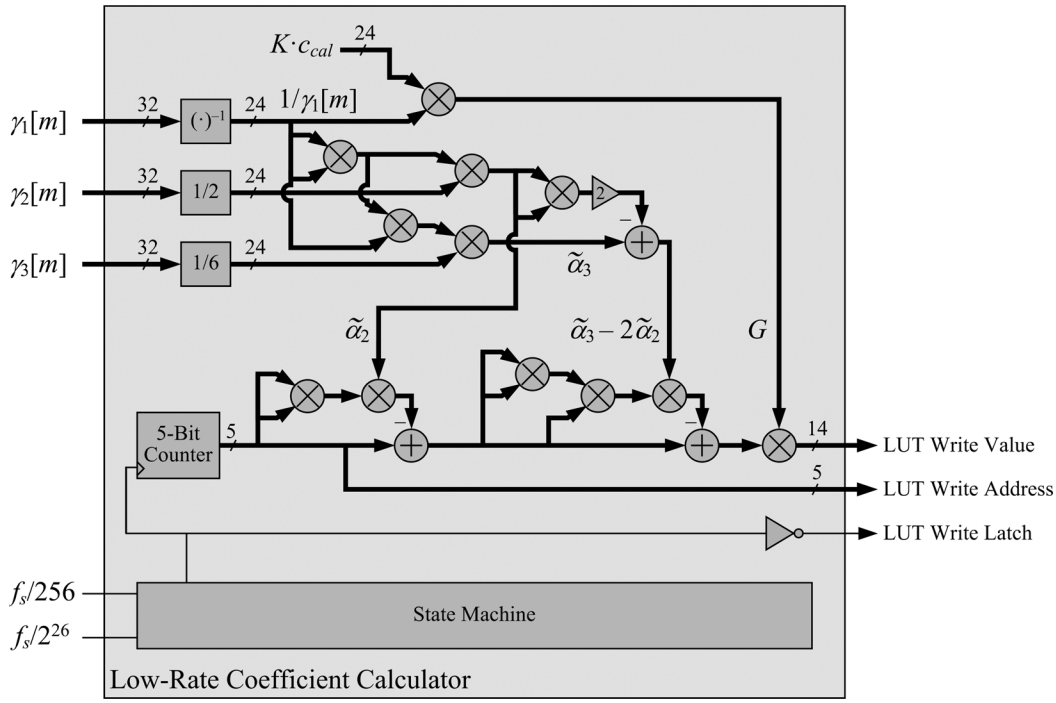

Fig. 9. Low-rate coefficient calculation block signal processing details.

The ORC blocks could easily be modified to further extend the input range prior to clipping, but this was not done for two reasons. First, the V/I converter becomes strongly non-linear for input signals outside the input-referred clipping range, so there is little benefit to maintaining output values below -16 or above 15. Second, clipping the output to 5 bits reduces the power dissipation and circuit area from what would otherwise be required by the NLC blocks.

D. Quadrature-Coupled Ring VCOs

In any $\Delta\Sigma$ modulator of a given order, the signal to quantization noise ratio (SQNR) over the signal bandwidth increases with the number of quantization levels and the oversampling ratio, and for a given signal bandwidth the oversampling ratio is determined by the $\Delta\Sigma$ modulator's sample-rate, f_s. Unfortunately, the number of quantization levels and f_s are not independent design variables in ring VCO based $\Delta\Sigma$ modulators as they are in conventional $\Delta\Sigma$ modulators. The number of quantization levels is equal to twice the number of ring oscillator delay elements whereas f_s is inversely proportional to the number of ring oscillator delay elements. Therefore, the SQNR ultimately depends on the minimum delay, τ, through each of the ring oscillator's delay elements, which is IC technology and supply voltage dependent.

In the first-generation $\Delta\Sigma$ modulator each ICRO has 15 delay elements and each delay element has a minimum τ of approximately 30 ps, so the maximum f_s is 1.15 GHz. Unfortunately, the resulting quantization noise floor is higher than the noise floor imposed by the other noise sources in the first-generation $\Delta\Sigma$ modulator for signal bandwidths above 9 MHz, so the $\Delta\Sigma$ modulator's overall SNR is approximately equal to the SQNR over such bandwidths. This is undesirable because the quantization noise prevents utilization of what would otherwise be the full dynamic range of the $\Delta\Sigma$ modulator.

Unfortunately, τ is approximately the same in both the first-generation and second-generation versions of the $\Delta\Sigma$ modulator. Although the second-generation version is implemented in the TSMC 65 nm CMOS G+ process, which is somewhat faster than the TSMC 65 nm LP CMOS process used for the first-generation version, the lower V/I converter supply voltage in the second-generation version negated the potential reduction in τ. The ICRO delay elements in both generations are current-starved inverters driven by the V/I circuits, so the voltage of the current starved node is lower in the second-generation version than in the first-generation version.

One way to circumvent this problem is to use a more highly-scaled CMOS process. This option was not available to the authors at the time the second-generation $\Delta\Sigma$ modulator was developed, so a system-level solution to reduce the quantization noise floor was developed. As illustrated in Fig. 6 each of the ICROs in the second-generation $\Delta\Sigma$ modulator consists of two 7-element sub-ICROs quadrature-coupled through a resistor network to lock 90° out of phase with each other. The 7 pseudo-differential inverter outputs from each of the sub-ICROs are interlaced with those from the other to form the 14 pseudo-differential quadrature-coupled ICRO outputs. The result is equivalent to a 14-element conventional ICRO with a minimum inverter delay of $\tau/2$ rather than τ [17]. The technique thus reduces the $\Delta\Sigma$ modulator's quantization noise floor 6 dB below that which would otherwise have been imposed by the IC technology.

Pseudo-differential current starved inverters are used for each delay element as shown in Fig. 6. In conventional ICROs, such as in the first-generation $\Delta\Sigma$ modulator, cross-coupled inverters are required at the delay element outputs to maintain a differen-

tial output signal. Such cross-coupled inverters are not required in the ICRO delay elements used in the second-generation $\Delta\Sigma$ modulator because the resistor network maintains differential delay element outputs in addition to keeping the two sub-ICROs locked 90° out of phase. Simulations indicate that eliminating the cross-coupled inverters reduces circuit noise by more than the resistor network increases circuit noise. Hence, the ICROs in the second-generation $\Delta\Sigma$ modulator introduce less noise than those in the first-generation $\Delta\Sigma$ modulator, although in both cases the ICRO noise is much lower than the V/I circuit noise.

E. Digital Enhancements to the Calibration Unit

The second-generation $\Delta\Sigma$ modulator's calibration unit incorporates three digital enhancements relative to that of the first-generation $\Delta\Sigma$ modulator: on-chip implementation of the low-rate coefficient calculator, automatic normalization of the output signal to represent input voltage independent of PVT variations, and adjustable duty cycle scaling to reduce power dissipation. These enhancements are described below.

As described in [13], the low-rate coefficient calculations convert the sequences, $\gamma_1[m]$, $\gamma_2[m]$, and $\gamma_3[m]$, shown in Fig. 4 into look-up table (LUT) data used by the NLC blocks to correct second-order and third-order nonlinearity. In the first-generation $\Delta\Sigma$ modulator they are performed off-chip. In the second-generation $\Delta\Sigma$ modulator they are performed on-chip by the low-rate coefficient calculator.

As indicated in Fig. 9, the low-rate coefficient calculator sequentially generates the 32 look-up table entries and writes them into the NLC blocks as they become available. The $\tilde{\alpha}_2$ and $\tilde{\alpha}_3$ intermediate variables shown in Fig. 9 are the estimated second and third Taylor series coefficient estimates described in [13], and the look-up table data cause the each NLC block to implement

$$y[n]|_{corrected} = G\left[y[n] - \tilde{\alpha}_2(y[n])^2 - \left(\tilde{\alpha}_3 - 2\tilde{\alpha}_2^2\right)\left(y[n] - \tilde{\alpha}_2(y[n])^2\right)^3\right] \quad (3)$$

where $y[n]$ denotes the NLC block input sequence. The gain variable G is calculated to scale the $\Delta\Sigma$ modulator's output code such that the least significant bit (LSB) code step is 12.2 μV independent of PVT variation.

The sub 1 kHz look-up table update-rate allows area-efficient multi-clock implementation of the $1/\gamma_1[m]$ calculation and all the multiplications shown in Fig. 9 to be performed sequentially by reusing a single 24-bit multiplier. Consequently, the circuit area occupied by the low-rate coefficient calculator is less than 0.01 mm^2.

A new duty cycle scaling feature is implemented in the calibration unit. When the feature is enabled via serial port control, the calibration unit's duty cycle is reduced by repeatedly enabling the calibration unit for $2^{26}f_s$-rate clock cycles and then disabling it for $7 \cdot 2^{26}$ clock cycles, thereby reducing its logic switching power dissipation by a factor of 8. When the ADC is powered up, the duty cycle scaling feature is disabled and the calibration unit generates full sets of NLC look-up table data at a rate of $f_s/2^{26}$ (once every 28 ms when f_s is at its maximum value of 2.4 GHz). After a few $f_s/2^{26}$-rate update intervals the duty cycle scaling feature is enabled. Subsequent sets of NLC look-up table data are then generated at a rate of $f_s/2^{29}$ (once every 224 ms when $f_s = 2.4$ GHz).

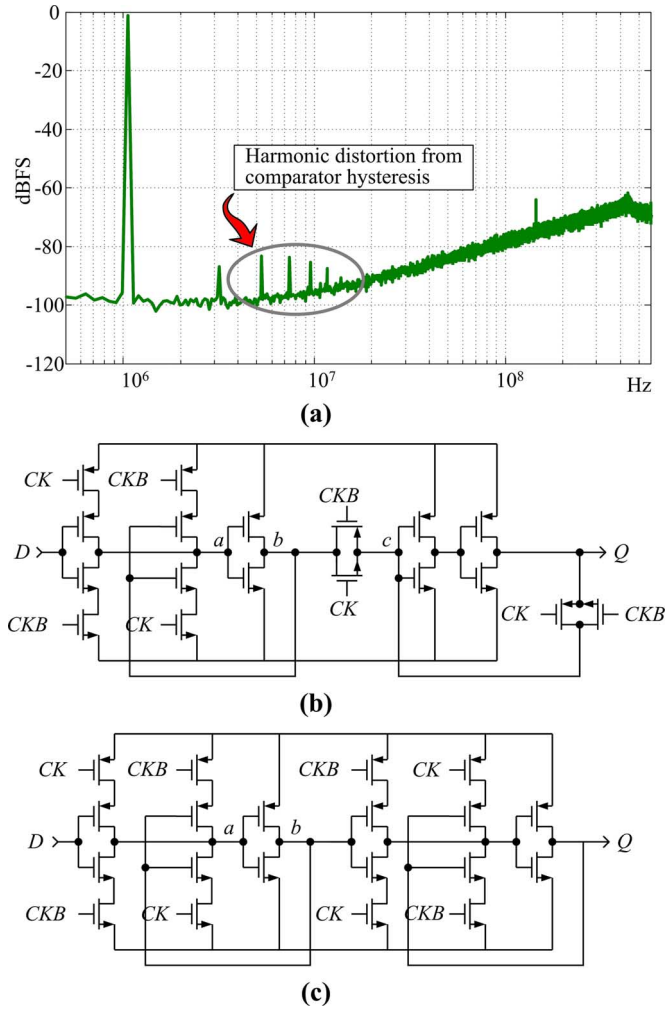

Fig. 10. (a) Output PSD of first-generation $\Delta\Sigma$ modulator with harmonic distortion caused by the flip-flop's signal-dependent hysteresis, (b) flip-flop used in first-generation $\Delta\Sigma$ modulator's ring sampler, and (c) the flip-flop used in the second-generation $\Delta\Sigma$ modulator to avoid the problem.

F. Ring Sampler Signal-Dependent Hysteresis Elimination

A measured output PSD plot from the first-generation $\Delta\Sigma$ modulator is shown in Fig. 10(a). The harmonic distortion tones circled on the plot were not predicted by theory or simulation prior to fabricating the IC. Although relatively small, they are not insignificant so an effort was made to avoid them in the second-generation $\Delta\Sigma$ modulator. An investigation led to the conclusion that they result from signal-dependent hysteresis in the ring sampler flip-flops. The circuit simulations from which output PSD plots were estimated prior to fabrication used a behavioral model for the flop-flops, so this problem was missed initially.

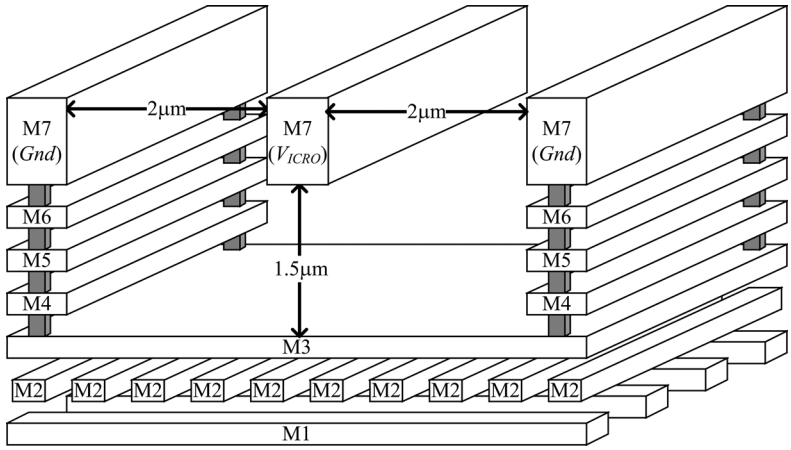

Fig. 11. Layout of the connection between each dither DAC output and ICRO input in the signal converter.

A circuit diagram of the standard transmission-gate flip-flop used in the first-generation $\Delta\Sigma$ modulator's ring sampler is shown in Fig. 10(b). The design is such that node c is charged or discharged depending on the current state of the flip-flop. When the flip-flop transitions from hold to sample mode, the transmission gate switch across nodes b and c closes and the inverter connected to node b must charge or discharge the capacitance of both nodes b and c. This causes the flip-flop's decision threshold at each clock edge to depend on the current state of the flip-flop, i.e., it causes signal-dependent hysteresis. The result is relatively high-order harmonic distortion in the $\Delta\Sigma$ modulator output as indicated in Fig. 10(a).

A solution is to use the standard non-transmission-gate flip-flop shown in Fig. 10(c). Simulations indicate that it exhibits far less signal-dependent hysteresis than the flip-flop of Fig. 10(b). The ring samplers in the second-generation $\Delta\Sigma$ modulator incorporate the flop-flop of Fig. 10(c). As expected, neither transistor-level simulation results nor the experimental results presented in Section IV indicate the presence of harmonic distortion tones like those attributed to signal-dependent hysteresis in the first-generation $\Delta\Sigma$ modulator.

G. High-Frequency Linearity Improvement

The calibration unit's nonlinearity correction algorithm assumes that the nonlinearity introduced by each V/I circuit and ICRO is independent of frequency. This assumption starts to break down and the correction implemented by the calibration unit and NLC blocks becomes less accurate as the frequency of the input signal is increased. Circuit simulations indicate that the most significant contributor to frequency-dependent nonlinearity in both $\Delta\Sigma$ modulator generations is parasitic capacitance at the current-starved input nodes of the ICROs.

Two techniques were applied in the in the second-generation $\Delta\Sigma$ modulator to reduce this parasitic capacitance so as to increase the usable signal bandwidth relative to the first-generation $\Delta\Sigma$ modulator. First, the relatively long interconnect lines between the dither DACs and the ICROs were each laid out as shown in Fig. 11, where the bathtub-like grounded metal structure surrounding the interconnect line provides shielding with low parasitic capacitance because of its large spacing from the interconnect line. Second, the diffusion capacitance at the coupled sources of the ICRO transistors labeled M_1 and M_2 in Fig. 6 is minimized. Each of M_1 and M_2 is laid out as two parallel devices with a shared source diffusion well to minimize capacitance at the current starved node of the inverter. Having the sources share a diffusion well instead of the drain reduces parasitic capacitance at the critical current starved node at the expense of increasing the drain capacitance, so for a given ICRO

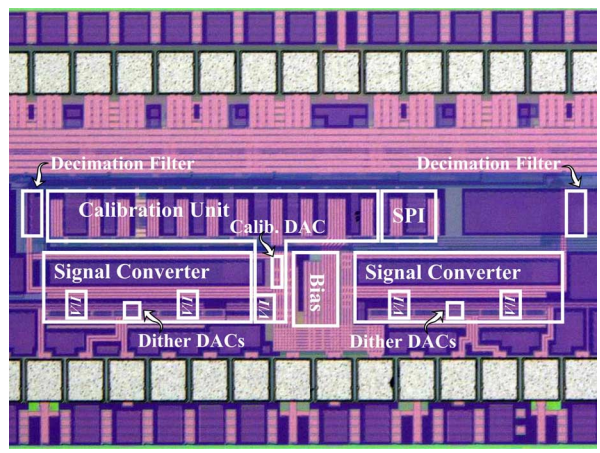

Fig. 12. Die photograph.

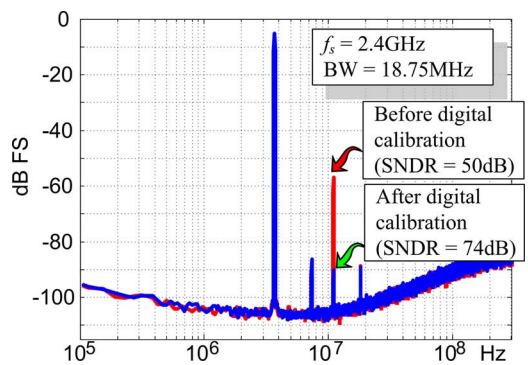

Fig. 13. Typical measured output PSD plots with and without calibration enabled for $f_s = 2.4$ GHz.

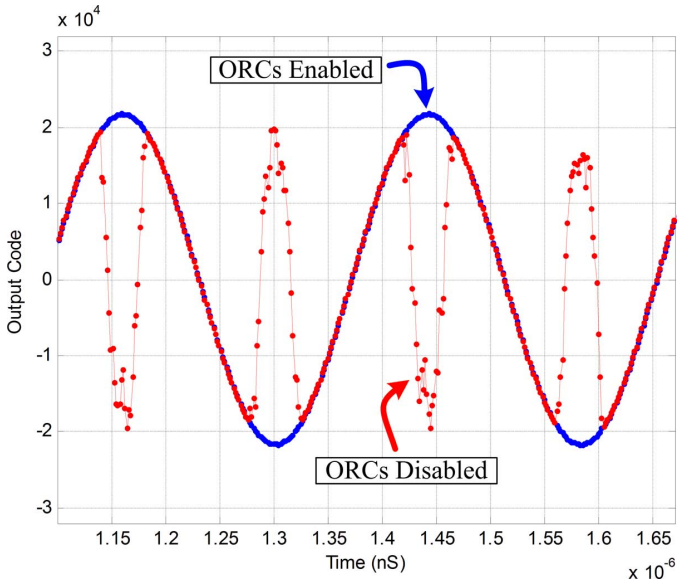

Fig. 14. Measured decimation filter output sequences with the ORC blocks enabled and disabled for $f_s = 2.4$ GHz and an input signal below the clipping level.

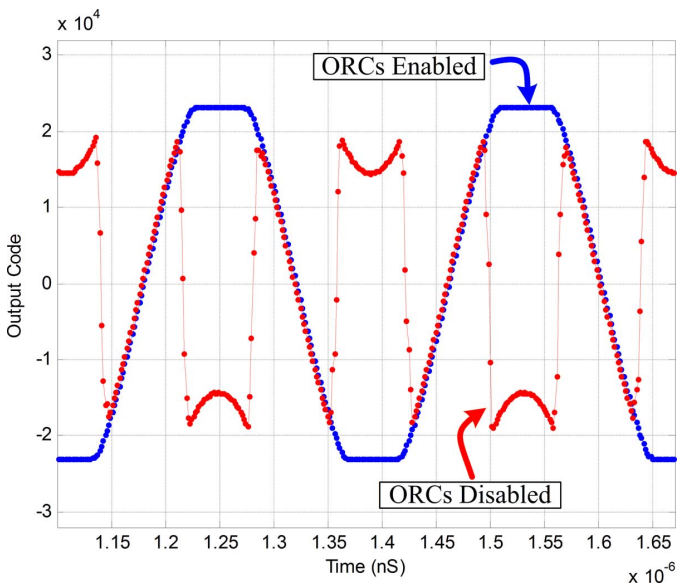

Fig. 15. Measured decimation filter output sequences with the ORC blocks enabled and disabled for $f_s = 2.4$ GHz and an input signal above the clipping level.

design and VLSI process it improves high-frequency linearity at the expense of reducing the maximum ICRO frequency

IV. Measurement Results

A die photograph of the IC is shown in Fig. 12. The IC was fabricated in the TSMC 65 nm G+ process with the deep n-well and dual-oxide device options, but without the MiM capacitor option. It contains two $\Delta\Sigma$ modulators that share a common calibration unit, two decimation filters, LVDS output drivers, bias circuitry, and serial port interface logic.

All of the components of both $\Delta\Sigma$ modulators are implemented on-chip. The combined area occupied by the two signal

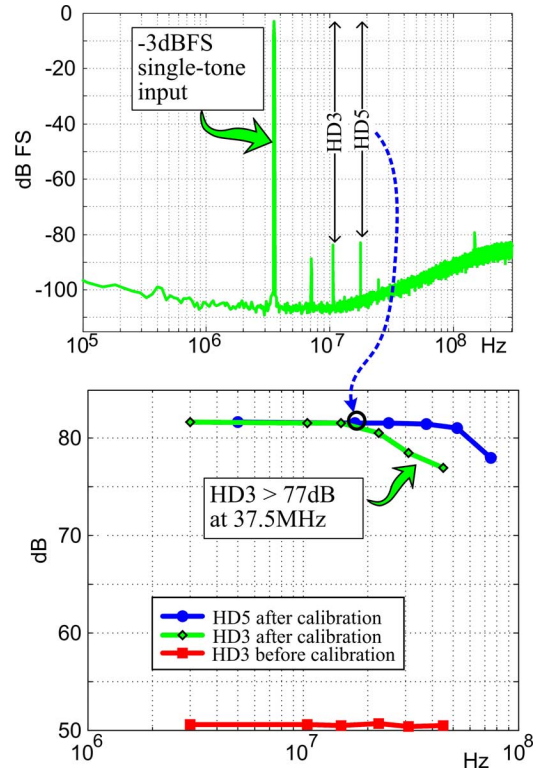

Fig. 16. Measured harmonic distortion versus input frequency for $f_s = 2.4$ GHz.

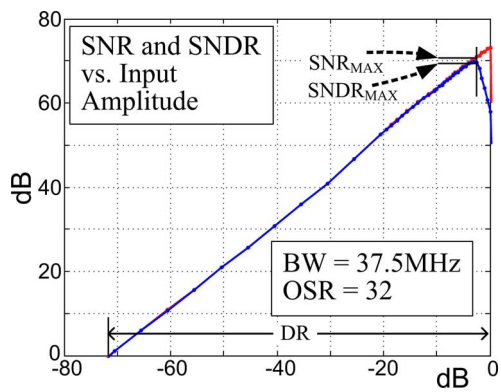

Fig. 17. Measured SNR and SNDR versus input amplitude for $f_s = 2.4$ GHz.

converters, the calibration unit, and the ADC bias circuitry is 0.15 mm^2, so the area per $\Delta\Sigma$ modulator is 0.075 mm^2. The calibration unit and each signal converter occupy 0.07 mm^2 and 0.04 mm^2, respectively. The calibration unit is 0.01 mm^2 larger than that in the first-generation $\Delta\Sigma$ modulator because it includes the low-rate coefficient calculator.

The IC was packaged in a 64-pin LFCSP package which was socket mounted to a printed circuit test board. The test board contains input signal and clock conditioning circuitry, and an FPGA for data capture and serial port communication. A simplified diagram of the input conditioning circuitry is shown in Fig. 2(a). The clock conditioning circuitry is also transformer-based; it converts the single-ended output of a laboratory signal generator to a differential clock signal for the IC. A single 0.9 V to 1.2 V power supply provides the supply voltage for all blocks

	This Work												[13]		[1]	[2]	[3]	[4]	[5]	[6]
Area (mm^2)	0.075												0.07		0.7	1.5	0.45	0.9	0.15	0.4
Process	65nm G+												65nm LP		180nm	130nm	130nm	45nm	90nm	90nm
f_s (MHz)	1300			1600			1920			2400			500	1152	640	640	900	4000	500	640
OSR	128	64	32	128	64	32	64	48	32	64	48	32	64	32	32	16	22.5	16	10	32
BW (MHz)	5.08	10.2	20.3	6.25	12.5	25	15	20	30	18.8	25	37.5	3.9	18	10	20	20	125	25	10
f_{in} (MHz)	1*	1*	3.5*	1*	2.3*	4.9*	2.3*	3.5*	5*	3.5*	4.9*	7.49*	1*	2.3*	2.4	3.68	2	41	2	2
SNR (dB)	76	74	70	76	75	71	75	74	71	76	74	71	71.5	70	84	76	81.2	65.5	64	
SNDR (dB)	75	73	69	75	74	70	74	73	70	74	73	70	71	67.3	82	74	78.1	65	63.5	65
DR (dB)	78	76	71	80	77	72	78	76	72	78	76	73	70	68	84	80	81.2	70	68	67
THD (dB)	81	79	80	82	82	79	81	80	77	79	80	76						74		
SFDR (dB)	82	82	82	83	83	80	82	81	78	81	81	77							81	72
Power Supply (V)	0.9			1.0			1.1			1.2			2.5/1.2	2.5/1.2	1.8	1.2	1.5	1.1/1.8	1.2	1.2
Power Total (mW)	11.5			17.5			26			39			8	17	100	20	87	256	8	6.8
Power Analog (mW)	3			4			5			7			2.5	5						
Power Digital (mW)	8.5			13.5			21			32			5.5	12						
FOM (dB) **	161	162	161	161	163	162	162	162	161	161	161	160	158	158	162	164	162	152	158	157
FOM2 (fJ/conv) ***	246	155	123	305	171	135	212	178	168	254	214	201	354	249	486	122	331	705	131	234

*** Worst-case input frequency value over stated BW (SNDR remains unchanged or improves at higher f_{IN} values)**
**** FOM (SNDR) = SNDR + 10 $\log_{10}$(BW/Power)**
***** FOM2 = Power / (2BW*2^ENOB)**

Fig. 18. Performance table with comparison to relevant prior ADCs.

on the IC. The IC has three power domains that connect to the single power supply via three sets of power and ground pins: one for the V/I circuits, one for the ring samplers and associated clock buffers, and one for all other circuit blocks.

Both $\Delta\Sigma$ modulators on 4 copies of the IC were tested. Four of the $\Delta\Sigma$ modulators had 1 to 3 dB worse-than-typical SNDR because of second-order distortion. The variability was traced to gain mismatches among the pseudo-differential signal path halves resulting from the unfortunate choice of short-length degeneration resistors in the V/I circuits. This gain mismatch theory was verified experimentally by modifying the NLC data (via the serial port interface) to compensate for the gain mismatches, after which all the $\Delta\Sigma$ modulators exceeded typical performance. Simulations indicate that wider and longer degeneration resistors would result in negligible variability without introducing other problems.

Fig. 13 shows typical measured output PSD plots with and without calibration enabled for $f_s = 2.4$ GHz. The results indicate that without calibration the SNDR over an 18.75 MHz signal band is 50 dB and that calibration increases the SNDR to 74 dB. The $1/f$ noise corner occurs at a frequency of approximately 800 kHz which is roughly twice that predicted by simulations.

Figs. 14 and 15 show measured decimation filter output sequences (as opposed to the simulated $\Delta\Sigma$ modulator output sequences shown in Fig. 8) with and without the ORC blocks enabled for sinusoidal $\Delta\Sigma$ modulator input signals large enough to cause $1 - z^{-1}$ block roll-overs. They correspond to cases where the input signal is below and above the ORC block clipping levels, respectively.

Fig. 16 shows measured harmonic distortion performance of the $\Delta\Sigma$ modulator with $f_s = 2.4$ GHz. The bottom plot in the figure shows signal-to-third-order distortion (HD3) ratios before and after calibration and signal-to-fifth-order distortion (HD5) ratios after calibration for several -3 dBFS single tone input signals between 1 MHz and 15 MHz. The -3 dBFS input level was chosen because it corresponds to the $\Delta\Sigma$ modulator's peak SNDR. The HD5 ratios were not noticeably affected by calibration, so only the post-calibration HD5 ratios are shown. The top plot in the figure shows a measured output PSD plot corresponding to one pair of HD3 and HD5 measurements. The HD3 and HD5 ratios after calibration are greater than 81 dB up to about 19 MHz. Above 19 MHz the HD3 term starts to roll off at 20 dB per decade, although it remains greater than 77.5 dB throughout the maximum signal bandwidth of 37.5 MHz. Two-tone harmonic distortion tests yielded comparable results.

Fig. 17 shows plots of the SNR and SNDR versus amplitude of 7.49 MHz sinusoidal input signals measured over a 37.5 MHz signal bandwidth with $f_s = 2.4$ GHz. The input signal frequency represents a worst-case situation because it is nearly the largest frequency for which the fifth harmonic falls within the 37.5 MHz signal bandwidth. The peak SNR, peak SNDR, and DR for this case are 70 dB, 69 dB, and 73 dB, respectively.

Measurements of the types described above with multiple values of f_s ranging from 1.3 GHz to 2.4 GHz, several signal bandwidths, and signal frequencies corresponding to worst-case performance are tabulated in Fig. 18. The figure also tabulates data from comparable published state-of-the-art $\Delta\Sigma$ modulators. A comparison indicates that the new $\Delta\Sigma$ modulator achieves state-of-the-art FOM performance, yet exceeds the previously published state-of-the-art in terms of area and reconfigurability. Furthermore, as explained in [13], it is less sensitive to clock jitter and far more amenable to implementation in digitally-optimized CMOS processes than typical conventional $\Delta\Sigma$ modulators.

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