16.4 A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator

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A digitally background calibrated ring oscillator ADC ΔΣ modulator is presented that consists mostly of digital circuitry. It does not contain analog integrators, feedback DACs, comparators, or reference voltages, and does not require a low-jitter clock. Unlike conventional ΔΣ modulators, its performance depends mainly on the speed of its digital circuitry, so it works best in IC processes optimized for fast digital circuitry. A 65nm LP CMOS prototype is presented with comparable performance to and much lower area than previously published ΔΣ modulators.

As shown in [1], a voltage-controlled ring oscillator (VCRO) with its inverters sampled at the desired output sample-rate followed by a phase decoder and digital differentiator is equivalent to a 1st-order ΔΣ modulator. However, VCRO nonlinearity and the high spurious tone content of 1st-order ΔΣ quantization noise have limited the approach to date. Until now it has only yielded good performance when used as the last stage of an otherwise conventional ΔΣ modulator, which requires high-accuracy analog circuitry and a low-jitter clock [2]. The ΔΣ modulator reported here avoids these issues via new digital background calibration and self-cancelling dither techniques.

The ΔΣ modulator consists of a signal converter (Fig. 16.4.1) and a calibration unit (Fig. 16.4.2). The signal converter consists of two VCRO paths that each contain a differential voltage-to-current (*V/I*) circuit, a pair of 15-element current-controlled ring oscillators (ICROs), and digital processing blocks. The inverters in each ICRO are sampled at the output sample-rate, f_s, and the resulting 30-bit sequence is converted to a 5-bit ICRO phase sequence, digitally differentiated, and applied to a look-up-table-based nonlinearity correction (NLC) block. The outputs of the two NLC blocks in each VCRO path are differenced, and the resulting f_s-rate sequence is added to that of the other VCRO path to form the ΔΣ modulator output. A dither sequence with an update-rate of $f_s/8$ is added to the input of each ICRO via one of two 4-level current-steering DACs to suppress spurious tones in the quantization noise.

The four-ICRO architecture facilitates dither cancellation and even-order distortion suppression. The dither is added positively in one of the VCRO paths and negatively in the other path, so it is largely cancelled when the two VCRO path outputs are summed. The two ICROs in each VCRO path are driven differentially to partially suppress 2nd-order distortion, which simplifies the NLC blocks by reducing the accuracy with which 2nd-order distortion must be suppressed.

The calibration unit (Fig 16.4.2) measures the 2nd and 3rd order distortion coefficients of a replica ICRO using a modified version of the technique described in [3]. A 4-level digital calibration sequence with an update-rate of $f_s/64$ is added to the ICRO input via a current-steering DAC. The calibration sequence is $t_1[n]+t_2[n]+t_3[n]$ where the $t_i[n]$ sequences are 2-level, independent, zero-mean, pseudo-random sequences. The ICRO output is sampled, differentiated, and correlated against the three 2-level sequences: $t_1[n]$, $t_1[n]\times t_2[n]$, and $t_1[n]\times t_2[n]\times t_3[n]$. Each correlator multiplies the f_s-rate differentiator output by one of the $f_s/64$-rate 2-level sequences and successively sums 2^{28} samples of the f_s-rate result. The 2nd and 3rd order distortion coefficients are calculated from the three correlator outputs, and the NLC blocks in Fig. 16.4.1 are updated with the coefficients at a rate of $f_s/2^{28}$. Hence, the required initial calibration time is $2^{28}/f_s$ (233ms for f_s=1.152GHz).

The calibration unit also contains a loop that locks the zero-input frequency of the ICRO to the f_s-rate clock via digital control of a replica *V/I* circuit. The same digital control signal is applied to the *V/I* circuits in Fig. 16.4.1. This maximizes the dynamic range about which each ICRO frequency can vary as a function of the ΔΣ modulator input voltage, and makes it possible to vary f_s from 0.5 to 1.15 GHz without losing dynamic range.

An open-loop V/I circuit could have been used and linearized via digital calibration along with the ICRO, but a closed loop V/I circuit (Fig. 16.4.3) without digital calibration was found to have lower overall power and area consumption because it simplifies the 4-level DACs. The *V/I* circuit operates from a 2.5V supply, so it consists of all thick-oxide devices. It uses a telescopic cascode op-amp with an open-loop gain and a unity-gain bandwidth of 50dB and 2.3GHz, respectively. Simulations with layout-extracted parasitics indicate that nonlinear distortion from the *V/I* circuit is at least 20dB less than that of the overall ΔΣ modulator regardless of input signal frequency.

Each ICRO is a ring of 15 current-starved pseudo-differential inverters (Fig. 16.4.3). The ring sampler latches the inverter outputs on the rising edge of each f_s-rate clock, and the phase decoder calculates a corresponding instantaneous phase number by identifying which pair of adjacent inverters have both top or bottom output samples of zero. The scheme ensures that the phase estimate depends only on high-to-low transitions of the inverter outputs, which reduces ICRO amplitude-modulation-induced phase quantization step-size mismatches.

The mostly-digital ΔΣ modulator is much less sensitive to clock jitter than most wideband continuous-time ΔΣ modulators because it does not contain feedback DACs. Jitter-induced ring sampler error is suppressed in the signal band because it is subjected to 1st-order highpass shaping by the differentiators, and jitter-induced DAC error largely cancels along with the dither in the signal converter. In contrast, jitter-induced 1st-stage feedback DAC error in a conventional continuous-time ΔΣ modulator is neither highpass shaped nor cancelled. Most of the published wideband continuous-time ΔΣ modulators use current-steering feedback DACs whose pulse widths and pulse positions are subject to clock jitter so they require very low-jitter clocks [4].

Each IC contains two ΔΣ modulators that share a common calibration unit with a combined area of 0.14mm^2. All the blocks in Fig. 16.4.1 and Fig. 16.4.2 are implemented on-chip except for the $f_s/2^{28}$-rate coefficient calculation block. A schedule problem just prior to tapeout prevented on-time completion of this block so it is implemented off-chip. It has since been laid out for a new version of the IC and found to increase the overall area by 0.004mm^2 with negligible incremental power consumption.

Both ΔΣ modulators on 5 copies of the IC were tested with no noticeable performance differences. Figure 16.4.4 shows representative measured output PSDs, Fig. 16.4.5 shows various measured SNDR, SNR, and IMD plots, and Fig. 16.4.6 summarizes measured performance relative to comparable state-of-the-art ΔΣ modulators. As implied in Fig. 16.4.6, quantization noise, which depends on digital circuit speed, limits performance rather than thermal noise, and the *V/I* circuits account for less than a third of the total power dissipation. Therefore, while this work demonstrates benefits over conventional ΔΣ modulators in the 65nm LP CMOS process, the approach is expected to be even more beneficial with more highly-scaled CMOS technology.

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 978-1-4244-6034-2/10/$26.00

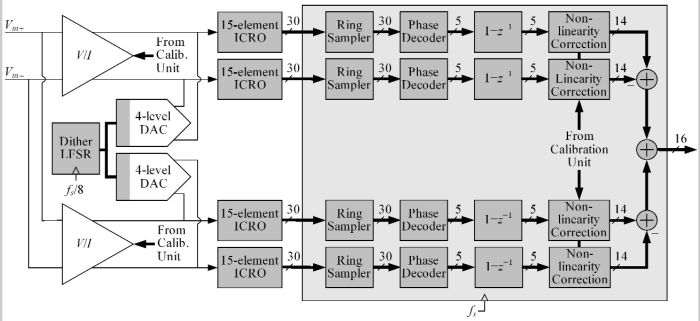

Figure 16.4.1: Signal converter portion of the ΔΣ modulator.

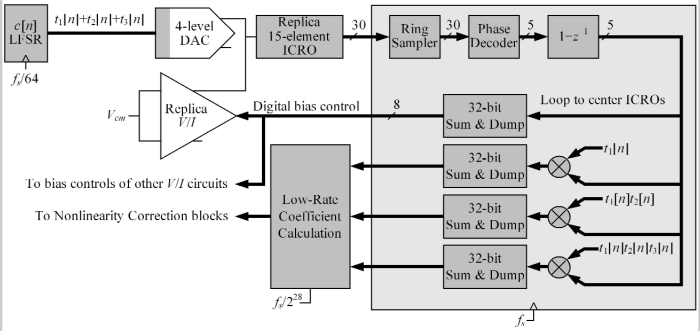

Figure 16.4.2: Calibration unit portion of the ΔΣ modulator.

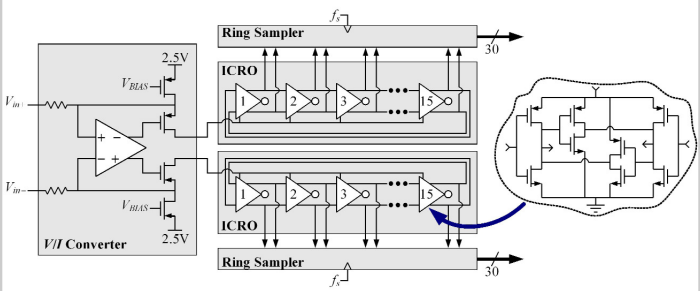

Figure 16.4.3: Simplified diagram of the V/I and ICRO circuits.

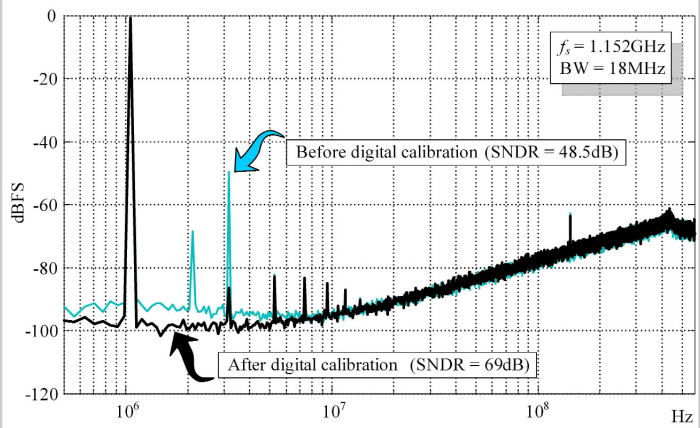

Figure 16.4.4: Measured PSD plots of the ΔΣ modulator.

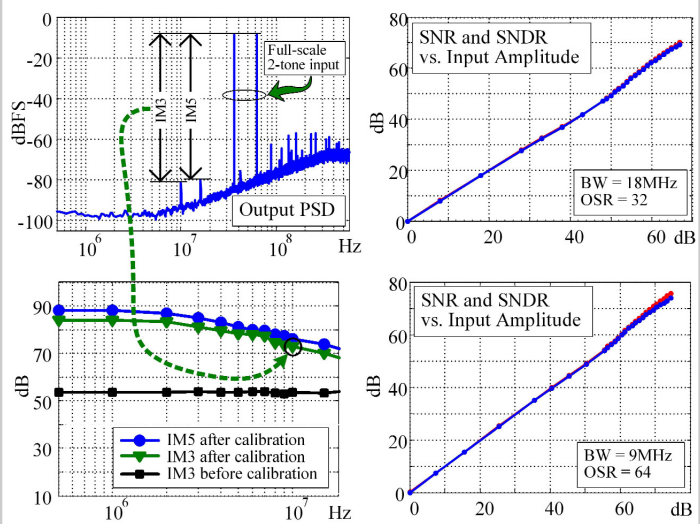

Figure 16.4.5: Measured PSD, IMD, SNR, and SNDR versus frequency and amplitude with f_s=1.152GHz

	This Work							ISSCC08 Paper 27.6	ISSCC06 Paper 3.1	ISSCC09 Paper 9.5	ISSCC09 Paper 9.7
Area (mm^2)	0.07							0.7	1.5	0.45	0.15
Process	65nm							180nm	130nm	130nm	65nm
f_s (MHz)	1152†						500	640	640	900	250
OSR	32			64		128	64	32	16	22.5	12.5
BW (MHz)	18			9		4.5	3.9	10	20	20	20
f_{in} (MHz)	1	2.3	5	1	2.3	1	1	2.4	3.68	2	3.9
SNR (dB)	70	70	70	76	76	80	71.5	84	76	81.2	62
SNDR (dB)	69	67.3	67*	73	72*	77.8*	71*	82	74	78.1	60
Power (mW)	17‡	17	17	17	17	17	8	100	20	87	10.5
FOM**	159	157.5	157*	160	159*	162*	157.9*	162	164	161.7	152.7

† Maximum frequency limited by test board FPGA used for data acquisition
‡ Analog (*V/I* circuits and DACs): 5mW, Digital: 12mW
* Worst-case value over stated BW (SNDR remains unchanged or improves at higher f_{in} values)
** FOM ≡ SNDR + $10\log_{10}$(BW/Power)

Figure 16.4.6: Performance table and comparison to prior work.

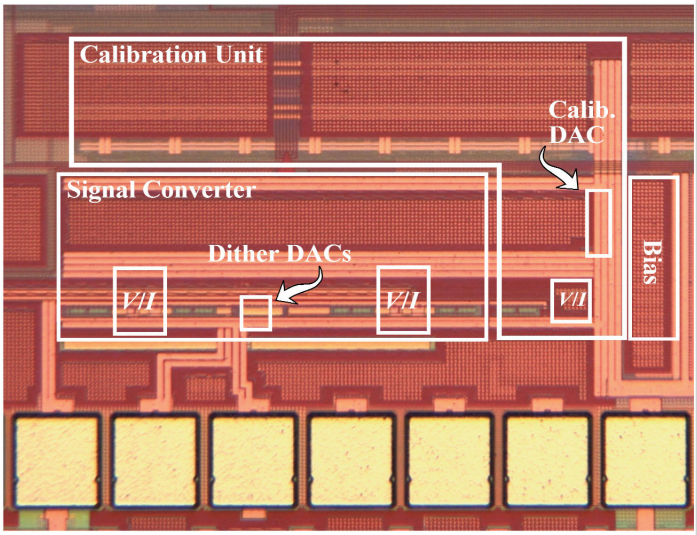

Figure 16.4.5: Die micrograph.

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