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9.1 A 130mW 100MS/s Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction

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A pipelined ADC is presented with 2 fully integrated digital background calibration techniques: harmonic distortion correction (HDC) to compensate for residue amplifier gain error and nonlinearity, and DAC noise cancellation (DNC) to compensate for DAC capacitor mismatches [1,2]. It is the first IC implementation of HDC, and the results demonstrate that HDC and DNC together enable reductions in power dissipation relative to comparable conventional state-of-the-art pipelined ADCs.

HDC is one of two recently proposed techniques that digitally measure and cancel ADC errors caused by residue-amplifier distortion to permit higher-distortion and, thus, lower-power residue amplifiers in pipelined ADCs [1,3]. The benefit of HDC relative to the technique of [3] is that it works for any pipelined ADC input signal [1]. It requires an increase in the resolution of the DAC in each pipeline stage to which it is applied, but as described below this is achieved without significantly increasing the area or power dissipation of the ADC.

The ADC consists of five 9-level stages with a nominal residue amplifier gain of 4, and a 17-level 6th stage (Fig. 9.1.1). HDC and DNC are applied to the first 3 stages because the performance of these stages most critically affects ADC performance. DNC is as described in [2], so only HDC is described below.

Each stage with HDC contains a 65-level DAC with a step-size of $\Delta/8$ where Δ is the step-size of the stage's flash ADC. A calibration sequence $c_k[n]=t_{1,k}[n]+t_{2,k}[n]+t_{3,k}[n]$, k=1,2, or 3, is added after the flash ADC of the k^{th} stage, where $t_{1,k}[n]$, $t_{2,k}[n]$, and $t_{3,k}[n]$ are uncorrelated zero-mean pseudo-random sequences that each take on values of $\pm\Delta/16$ referred to the DAC's output. As shown in Fig. 9.1.1, $c_k[n]$ is converted to analog and passed through the residue amplifier along with the stage's residue using a portion of the overrange margin.

Ideally, $c_k[n]$ would be cancelled in the digital recombination logic along with error from the flash ADC. However, residue amplifier gain error and nonlinearity cause extra terms that are functions of both flash ADC error and $c_k[n]$ to appear in the digitized residue at the input to the stage's divide-by-4 block. For example, 3rd-order distortion causes a term proportional to $\alpha_{3,k}t_{1,k}[n]t_{2,k}[n]t_{3,k}[n]$ in the digitized residue, where $\alpha_{3,k}$ is the 3rd-order distortion coefficient of the k^{th} residue amplifier. This term is uncorrelated with other terms in the digitized residue, so multiplying the digitized residue by $t_{1,k}[n]t_{2,k}[n]t_{3,k}[n]$ and averaging yields an estimate of $\alpha_{3,k}$ that can be used to digitally cancel all the error terms from the residue amplifier's 3rd-order distortion. The k^{th} HDC block (Fig. 9.1.2) does this, and similarly estimates and compensates for the amplifier's gain error, $\alpha_{1,k}$ [1]. It was found from circuit simulation during design that only gain error and 3rd-order distortion limit overall performance if left uncorrected, so other orders of residue amplifier distortion are not corrected.

The 65-level DAC is the most critical component for HDC. Any nonlinear distortion it introduces must be negligible compared to that from the residue amplifier so as not to degrade the HDC estimates of $\alpha_{1,k}$ and $\alpha_{3,k}$. Furthermore, its latency must be low so as not to significantly reduce the time available for the residue amplifier to settle. These objectives are achieved by combining the $c_k[n]$ adder with a dynamic-element-matching (DEM) encoder of the type presented in [4], and collapsing the critical paths of the digital logic into 2 layers of transmission gates. The DAC and $c_k[n]$ adder together consist of the modified DEM encoder followed by 14 1b DACs with weights of $\Delta/8$, $\Delta/4$, $\Delta/2$, and Δ (Fig. 9.1.3). The DEM encoder scrambles the usage pattern of the 1b DACs via 13 pseudo-random bit sequences to convert nonlinear distortion that would otherwise arise from capacitor mismatches, into white noise.

The idea behind the DEM encoder modification is to provide each $c_k[n]$ sample to the DEM encoder a clock period before the corresponding flash ADC output sample. The input bits to the 6 smallest 1b DACs are independent of the flash ADC output, so the DEM encoder has a full clock period to calculate them. Exactly p[n]+q[n] of the input bits to the largest eight 1b DACs must be set high, where p[n] is the sum of the 8 thermometer code bits from the flash ADC, and q[n] takes on values of 1, –1, and 0 depending on $c_k[n]$. The first layer of transmission gates in the DEM encoder (Fig. 9.1.3) adds p[n] and q[n], and the second layer scrambles the usage pattern of the largest eight 1b DACs. Hence, the latency associated with the $c_k[n]$ adder and DEM is 2 transmission gate delays.

HDC only compensates for residue amplifier error, so care is taken to prevent other non-idealities from limiting performance. Passive sampling is used to avoid using a sample-and-hold amplifier [2,5]. Bootstrapped switches as in [2] are used to reduce switch nonlinearity where necessary. Separate sampling and DAC capacitors are used to avoid signal-dependent loading of the on-chip reference voltage generators. If the capacitors were shared, kT/C noise would be reduced but lower-impedance reference generators with much higher power dissipation would be required.

Conventional switched-capacitor techniques are used with low-current 2-stage opamps. To reduce design and layout time, successive stages are not aggressively scaled or individually optimized for minimum power dissipation. The 1st-stage residue amplifier's simulated loop gain is 23dB at DC with a unity gain frequency of 200MHz, and its bias current is 4.8mA. As expected, given the loop gain's low amplitude and bandwidth, the measured –1dBFS SNDR of the ADC prior to correction by HDC is 43dB. As indicated in Fig. 9.1.4, HDC and DNC increase this value by 26dB, of which DNC accounts for about 4dB.

HDC operates in the background during normal operation of the pipelined ADC, so it adapts to environmental changes without interrupting normal ADC operation. However, initial HDC convergence with a worst-case (i.e., full-scale) ADC input signal requires 130s in this design. Although not implemented, simulations indicate that an auto-calibration mode with no changes to HDC except for zeroing the input signal and using $4c_k[n]$ in place of $c_k[n]$ in each of the first 3 stages would reduce the initial convergence time to less than 1s.

Three test boards are populated and used to obtain the measured data in Figs. 9.1.4 and 9.1.5. Figure 9.1.4 shows worst-case results both with nominal and reduced supply voltages. A mistake found after tapeout prevents HDC convergence for small ADC input signals, but simulations confirm that the problem can be eliminated by a metal mask change in the digital circuitry. Normally, HDC continually updates its coefficients, but it can optionally freeze the coefficients after convergence. Measurements with frozen coefficients for numerous input signals, including small input signals, indicate that full performance is achieved in all cases. As shown in Fig. 9.1.6, the FOM values achieved by the ADC are better than those of previously published ADCs with comparable bandwidth and SNDR performance. A die micrograph is shown in Fig. 9.1.7.

References:

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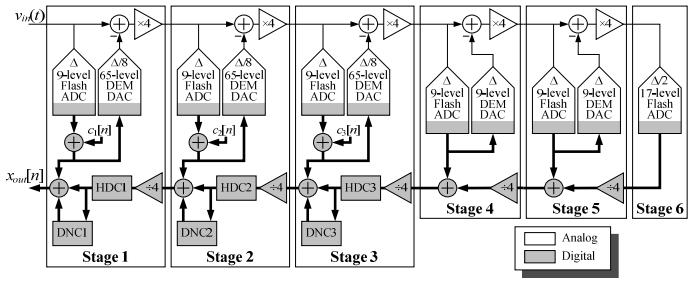

Figure 9.1.1: High-level diagram of the pipelined ADC integrated circuit (pipeline delays not shown).

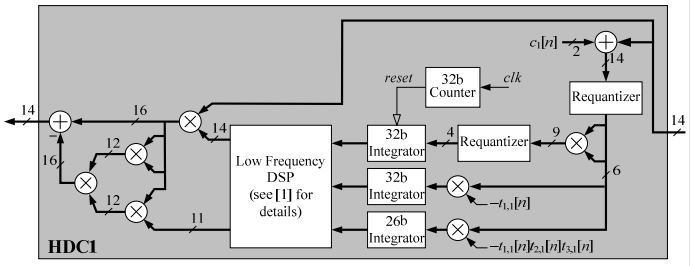

Figure 9.1.2: Details of the stage-1 HDC logic (stages 2 and 3 are similar).

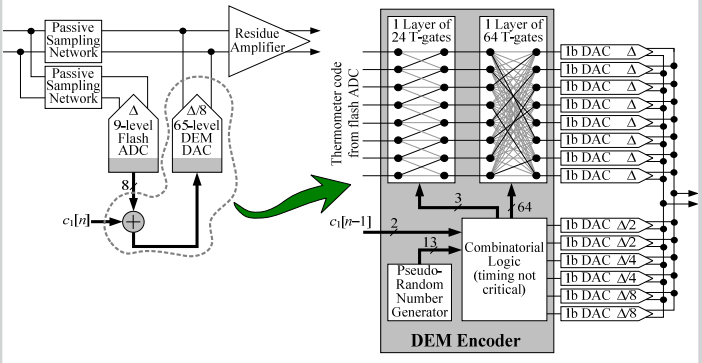

Figure 9.1.3: Additional details of stage 1 (stages 2 and 3 are similar).

Design Details								
Technology	90nm CMOS							
Package	56-pin QFN							
Die Size Including Pads and ESD Protection	2.15×3.35mm^2							
Active Area	4 mm^2							
Digital Calibration	on-chip							
Voltage References	on-chip							
Worst-Case Measured Results Over Nyquist Band for f_s = 100MHz								
Power Supplies	V_{DD} Test Case 1				V_{DD} Test Case 2			
	V_{DD}	Power Dissipation			V_{DD}	Power Dissipation		
Analog	1.2V	93mW	130mW		1.0V	62mW	92mW	
Digital	1.0V†	17mW			0.7V†	7mW		
Clock Generator	1.0V	1mW			1.0V	1mW		
Clock Drivers and DEM	1.35V‡	19mW			1.35V‡	22mW		
Input and References								
Input Voltage Range	1.5V$_{pp\text{-}diff}$				1.25 V$_{pp\text{-}diff}$			
Internal V_{refp} / V_{refn}	950mV / 265mV				775mV / 225mV			
Performance with HDC and DNC On								
Peak *SNR*	70dB				68.3dB			
SNDR at −1dBFS	68.8dB				66.6dB			
SFDR at −1dBFS	85dB				75dB			
2-tone *SFDR* at −1dBFS	86dB				80dB			
Maximum *INL*	3.6 LSB				3.8 LSB			
Maximum *DNL*	0.54 LSB				0.39 LSB			
Performance with HDC and DNC Off								
SNDR at −1dBFS	43.3dB				47.3dB			
SFDR at −1dBFS	52.3dB				58dB			
Performance with HDC on and DNC Off								
SNDR at −1dBFS	64.6dB				64.3dB			
SFDR at −1dBFS	85dB				75dB			

† The digital circuitry works reliably and full ADC performance is achieved provided this V_{DD} is at least 0.6V.
‡ When this V_{DD} is set to its targeted design value of 1.2V, the peak *SNDR* decreases by approximately 3dB. Although not predicted by simulations, the authors believe that the clock drivers have insufficient strength to achieve full ADC performance at 1.2V.

Figure 9.1.4: Performance summary.

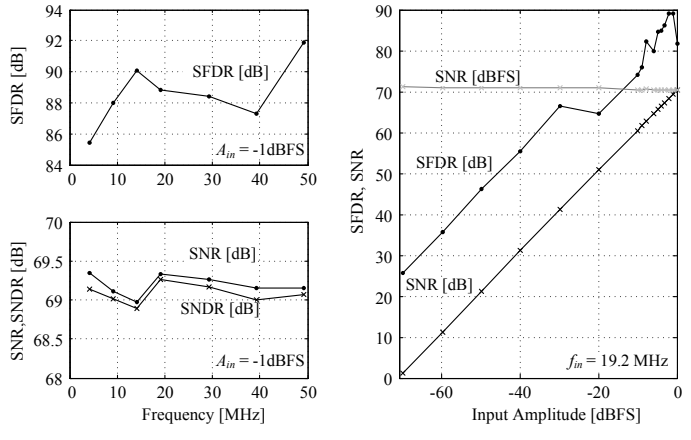

Figure 9.1.5: Measured SFDR, SNR, and SNDR versus frequency and amplitude.

Reference or Part Number	f_s (MS/s)	*SNDR* (dBFS)	*SFDR* (dB)	V_{DD} (V)	P_{tot} (mW)	*FOM*1 (pJ/step)	*FOM*2 (pJ·V/step)	Residue Amplifier Type
[3]	75	68	76	3	314	2.04	6.12	S-C
LTC2229	80	71.6	90	3	211	0.85	2.54	S-C
AD9233	80	70.5	90	1.8	248	1.13	2.03	S-C
ADS6123	80	72.3	89	3.3	318	1.18	3.89	S-C
LTC2252	105	712	88	3	320	1.03	3.08	S-C
AD9233	105	70.5	90	1.8	320	1.11	2.00	S-C
ADS6124	105	72.3	84	3.3	374	1.06	3.49	S-C
[6]	250	65.9	82	1.8	150	0.37†	0.67	BBD
This work	100	69.8	85	1.2	130	0.52	0.62	S-C
This work	100	67.6	75	1.0	92	0.47	0.47	S-C

$$FOM1 = \frac{P_{tot}}{2^{ENOB} f_s} \quad \text{and} \quad FOM2 = FOM1 \times V_{DD} \quad \text{where} \quad ENOB = \frac{SNDR - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

Figure 9.1.6: Comparison to prior work.

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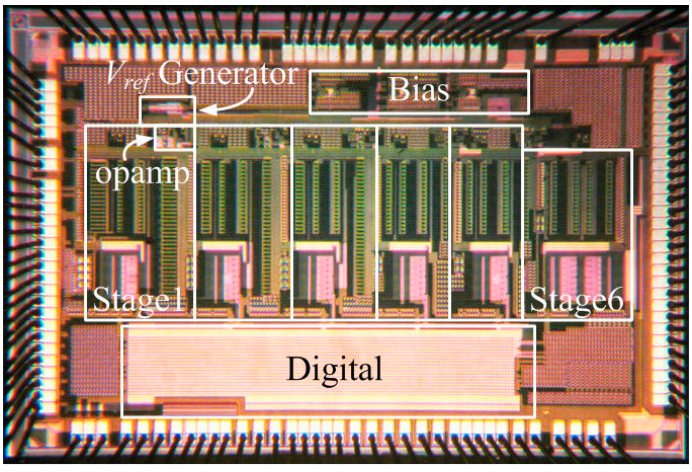

Figure 9.1.7: Die micrograph.

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