Segmented Dynamic Element Matching for High-Resolution Digital-to-Analog Conversion

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***Abstract*—Dynamic element matching (DEM) is widely used in multibit digital–analog converters (DACs) to prevent mismatches among nominally identical components from introducing nonlinear distortion. It has long been used as a performance-enabling technique in delta-sigma data converters which require low-resolution but high-linearity DACs. More recently, segmented DEM architectures have made high-resolution Nyquist-rate DEM DACs practical. However, the previously published segmented DEM DAC designs have been ad hoc. Systematic techniques for synthesizing segmented DEM DACs and analyses of their design tradeoffs have not been published previously. This paper quantifies a fundamental power dissipation versus complexity tradeoff implied by segmentation and provides a systematic method of synthesizing segmented DEM DACs that are optimal in terms of the tradeoff.**

***Index Terms*—Digital-to-analog conversion, dynamic element matching (DEM), segmentation.**

I. Introduction

In a dynamic element matching (DEM) digital-to-analog converter (DAC), a *DEM encoder* maps a digital input sequence to multiple 1-b output sequences, each of which drives a 1-b DAC. The outputs of the 1-b DACs are summed to form the output of the DEM DAC. If the 1-b DACs are nominally identical, then the structure is called a *unity-weighted* DEM DAC. In this case, for most input values, there are several sets of DEM encoder output bit values that would result in the same DEM DAC output pulse in the absence of mismatches among the 1-b DACs. The DEM encoder exploits this *redundancy* to scramble the usage pattern of the 1-b DACs from sample to sample such that the error waveform resulting from mismatches among the 1-b DACs has a noise-like structure that is free of nonlinear distortion and spurious tones and has either a white or shaped power spectral density (PSD).

Such DEM DACs have long been used as enabling components in delta-sigma data converters which require low-resolution but high-linearity DACs [1]–[27]. However, their complexity grows exponentially with the number of bits of DAC resolution so they are not practical as high-resolution Nyquist-rate DACs. Instead, high-resolution Nyquist-rate DACs are often implemented with 1-b DACs of different weights, and DEM is applied only to the set of 1-b DACs with the maximum weight [28]–[31]. The rationale is that the 1-b DACs with the largest weight contribute the bulk of the mismatch error. However, mismatch-induced errors from the other 1-b DACs as a group are still significant, particularly pulse shape and timing errors, so the approach is only a partial solution.

Recently, *segmented* DEM DACs have been developed that overcome this problem [32]–[37]. Segmented DEM DACs have the same general structure as their unity-weighted counterparts except that the 1-b DAC weights are not all equal and their DEM encoders function somewhat differently. By having groups of 1-b DACs with equal weights, yet having the weights of the 1-b DACs in each group be larger than those of the previous group, sufficient redundancy can be retained for DEM to be effective without having complexity that grows exponentially with the number of input bits. Given two DEM DACs capable of handling the same range of input values, the one with fewer 1-b DACs is said to have the *higher level of segmentation*. Typically, a higher level of segmentation implies lower DEM encoder complexity but a higher ratio of the largest to smallest 1-b DAC weights.

Unfortunately, each segmented DEM DAC published to date has incurred a penalty in return for the complexity reduction achieved by segmentation: the error resulting from mismatches is free of nonlinear distortion only if the range of values taken on by the input sequence is restricted relative to the set of all possible input values. Moreover, at least for the DEM DACs published to date, the higher the level of segmentation, the more the range must be restricted. For example, the DEM DAC with highest level of segmentation published to date can handle an input sequence which takes on any of 32 767 values, but it is necessary to restrict the input sequence to the middle 16 385 values of this range to ensure that the error resulting from mismatches is free of nonlinear distortion [36]. This corresponds to a 6-dB reduction in signal swing. In terms of the signal-to-noise ratio (SNR), the signal-swing reduction can be compensated by reducing the circuit noise from the 1-b DACs by 6 dB, but doing so usually dictates a significant increase in power dissipation. Therefore, the published DEM DACs suggest that segmentation represents a tradeoff between circuit complexity and power dissipation.

Nevertheless, the previously published work on DEM DACs does not address whether the range restriction problem men-

Manuscript received January 24, 2008; revised April 25, 2008. First published nulldate; current version published December 12, 2008. This work was supported by the National Science Foundation under Award 0515286, by the UCSD Center for Wireless Communications and by the University of California Discovery Program. This paper was recommended by Associate Editor M. Delgado-Restituto.

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Digital Object Identifier 10.1109/TCSI.2008.2001757

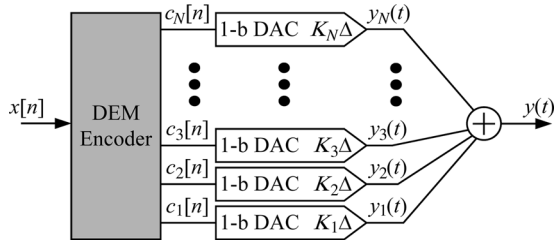

Fig. 1. High-level system diagram of a general DEM DAC.

tioned above is a fundamental limitation of segmentation or just a limitation of the particular published DEM DAC designs. Moreover, while specific segmented DEM encoders have been described, methods of synthesizing segmented DEM encoders and analyses of their tradeoffs have not been presented. This paper addresses these issues. It proves that the range restriction problem is an unavoidable side effect of segmentation, and quantifies the optimal range that can be achieved by a segmented DEM DAC for each possible set of 1-b DAC weights. It also provides a method of synthesizing segmented DEM DACs that achieve the optimal input range.

II. General DEM DAC

A. Ideal Behavior

The input to a DAC is a sequence of digital codewords, each of which is interpreted by design convention to have a numerical value. In this paper these numerical values are assumed without loss of generality to be integer multiples of a constant Δ, where Δ is called the minimum *step-size* of the input sequence.

A general DEM DAC architecture is shown in Fig. 1. It consists of an all-digital block called a *DEM encoder*, followed by N 1-b DACs. Ideally, during the nth sample period, i.e., $nT \le t < (n+1)T$, the output of the ith 1-b DAC is

$$y_i(t) = \begin{cases} K_i \frac{\Delta}{2} a(t-nT), & \text{if } c_i[n] = 1 \\ -K_i \frac{\Delta}{2} a(t-nT), & \text{if } c_i[n] = 0 \end{cases} \tag{1}$$

where $c_i[n]$ is the input to the 1-b DAC, K_i is the *weight* of the 1-b DAC, and $a(t)$ is an analog pulse that is zero outside of $0 \le t < T$. By definition, $K_1 = 1$ and each K_i for $i = 2, 3, \ldots, N$ is a positive integer ordered such that $K_i \ge K_{i-1}$. The DEM encoder is designed to satisfy

$$x[n] = \Delta \sum_{i=1}^{N} K_i \left(c_i[n] - \frac{1}{2} \right) \tag{2}$$

where $x[n]$ is the digital input sequence to the DEM encoder. Therefore, the set of possible input values depends on the number of 1-b DACs and their weights. With the ideal 1-b DAC behavior given by (1), it follows from (2) and Fig. 1 that the output of the DEM DAC during the nth sample period is

$$y(t) = x[n] a(t - nT). \tag{3}$$

It can be shown from (2) that, if

$$K_i \le \sum_{m=1}^{i-1} K_m + 1 \tag{4}$$

for $i = 2, 3, \ldots, N$, then $x[n]$ can take on all values in the set

$$\left\{ -\frac{M}{2}\Delta, -\left(\frac{M}{2} - 1\right)\Delta, -\left(\frac{M}{2} - 2\right)\Delta, \ldots, \frac{M}{2}\Delta \right\} \tag{5}$$

where

$$M = \sum_{i=1}^{N} K_i. \tag{6}$$

If (4) is not satisfied, then the minimum and maximum possible values of $x[n]$ are still $-M\Delta/2$ and $M\Delta/2$, but some of the values in (5) between these two extremes are not possible, so the range of possible input values is *not contiguous*. Having a contiguous range of input values is desirable in most applications, so (4) is taken as a design requirement in this paper.

B. Behavior With Component Mismatches

In practice, mismatches among nominally identical components used to implement the 1-b DACs cause the ideal behavior given by (1) to degrade to

$$y_i(t) = \begin{cases} K_i \frac{\Delta}{2} a(t-nT) + e_{hi}(t-nT), & \text{if } c_i[n] = 1 \\ -K_i \frac{\Delta}{2} a(t-nT) + e_{li}(t-nT), & \text{if } c_i[n] = 0 \end{cases} \tag{7}$$

where $e_{hi}(t)$ and $e_{li}(t)$ are *mismatch error pulses* caused by the component mismatches. It is assumed in the remainder of the paper that the mismatch error pulses are nonzero only for the duration of the sample period. Otherwise, no assumptions are made about $e_{hi}(t)$ and $e_{li}(t)$. An equivalent form of (7) is

$$y_i(t) = \underbrace{\left(c_i[n] - \frac{1}{2} \right)}_{=\pm\frac{1}{2}} \alpha_i(t-nT) K_i \Delta + \beta_i(t-nT) \tag{8}$$

where

$$\begin{aligned} \alpha_i(t) &= a(t) + \frac{e_{hi}(t) - e_{li}(t)}{K_i \Delta} \\ \beta_i(t) &= \frac{e_{hi}(t) + e_{li}(t)}{2} \end{aligned} \tag{9}$$

which can be verified by substituting (9) into (8) to obtain (7).

The objective of DEM is to cause the DEM DAC's output signal to have the form

$$y(t) = x[n]\alpha(t - nT) + \beta(t - nT) + e_{\mathrm{DAC}}(t) \tag{10}$$

during the nth sample period for each n, where $\alpha(t)$ and $\beta(t)$ are pulses that are zero outside of $0 \le t < T$, and $e_{\mathrm{DAC}}(t)$ has a noise-like structure and satisfies

$$\begin{aligned} \mathrm{E}\{e_{\mathrm{DAC}}(t)\} &= 0 \\ \mathrm{E}\{e_{\mathrm{DAC}}(t) x[n]\} &= 0 \\ \mathrm{E}\{e_{\mathrm{DAC}}(t) e_{\mathrm{DAC}}(t+\tau)\} &= 0, \qquad \text{for all } |\tau| > T_1 \end{aligned} \tag{11}$$

where T_1 is some constant. Achieving this objective regardless of the mismatch error pulses ensures that the DAC does not introduce nonlinear distortion or spurious tones despite the mismatches among the 1-b DACs.

The three components of the DEM DAC's output signal in (10) are referred to as the *signal pulse sequence*, the *offset pulse sequence*, and the *DAC noise*, respectively. The signal pulse sequence consists of the analog pulses, $\alpha(t-nT)$, linearly scaled by the input sequence. The mismatch error pulses cause $\alpha(t)$ to deviate somewhat from the ideal pulse, $a(t)$, but in most applications this is not a serious problem because it has little effect on the SNR or spurious-free dynamic range (SFDR) of the overall DAC. The offset pulse sequence consists of the analog pulses, $\beta(t-nT)$. The offset pulses are identical from period to period, independent of $x[n]$. Consequently, they result only in spurious tones at multiples of the sample frequency, so they do not degrade the SNR or the in-band SFDR of the overall DAC. As explained in the remainder of the paper, provided the number of 1-b DACs and their weights are chosen with certain restrictions and then provided the input sequence stays within a certain range of values, the DEM encoder can be designed to ensure that the DAC noise satisfies (11).

C. Input Sequence Representation

In any practical DAC, each value of the input sequence is represented as a digital codeword. By design convention, each codeword is interpreted to represent one of the values in (5) as described above. This interpretation is useful when considering the behavior of the DEM DAC in the context of a larger signal processing system, such as a communication system, because it imparts a physical meaning to the input sequence in relation to the output waveform of the DAC as given by (10).

Nevertheless, (5) is a set of $M+1$ uniformly spaced numbers, so each of its values can be mapped to, and therefore represented by digital circuitry as, an unsigned integer in the range 0 to M given by

$$c[n] = \frac{x[n]}{\Delta} + \frac{M}{2}. \tag{12}$$

Hence, while the sequence of input codewords can be interpreted as a sequence of values $x[n]$ restricted to the set (5) as described previously, equivalently it can be interpreted as a sequence of values $c[n]$ restricted to the set of integers ranging from 0 to M. The latter interpretation is particularly convenient when designing the DEM encoder. With this interpretation, it follows from (12) that (10) can be written in terms of $c[n]$ as

$$y(t) = c[n]\alpha(t-nT)\Delta + \beta_c(t-nT) + e_{DAC}(t) \tag{13}$$

where

$$\beta_c(t) = \beta(t) - \alpha(t)\frac{M}{2}\Delta. \tag{14}$$

Furthermore, it follows from (12) that (11) holds if and only if

$$\begin{aligned} \mathrm{E}\{e_{\mathrm{DAC}}(t)\} &= 0 \\ \mathrm{E}\{e_{\mathrm{DAC}}(t)c[n]\} &= 0 \\ \lim_{\tau\to\infty} \mathrm{E}\{e_{\mathrm{DAC}}(t)e_{\mathrm{DAC}}(t+\tau)\} &= 0. \end{aligned} \tag{15}$$

Combining (2) and (12) gives

$$c[n] = \sum_{i=1}^{N} K_i c_i[n]. \tag{16}$$

Together with (6), this suggests the following physical interpretation of $c[n]$. In the absence of mismatches, the DEM DAC's output pulse during the nth sample period is the same as would be produced by adding the output pulses during the nth sample period of M 1-b DACs all of weight $K_1 = 1$, $c[n]$ of which have their input bits set to 1 and the rest of which have their input bits set to 0.

D. DEM DAC Decomposition

To analyze the DEM DAC shown in Fig. 1, it is convenient to decompose it into parallel combinations of smaller DEM DACs. The definition of these smaller DEM DACs is presented in the remainder of this section for use in the analyses that follow.

$\mathrm{DAC}^{(u,w)}$ *Definition:* For any integers u and w that satisfy $1 \le u \le w \le N$ and for which K_i is an integer multiple of K_u for each $i = u, u+1, u+2, \ldots, w$, $\mathrm{DAC}^{(u,w)}$ consists of an encoder followed by the uth through wth 1-b DACs of the DEM DAC shown in Fig. 1. The encoder maps a digital input sequence given by

$$c^{(u,w)}[n] = \frac{1}{K_u}\sum_{i=u}^{w} K_i c_i[n] \tag{17}$$

to the same 1-b sequences $c_u[n], c_{u+1}[n], \ldots, c_w[n]$ generated by the DEM encoder shown in Fig. 1. The output of $\mathrm{DAC}^{(u,w)}$ during the nth sample is

$$y^{(u,w)}(t) = \sum_{i=u}^{w} y_i(t). \tag{18}$$

□

Although $\mathrm{DAC}^{(u,w)}$ is not the full DEM DAC of Fig. 1, it nevertheless has the same general form as the DEM DAC of Fig. 1 except that $K_u \neq 1$ is permissible. Therefore, identical reasoning to that presented above for the full DEM DAC implies that $c^{(u,w)}[n]$ is restricted to the set

$$\left\{0, 1, \ldots, M^{(u,w)}\right\} \tag{19}$$

where

$$M^{(u,w)} = \frac{1}{K_u}\sum_{i=u}^{w} K_i. \tag{20}$$

In analogy with (13)–(15), if the output of $\mathrm{DAC}^{(u,w)}$ can be written as

$$\begin{aligned} y^{(u,w)}(t) =& c^{(u,w)}[n]\alpha^{(u,w)}(t-nT)\Delta \\ &+ \beta_c^{(u,w)}(t-nT) + e_{DAC}^{(u,w)}(t) \end{aligned} \tag{21}$$

during the nth sample period for each n, where $\alpha^{(u,w)}(t)$ and $\beta_c^{(u,w)}(t)$ are pulses that are zero outside of $0 \le t < T$, and

$$\begin{aligned} \mathrm{E}\left\{e_{\mathrm{DAC}}^{(u,w)}(t)\right\} &= 0 \\ \mathrm{E}\left\{e_{\mathrm{DAC}}^{(u,w)}(t)c^{(u,w)}[n]\right\} &= 0 \\ \mathrm{E}\left\{e_{\mathrm{DAC}}^{(u,w)}(t)e_{\mathrm{DAC}}^{(u,w)}(t+\tau)\right\} &= 0, \qquad \text{for all } |\tau| > T_1 \end{aligned} \tag{22}$$

hold, then the DAC noise from $\mathrm{DAC}^{(u,w)}$ is free of nonlinear distortion and spurious tones.

It follows from (17) and (18) that $c^{(i,i)}[n] = c_i[n]$ and $y^{(i,i)}(t) = y_i(t)$. Therefore, the special case of $\mathrm{DAC}^{(i,i)}$ is just the ith 1-b DAC. A comparison of (8) and (21) indicates that (21) holds with

$$\begin{aligned} \alpha^{(i,i)}(t) &= K_i \alpha_i(t) \\ \beta_c^{(i,i)}(t) &= \beta_i(t) - \frac{K_i}{2}\alpha_i(t)\Delta \\ e_{DAC}^{(i,i)}(t) &= 0. \end{aligned} \tag{23}$$

III. Range Restriction Versus Segmentation Tradeoff

This section presents the main results of the paper as two theorems and two corollaries. The proofs are deferred to the Appendix.

The first theorem quantifies the maximum input range that a DEM DAC can possibly have without the mismatch error pulses causing nonlinear distortion and spurious tones, and the first corollary presents an analogous result for $\mathrm{DAC}^{(u,w)}$. The second theorem provides the means by which DEM DACs that achieve such performance over the maximum input range can be synthesized. The second corollary provides the means by which expressions for the unit gain pulses and DAC noise of the synthesized DACs can be derived. The synthesis and analysis procedures that utilize the second theorem and second corollary are described in the next section.

Theorem 1: Suppose a DEM DAC has the form shown in Fig. 1, satisfies (7) and (16), and its DAC noise satisfies (15) provided

$$c[n] \in \{c_{\min}, c_{\min}+1, c_{\min}+2, \ldots, c_{\max}\} \tag{24}$$

for all n where $0 \le c_{\min} \le c_{\max} \le M$. If $K_{N-1} = K_N$ then

$$\begin{aligned} c_{\min} &\ge K_N - 1 \\ c_{\max} &\le M - K_N + 1. \end{aligned} \tag{25}$$

If $K_{N-1} \ne K_N$, then the Nth 1-b DAC can be removed and the DEM encoder modified to obtain a new DEM DAC with DAC noise that satisfies (15) provided (24) holds for all n with $c_{\max} - c_{\min}$ at least as large as in the original DEM DAC.

Corollary 1: If $\mathrm{DAC}^{(u,w)}$ with $w > u$ satisfies (7), $K_{w-1} = K_w$, and $e_{\mathrm{DAC}}^{(u,w)}(t)$ satisfies (22) provided

$$c^{(u,w)}[n] \in \left\{c_{\min}^{(u,w)}, c_{\min}^{(u,w)}+1, c_{\min}^{(u,w)}+2, \ldots, c_{\max}^{(u,w)}\right\} \tag{26}$$

for all n, then

$$\begin{aligned} c_{\min}^{(u,w)} &\ge K_w/K_u - 1 \\ c_{\max}^{(u,w)} &\le M^{(u,w)} - K_w/K_u + 1. \end{aligned} \tag{27}$$

Maximum Linear Range Definition: $\mathrm{DAC}^{(u,w)}$ is said to have *maximum linear range* if it satisfies the hypothesis of Corollary 1 and

$$\begin{aligned} c_{\min}^{(u,w)} &= K_w/K_u - 1 \\ c_{\max}^{(u,w)} &= M^{(u,w)} - K_w/K_u + 1. \end{aligned} \tag{28}$$

Theorem 2: Suppose $\mathrm{DAC}^{(u,v)}$ and $\mathrm{DAC}^{(v+1,w)}$ have maximum linear range, $K_u = K_{u+1} = \cdots = K_v$, and $e_{\mathrm{DAC}}^{(u,v)}(t)$ and $e_{\mathrm{DAC}}^{(v+1,w)}(t)$ are uncorrelated. Then $\mathrm{DAC}^{(u,w)}$ has maximum linear range if

$$c^{(v+1,w)}[n] = \frac{1}{K}\left(Gc^{(u,w)}[n] - b - s[n]\right) \tag{29}$$

and

$$c^{(u,v)}[n] = (1-G)c^{(u,w)}[n] + b + s[n] \tag{30}$$

where $K = K_{v+1}/K_u$,

$$G = K\frac{M^{(v+1,w)} - 2K_w/K_{v+1} + 2}{M^{(u,w)} - 2K_w/K_u + 2} \tag{31}$$

$$b = K\frac{(K_w/K_u - 1)M^{(v+1,w)} - (K_w/K_{v+1} - 1)M^{(u,w)}}{M^{(u,w)} - 2K_w/K_u + 2} \tag{32}$$

and

$$s[n] = \begin{cases} m \text{ or } m-K, & \text{if } m \ne 0 \\ 0, & \text{otherwise} \end{cases} \tag{33}$$

with

$$m = \left[Gc^{(u,w)}[n] - b\right] - K\left\lfloor \frac{Gc^{(u,w)}[n] - b}{K} \right\rfloor \tag{34}$$

is a random sequence that is zero-mean, uncorrelated with $c^{(u,w)}[n]$, $e_{\mathrm{DAC}}^{(u,v)}(t)$, and $e_{\mathrm{DAC}}^{(v+1,w)}(t)$, and

$$\lim_{k\to\infty} \mathrm{E}\{s[n]s[n+k]\} = 0. \tag{35}$$

Corollary 2: If $\mathrm{DAC}^{(u,v)}$ and $\mathrm{DAC}^{(v+1,w)}$ satisfy the hypothesis of Theorem 2 then

$$\alpha^{(u,w)}(t) = (1-G)\alpha^{(u,v)}(t) + \frac{1}{K}G\alpha^{(v+1,w)}(t) \tag{36}$$

and during the nth sample period

$$\begin{aligned} e_{\mathrm{DAC}}^{(u,w)}(t) = s[n]\left[\alpha^{(u,v)}(t-nT) - \frac{1}{K}\alpha^{(v+1,w)}(t-nT)\right]\Delta \\ + e_{\mathrm{DAC}}^{(u,v)}(t) + e_{\mathrm{DAC}}^{(v+1,w)}(t). \end{aligned} \tag{37}$$

IV. Synthesis of Optimal-Range Segmented DEM Encoders

Here, we describe how Theorem 2 and Corollary 2 can be applied to synthesize and analyze segmented DEM DACs with maximum linear range. For specificity, this is done in the context of two 14-b DACs for which experimental results have been presented in [36] and [37]. These cases are used to illustrate the synthesis technique as well as the fundamental complexity versus range restriction tradeoff implied by Theorem 1.

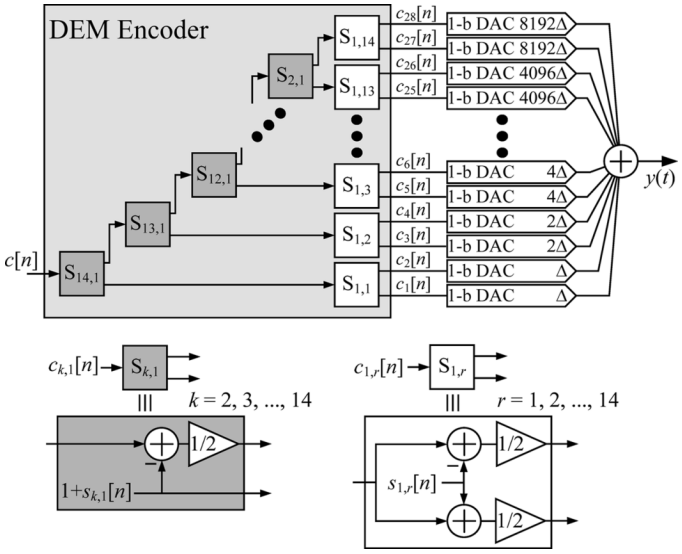

Fig. 2. A 14-b fully segmented DEM DAC.

A. Fully Segmented 14-b DEM DAC

The DEM DAC shown in Fig. 2 consists of 28 1-b DACs with weights given by

$$K_{2j-1} = K_{2j} = 2^{j-1}, \qquad \text{for } j = 1, 2, \ldots, 14. \tag{38}$$

Thus, the first two 1-b DACs each have a weight of unity, the next two each have a weight of 2, the next two each have a weight of 4, and so on, up to the last two which each have a weight of 8192.

The DEM encoder consists of a tree of 27 digital *switching blocks*, labeled $S_{1,r}$ for $r = 1, \ldots, 14$ and $S_{k,1}$ for $k = 2, \ldots, 14$. Each switching block generates two output sequences that depend on its input sequence and one of 14 pseudorandom bit sequences, $d_k[n]$. The pseudorandom sequences, $d_1[n], d_2[n], \ldots, d_{14}[n]$, are designed to well approximate white random processes that are independent of each other and $x[n]$ and take on values of 0 and 1 with equal probability.

There are two types of switching blocks. Switching blocks $S_{k,1}$ for $k = 2, 3, \ldots, 14$ are called *segmenting switching blocks* and switching blocks $S_{1,r}$ for $r = 1, 2, \ldots, 14$ are called *nonsegmenting switching blocks*. The top and bottom outputs of the segmenting switching blocks $S_{k,1}$ are

$$\frac{1}{2}\left(c_{k,1}[n] - 1 - s_{k,1}[n]\right) \quad \text{and} \quad 1 + s_{k,1}[n] \tag{39}$$

respectively, where $c_{k,1}[n]$ is the switching block input sequence and

$$s_{k,1}[n] = \begin{cases} 0, & \text{if } c_{k,1}[n] = \text{odd} \\ 1, & \text{if } c_{k,1}[n] = \text{even}, d_k[n] = 1 \\ -1, & \text{if } c_{k,1}[n] = \text{even}, d_k[n] = 0. \end{cases} \tag{40}$$

Similarly, the top and bottom outputs of the nonsegmenting switching blocks $S_{k,r}$ are

$$\frac{1}{2}\left(c_{k,r}[n] - s_{k,r}[n]\right) \quad \text{and} \quad \frac{1}{2}\left(c_{k,r}[n] + s_{k,r}[n]\right) \tag{41}$$

respectively, where $c_{k,r}[n]$ is the switching block input sequence and

$$s_{k,r}[n] = \begin{cases} 0, & \text{if } c_{k,r}[n] = \text{even} \\ 1, & \text{if } c_{k,r}[n] = \text{odd}, d_k[n] = 1 \\ -1 & \text{if } c_{k,r}[n] = \text{odd}, d_k[n] = 0. \end{cases} \tag{42}$$

For the DEM DAC shown in Fig. 2, $k = 1$ for each nonsegmenting switching block.

As described previously, the ith 1-b DAC is $\text{DAC}^{(i,i)}$, and, since $e_{DAC}^{(i,i)}(t) = 0$, it follows that $\text{DAC}^{(i,i)}$ has maximum linear range. Fig. 2 indicates that the input sequences to $\text{DAC}^{(1,1)}$ and $\text{DAC}^{(2,2)}$ are the top and bottom outputs, respectively, of the $S_{1,1}$ switching block. It follows from (17) and (41) that $c^{(1,2)}[n] = c_{1,1}[n]$. Therefore, $\text{DAC}^{(1,2)}$ consists of switching block $S_{1,1}$ followed by $\text{DAC}^{(1,1)}$ and $\text{DAC}^{(2,2)}$. Comparison of the left and right expressions in (41) with (29) and (30), respectively, indicates that the $S_{1,1}$ switching block implements (29) and (30) with $K = 1$, $G = 1/2$, $b = 0$, and $s[n] = s_{1,1}[n]/2$. This satisfies the hypothesis of Theorem 2, so $\text{DAC}^{(1,2)}$ has maximum linear range. By the same reasoning, for each $j = 4, 6, 8, \ldots, 28$, $\text{DAC}^{(j-1,j)}$ consists of the $S_{1,j/2}$ switching block followed by $\text{DAC}^{(j-1,j-1)}$ and $\text{DAC}^{(j,j)}$ and has maximum linear range. Furthermore, Corollary 2 with (23) and (38) implies that, for $j = 2, 4, 6, \ldots, 28$, we have

$$\alpha^{(j-1,j)}(t) = \frac{K_j}{2}\left[\alpha_{j-1}(t) + \alpha_j(t)\right] \tag{43}$$

and, during the nth sample period, we have

$$e_{DAC}^{(j-1,j)}(t) = \frac{K_j}{2} s_{1,j/2}[n]\left[\alpha_{j-1}(t - nT) - \alpha_j(t - nT)\right]\Delta. \tag{44}$$

Hence, the input sequences to $\text{DAC}^{(25,26)}$ and $\text{DAC}^{(27,28)}$ are the top and bottom outputs, respectively, of the $S_{2,1}$ switching block. It follows from (17) and (39) that $c^{(25,28)}[n] = c_{2,1}[n]$. Therefore, $\text{DAC}^{(25,28)}$ consists of switching block $S_{2,1}$ followed by $\text{DAC}^{(25,26)}$ and $\text{DAC}^{(27,28)}$. Comparison of the left and right expressions in (39) with (29) and (30), respectively, indicates that the $S_{2,1}$ switching block implements (29) and (30) with $K = 2$, $G = 1$, $b = 1$, and $s[n] = s_{2,1}[n]$. This satisfies the hypothesis of Theorem 2, so $\text{DAC}^{(25,28)}$ has maximum linear range.

By successively applying this reasoning for $k = 3, 4, \ldots, 14$, it follows that $\text{DAC}^{(29-2k,28)}$ consists of the $S_{k,1}$ switching block followed by $\text{DAC}^{(29-2k,30-2k)}$ and $\text{DAC}^{(31-2k,28)}$ and has maximum linear range. In particular, for $k = 14$, this proves that $\text{DAC}^{(1,28)}$, which is the DEM DAC of Fig. 2, has maximum linear range. Since $K_N = 8192$ and $M = 32766$, This implies that, if

$$c[n] \in \{8191, 8192, \ldots, 24575\} \tag{45}$$

for all n, then the DAC noise satisfies (15). Thus, $c_{\max} - c_{\min} = 16384$.

Recursively applying Corollary 2 with (38) and (43) gives

$$\alpha^{(29-2k,28)}(t) = \frac{K_{29-2k}}{2}\left[\alpha_{27}(t) + \alpha_{28}(t)\right] \tag{46}$$

for $k = 1, 2, \ldots, 14$. Hence, for the DEM DAC of Fig. 2, we have

$$\alpha(t) = \frac{1}{2}\left[\alpha_{27}(t) + \alpha_{28}(t)\right]. \tag{47}$$

Corollary 2 with (38), (43), (44), and (46) further implies that during the nth sample period

$$\begin{aligned} e_{\mathrm{DAC}}^{(29-2k,28)}(t) = {} & s_{k,1}[n]K_{30-2k}B_k\frac{\Delta}{2} + s_{1,15-k}[n]K_{30-2k} \\ & \times \left[\alpha_{29-2k}(t-nT) - \alpha_{30-2k}(t-nT)\right]\frac{\Delta}{2} \\ & + e_{\mathrm{DAC}}^{(31-2k,28)}(t) \end{aligned} \tag{48}$$

where

$$\begin{aligned} B_k = {} & \alpha_{29-2k}(t-nT) + \alpha_{30-2k}(t-nT) \\ & -\alpha_{27}(t-nT) - \alpha_{28}(t-nT) \end{aligned}$$

for $k = 2, 3, \ldots, 14$. Recursively applying (48) for $k = 2, 3, \ldots, 14$, gives

$$\begin{aligned} e_{\mathrm{DAC}}(t) = {} & \sum_{k=2}^{14} s_{k,1}[n]K_{30-2k}B_k\frac{\Delta}{2} \\ & + \sum_{r=1}^{14} s_{1,r}[n]K_{2r}\left[\alpha_{2r-1}(t-nT) - \alpha_{2r}(t-nT)\right]\frac{\Delta}{2} \end{aligned} \tag{49}$$

during the nth sample period.

With the top equation in (9), (47) and (49) give the unit pulse shape and DAC noise of the DEM DAC of Fig. 2 in terms of the mismatch error pulses. Given that the $s_{k,r}[n]$ sequences are white, have zero mean, and are uncorrelated with each other and with $c[n]$, it follows from (49) that the DAC noise satisfies (15) as expected, and, if the DAC noise is sampled at a rate of $f_s = 1/T$, the result is discrete-time white noise.

Theorem 2 is used above to verify that the DEM DAC of Fig. 2 has maximum linear range. However, the verification procedure is actually a synthesis procedure in that it successively combines the 1-b DACs two at a time to create increasingly large DEM DACs with maximum linear range. Furthermore, as demonstrated next, variations of the procedure yield maximum linear range DEM DACs with different topologies and tradeoffs.

B. Highly Segmented 14-b DEM DAC

The fully-segmented DEM DAC presented above is so named because it achieves maximum linear range with the minimum number of 1-b DACs. Therefore, in terms of the amount of digital logic (which is roughly proportional to the number of switching blocks), wire routing, and control circuitry for the 1-b DACs, the fully segmented DEM DAC is maximally hardware-efficient. However, a price is paid for this efficiency: the range of input values that can be represented by the set of 1-b DACs is {0, 1, . . ., 32766}, but, as implied by (45), $c[n]$ must be restricted to half of this range for the DAC to avoid introducing nonlinear distortion and spurious tones as a result of the mismatch error pulses. As described in the Introduction, the more the range has to be restricted, the higher the power dissipation for a given SNR.

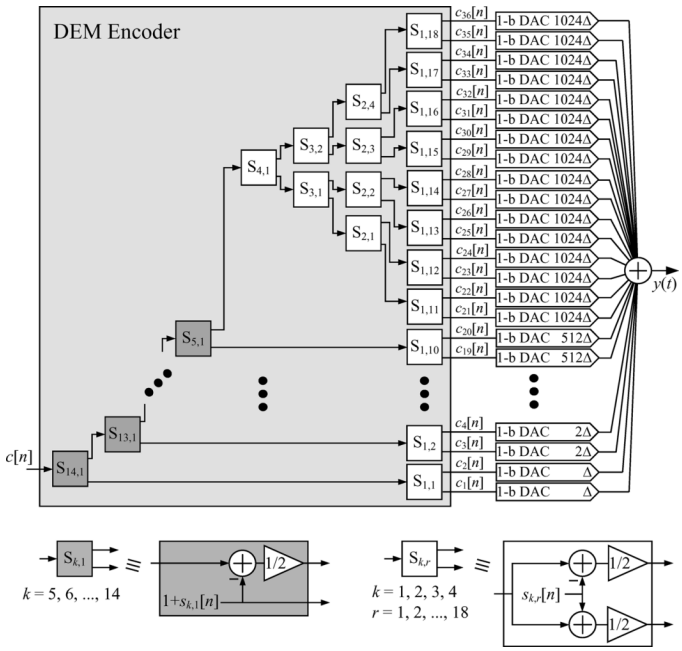

Fig. 3. A 14-b highly segmented DEM DAC.

A DEM DAC that represents a more balanced tradeoff between hardware complexity and power dissipation is shown in Fig. 3. Its DEM encoder contains 10 segmenting switching blocks, i.e., $S_{k,1}$ for $k = 5, 6, \ldots, 14$, and 25 nonsegmenting switching blocks, i.e., $S_{k,r}$ for $k = 1, 2, \ldots, 4$ and $r = 1, 2, \ldots, 18$, with the functionality described by (39) and (41), respectively. The weights of its 1-b DACs are

$$\begin{aligned} K_{2j-1} = K_{2j} = 2^{j-1}, \qquad & \text{for } j = 1, 2, \ldots, 10 \\ K_j = 1024, \qquad & \text{for } j = 21, \ldots, 36. \end{aligned} \tag{50}$$

Thus, the first two 1-b DACs each have a weight of unity, the next two each have a weight of 2, the next two each have a weight of 4, and so on, up to the 20th 1-b DAC which has a weight of 512. The 21st–36th 1-b DACs each have a weight of 1024.

By applying Theorem 2 in the same successive fashion as described above for the fully segmented DEM DAC, it can be verified that the DEM DAC of Fig. 3 has maximum linear range. Since $K_N = 1024$ and $M = 18430$, This implies that if

$$c[n] \in \{1023, 1024, \ldots, 17407\} \tag{51}$$

for all n, then the DAC noise satisfies (15). Thus, $c_{\max} - c_{\min} = 16384$, exactly as in the case of the fully segmented DEM DAC.

By recursively applying Corollary 2 as described above for the case of the fully segmented DEM DAC, it can be verified that

$$\alpha(t) = \frac{1}{16}\sum_{i=21}^{36}\alpha_i(t) \tag{52}$$

TABLE I
SEGMENTATION TRADEOFF OPTIONS FOR 14-b DEM DACS WITH MAXIMUM LINEAR RANGE

Number of Segmenting Switching Blocks	Number of Non-Segmenting Switching Blocks	M	Segmenting Switching Blocks: $S_{k,1}$	1-bit DAC Weights: $K_i = \begin{cases} K_{max}, & \text{if } P < i \le N, \\ 2^{\lceil (i-1)/2 \rceil}, & \text{if } 1 \le i \le P. \end{cases}$		
				K_{max}	P	N
0 (unity-weighted)	16383	16384	N/A	1	1	16384
1	8192	16386	$k = 14$	2	2	8194
2	4097	16390	$k = 13, 14$	4	4	4100
3	2050	16398	$k = 12, 13, 14$	8	6	2054
4	1027	16414	$k = 11, 12, 13, 14$	16	8	1032
5	516	16446	$k = 10, 11, \ldots, 14$	32	10	522
6	261	16510	$k = 9, 10, \ldots, 14$	64	12	258
7	134	16638	$k = 8, 9, \ldots, 14$	128	14	142
8	71	16894	$k = 7, 8, \ldots, 14$	256	16	80
9	40	17406	$k = 6, 7, \ldots, 14$	512	18	50
10 (Figure 3)	25	18430	$k = 5, 6, \ldots, 14$	1024	20	36
11	18	20478	$k = 4, 5, \ldots, 14$	2048	22	30
12	15	24574	$k = 3, 4, \ldots, 14$	4096	24	28
13 (Figure 2)	14	32766	$k = 2, 3, \ldots, 14$	8192	26	28

and during the nth sample period

$$e_{\mathrm{DAC}}(t) = \sum_{k=5}^{14} s_{k,1}[n] K_{30-2k} F_k \frac{\Delta}{2} + \sum_{k=2}^{4} \sum_{r=1}^{2^{4-k}} D_{k,r} + \sum_{r=1}^{18} s_{1,r}[n] K_{2r} \left[\alpha_{2r-1}(t-nT) - \alpha_{2r}(t-nT)\right] \frac{\Delta}{2} \tag{53}$$

where

$$D_{k,r}(t) = \frac{1}{2^k} \sum_{i=(r-1)2^k+1}^{(r-1)2^k+2^{k-1}} \left(\alpha_{20+i}(t-nT) - \alpha_{20+i+2^{k-1}}(t-nT)\right) K_{21}\Delta$$

$$F_k = \alpha_{29-2k}(t-nT) + \alpha_{30-2k}(t-nT) - \frac{1}{8}\sum_{i=21}^{36} \alpha_i(t-nT).$$

The range given by (51) represents a reduction of approximately 11% relative to the full range of input values that could otherwise be represented by the set of 36 1-b DACs in the DEM DAC of Fig. 3. In contrast, the corresponding input range reduction for the fully-segmented DEM DAC is 50%. As is evident from a comparison of Figs. 2 and 3, the smaller input range restriction for the DEM DAC of Fig. 3 comes at the expense of a modest increase in the numbers of 1-b DACs and switching blocks.

Other tradeoff points between input range reduction and complexity can be used. Table I enumerates the possibilities for maximum linear range DEM DACs with $c_{\max} - c_{\min} = 16\,384$. Similar results hold for different choices of $c_{\max} - c_{\min}$. The appropriate level of segmentation depends on the circuit technology, and the relative importance of minimizing complexity versus minimizing analog power dissipation for the given application.

V. CONCLUSION

This paper quantifies the fundamental complexity versus input range restriction tradeoff associated with segmentation in DEM DACs. In present-day CMOS circuit technology, the tradeoff translates into one of circuit area versus power dissipation. The analysis is general in that it applies to any DEM DAC of the form shown in Fig. 1 and is independent of the algorithm employed by the DEM encoder. The paper also presents a synthesis technique with which to design segmented DEM DAC encoders of any desired resolution and any desired level of segmentation. Together, the results presented in the paper can be used to design segmented DEM DACs that are optimized for their given applications in terms of the circuit area versus power dissipation tradeoff.

APPENDIX

The proofs of the Theorems and Corollaries are presented in this appendix. Additionally, two Lemmas are presented that support the proofs.

Lemma 1: Let u, v, and w be any integers such that $\mathrm{DAC}^{(u,v)}$ and $\mathrm{DAC}^{(v+1,w)}$ are defined. Then, for any constants G and b, there exists a sequence $s[n]$ such that the inputs to $\mathrm{DAC}^{(u,v)}$ and $\mathrm{DAC}^{(v+1,w)}$ are given by

$$c^{(u,v)}[n] = (1-G)c^{(u,w)}[n] + b + s[n] \tag{54}$$

and

$$c^{(v+1,w)}[n] = \frac{1}{K}\left(Gc^{(u,w)}[n] - b - s[n]\right) \tag{55}$$

respectively, where $K = K_{v+1}/K_u$ and $c^{(u,w)}[n]$ is the input to $\mathrm{DAC}^{(u,w)}$. Furthermore

$$\alpha^{(u,w)}(t) = (1-G)\alpha^{(u,v)}(t) + \frac{1}{K}G\alpha^{(v+1,w)}(t) \tag{56}$$

and during the nth sample period

$$e_{\mathrm{DAC}}^{(u,w)}(t) = s[n]\left[\alpha^{(u,v)}(t-nT) - \frac{1}{K}\alpha^{(v+1,w)}(t-nT)\right]\Delta + e_{\mathrm{DAC}}^{(u,v)}(t) + e_{DAC}^{(v+1,w)}(t). \tag{57}$$

Proof: It follows from (17) that

$$c^{(u,w)}[n] = c^{(u,v)}[n] + Kc^{(v+1,w)}[n]. \tag{58}$$

Let G and b be any pair of constants. For each n and any given values of $c^{(u,v)}[n]$ and $c^{(u,w)}[n]$, a value for $s[n]$ can be chosen such that (54) holds (the value can be found by solving (54) for $s[n]$). Substituting (54) into (58) and solving for $c^{(v+1,w)}[n]$ yields (55).

It follows from (18) that

$$y^{(u,w)}(t) = y^{(u,v)}(t) + y^{(v+1,w)}(t). \tag{59}$$

Substituting $y^{(u,v)}(t)$ and $y^{(v+1,w)}(t)$ in the form of (21) with (54) and (55) into (59) and collecting terms yields (21) with (56) and (57). □

Lemma 2: If the hypothesis of Lemma 1 is satisfied, then the DAC noise from $\mathrm{DAC}^{(u,w)}$ satisfies (22) regardless of the mismatch error pulses only if

$$\begin{aligned}\mathrm{E}\{s[n]\} &= 0\\ \mathrm{E}\left\{s[n]c^{(u,w)}[n]\right\} &= 0\end{aligned} \tag{60}$$

for all n.

Proof: It is sufficient to show that, for at least one set of mismatch error pulses, if (60) is not satisfied, then (22) is not satisfied.

Suppose

$$e_{hi}(t) = -e_{li}(t) = \begin{cases} 0, & \text{if } u \le i \le v \\ -\frac{1}{2}\varepsilon(t)K_i\Delta, & \text{if } v+1 \le i \le w \end{cases} \tag{61}$$

where $\varepsilon(t)$ is any nonzero function that is zero outside of $0 \le t < T$. In this case, (8) and (9) imply that the output of the ith 1-b DAC during the nth sample period is

$$y_i(t) = \begin{cases} \left(c_i[n] - \frac{1}{2}\right)a(t-nT)K_i\Delta, & \text{if } u \le i \le v \\ \left(c_i[n] - \frac{1}{2}\right)a_\varepsilon(t-nT)K_i\Delta, & \text{if } v+1 \le i \le w \end{cases} \tag{62}$$

where $a_\varepsilon(t) = a(t) - \varepsilon(t)$. It follows from (17), (18), and (20) that the output of $\mathrm{DAC}^{(u,w)}$ during the nth sample period is

$$y^{(u,w)}(t) = K_u\left(c^{(u,v)}[n] - \frac{1}{2}M^{(u,v)}\right)a(t-nT)\Delta + K_{v+1}\left(c^{(v+1,w)}[n] - \frac{1}{2}M^{(v+1,w)}\right)a_\varepsilon(t-nT)\Delta. \tag{63}$$

Substituting (54) and (55) into (63) and grouping terms as in (21) yields

$$e_{\mathrm{DAC}}^{(u,w)}(t) = s[n]K_u\varepsilon(t-nT)\Delta \tag{64}$$

during the nth sample period. Hence, for the set of mismatch error pulses given by (61), $e_{\mathrm{DAC}}^{(u,w)}(t)$ is proportional to $s[n]$ so if (60) is not satisfied then (22) is not satisfied. □

Proof of Theorem 1: Let p be the smallest integer for which $K_{p+1} = K_N$. Given that $K_i \ge K_{i-1}$, this implies that $K_i = K_N$ for $i = p+1, p+2, \ldots, N$. It follows from (16) and (17) that

$$c[n] = c^{(1,p)}[n] + K_N c^{(p+1,N)}[n]. \tag{65}$$

By definition

$$c[n] \in \{0, 1, \ldots, M\} \tag{66}$$

$$c^{(1,p)}[n] \in \left\{0, 1, \ldots, M^{(1,p)}\right\} \tag{67}$$

and

$$c^{(p+1,N)}[n] \in \left\{0, 1, \ldots, M^{(p+1,N)}\right\} \tag{68}$$

where

$$\begin{aligned}M^{(1,p)} &= \sum_{i=1}^{p} K_i\\ M^{(p+1,N)} &= N - p.\end{aligned} \tag{69}$$

It follows from (6) that

$$M = M^{(1,p)} + K_N M^{(p+1,N)}. \tag{70}$$

Let G and b be any pair of constants. Lemmas 1 and 2 with $u = 1$, $v = p$, and $w = N$ imply that

$$c^{(1,p)}[n] = (1-G)c[n] + b + s[n] \tag{71}$$

$$c^{(p+1,N)}[n] = \frac{1}{K_N}\left(Gc[n] - b - s[n]\right) \tag{72}$$

and $e_{DAC}(t)$ satisfies (15) only if the expected value of $s[n]$ is zero and $s[n]$ is uncorrelated to $c[n]$. This is possible for a given value of $c[n]$ only if either $s[n]$ can be set to zero or there exist at least two nonzero values to which it can be set, one positive and one negative, such that (71) and (72) yield values of $c^{(1,p)}[n]$ and $c^{(p+1,N)}[n]$ that satisfy (67) and (68), respectively.

If $c[n]$ takes on any value in the set

$$\{0, 1, \ldots, K_N - 1\} \tag{73}$$

then $c^{(p+1,N)}[n] = 0$ must hold to satisfy (65), (67), and (68), in which case only one value of $s[n]$ satisfies (72). Similarly, if $c[n]$ takes on any value in the set

$$\{M - K_N + 1, M - K_N + 2, \ldots, M\} \tag{74}$$

then $c^{(p+1,N)}[n] = M^{(p+1,N)}$ must hold to satisfy (65), (67), and (68), in which case only one value of $s[n]$ satisfies (72). In this sense, each value in (73) or (74) has a single corresponding value of $s[n]$. If $c[n]$ takes on any of the values in (73) or (74) for

which the corresponding value of $s[n]$ is nonzero, then $e_{DAC}(t)$ will not satisfy (15).

It follows from (72) that if $G \neq 0$, then $s[n] = 0$ for at most one value of $c[n]$ in (73) and at most one value of $c[n]$ in (74). Therefore, if $s[n] = 0$ when $c[n] = K_N - 1$, then $s[n] \neq 0$ when $c[n] = K_N - 2$. Similarly, if $s[n] = 0$ when $c[n] = M - K_N + 1$, then $s[n] \neq 0$ when $c[n] = M - K_N + 2$. This implies that the contiguous range of input values for which (15) is satisfied can be no larger than implied by (25).

If $G = 0$, then (67), (71), and the requirement that $s[n]$ have zero mean and be uncorrelated to $c[n]$ for the DAC noise to satisfy (15) imply that $c_{\max} - c_{\min}$ can be no larger than $M^{(1,p)} = M - K_N M^{(p+1,N)}$. Therefore, the contiguous range of input values for which (15) is satisfied can be no larger than implied by (25) if $M^{(p+1,N)} \geq 2$, which occurs if $K_{N-1} = K_N$.

Now, suppose that $K_{N-1} \neq K_N$. Then $p = N - 1$, so $c^{(p+1,N)}[n] \in \{0, 1\}$ for all n. Let $c_{\max}^{(1,p)}$ and $c_{min}^{(1,p)}$ be the largest and smallest integers, respectively, for which

$$c^{(1,p)}[n] \in \left\{ c_{\min}^{(1,p)}, c_{\min}^{(1,p)} + 1, c_{\min}^{(1,p)} + 2, \ldots, c_{\max}^{(1,p)} \right\} \quad (75)$$

for all n ensures that $e_{\mathrm{DAC}}^{(1,p)}[n]$ satisfies (22). Since $c^{(p+1,N)}[n] \geq 0$, $c[n] \geq c_{min}^{(1,p)}$ for all n is a necessary condition for $e_{\mathrm{DAC}}^{(1,p)}[n]$ to satisfy (22), and, consequently, for $e_{\mathrm{DAC}}(t)$ to satisfy (15). Furthermore, whenever $c[n]$ takes on any value in the set

$$\left\{ c_{\min}^{(1,p)}, c_{\min}^{(1,p)} + 1, \ldots, c_{\min}^{(1,p)} + K_N - 1 \right\} \quad (76)$$

then $c^{(p+1,N)}[n] = 0$ must hold to satisfy (65) and (75), in which case only one value of $s[n]$ satisfies (72). Similarly, for $e_{DAC}^{(1,p)}[n]$ to satisfy (22), and, consequently, for $e_{DAC}(t)$ to satisfy (15), if $c[n]$ takes on any value in the set

$$\left\{ c_{\max}^{(1,p)} + 1, c_{\max}^{(1,p)} + 2, \ldots, c_{\max}^{(1,p)} + K_N \right\} \quad (77)$$

then $c^{(p+1,N)}[n] = 1$ must hold to satisfy (65) and (75), in which case only one value of $s[n]$ satisfies (72).

By the same reasoning described above but with (76) and (77) playing the roles of (73) and (74), respectively, it follows that $c_{\max} - c_{\min} \leq c_{\max}^{(1,p)} - c_{\min}^{(1,p)}$. Consequently, the original DEM DAC can be replaced by $\mathrm{DAC}^{(1,p)}$ with $c^{(1,p)}[n] = c[n]$ without reducing the contiguous range of input values for which (15) is satisfied. □

Proof of Corollary 1: The proof is nearly identical to that of Theorem 1. □

Proof of Theorem 2: Substituting (33) into (29) shows that $c^{(v+1,w)}[n]$ is integer-valued for any $c^{(u,w)}[n]$ in (19). Furthermore, substituting (31)–(33) into (29) with

$$K_w/K_u - 1 \leq c^{(u,w)}[n] \leq M^{(u,w)} - K_w/K_u + 1 \quad (78)$$

gives

$$K_w/K_{v+1} - 1 \leq c^{(v+1,w)}[n] \leq M^{(v+1,w)} - K_w/K_{v+1} + 1. \quad (79)$$

Therefore, if

$$c_{\min}^{(u,w)} \leq c^{(u,w)}[n] \leq c_{\max}^{(u,w)} \quad (80)$$

then

$$c_{\min}^{(v+1,w)} \leq c^{(v+1,w)}[n] \leq c_{\max}^{(v+1,w)}. \quad (81)$$

Consequently, $e_{\mathrm{DAC}}^{(v+1,w)}(t)$ satisfies (22) because $\mathrm{DAC}^{(v+1,w)}$ has maximum linear range. Furthermore, Lemma 1 implies that $c^{(u,v)}[n]$ is given by (54) and, hence, (30). All of the 1-b DACs associated with $\mathrm{DAC}^{(u,v)}$ have the same weight, so $c_{\min}^{(u,v)} = 0$ and $c_{\max}^{(u,v)} = M^{(u,v)}$. Since $\mathrm{DAC}^{(u,v)}$ has maximum linear range, this implies that $e_{\mathrm{DAC}}^{(u,v)}(t)$ satisfies (22).

Lemma 1 further implies that $e_{\mathrm{DAC}}^{(u,w)}(t)$ is given by (57). Since $e_{\mathrm{DAC}}^{(v+1,w)}(t)$ and $e_{\mathrm{DAC}}^{(u,v)}(t)$ both satisfy (22) and are uncorrelated with each other, the hypothesized properties of $s[n]$ are sufficient for $e_{\mathrm{DAC}}^{(u,w)}(t)$ to satisfy (22). □

Proof of Corollary 2: The corollary follows directly from Lemma 1 and Theorem 2. □

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