Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional-*N* PLL

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***Abstract*—This paper demonstrates that spurious tones in the output of a fractional-*N* PLL can be reduced by replacing the $\Delta\Sigma$ modulator with a new type of digital quantizer and adding a charge pump offset combined with a sampled loop filter. It describes the underlying mechanisms of the spurious tones, proposes techniques that mitigate the effects of the mechanisms, and presents a phase noise cancelling 2.4 GHz ISM-band CMOS PLL that demonstrates the techniques. The PLL has a 975 kHz loop bandwidth and a 12 MHz reference. Its phase noise has a worst-case reference spur power of −70 dBc and a worst-case in-band fractional spur power of −64 dBc.**

***Index Terms*—Fractional-*N* phase-locked loop, PLL, frequency synthesis.**

I. Introduction

MOST wireless communication systems require local oscillators for up-conversion and down-conversion of their transmitted and received signals. Usually, the spectral purity of the local oscillator is a critical factor in overall transceiver performance, so communication standards explicitly or implicitly stipulate stringent spectral purity requirements on the local oscillators [1], [2]. In addition to dictating the maximum acceptable phase noise power in various frequency bands, most standards require that spurious tones in the local oscillator's output be highly attenuated, particularly in critical frequency bands.

Local oscillators in such applications are often implemented as fractional-N phase-locked loops (PLLs). Unfortunately, spurious tones are inevitable in the output signals of fractional-N PLLs, and in conventional designs they can be attenuated only with design tradeoffs that degrade other aspects of performance. Generally, spurious tone power can be reduced by increasing the linearity of key circuit blocks such as the charge pump and divider, restricting the choice of reference frequencies, and reducing the loop bandwidth. Unfortunately, increasing linearity tends to increase power consumption and circuit area, restricting the choice of reference frequencies reduces design flexibility, and reducing the loop bandwidth increases in-band phase noise, settling time, susceptibility to oscillator pulling, and loop filter size [1]. Furthermore, these methods of spurious tone reduction become less effective as CMOS circuit technology is scaled into the sub-100 nanometer regime. Therefore, the spurious tone problem negatively affects power consumption, cost, and manufacturability of wireless transceivers, and the problem gets worse as CMOS circuit technology scales with Moore's Law.

This paper presents a 2.4 GHz ISM band fractional-N PLL that achieves state-of-the-art spurious tone suppression enabled by techniques that avoid the tradeoffs mentioned above [3]. One of the techniques is the use of a new type of digital quantizer, called a *successive requantizer*, in place of the digital delta-sigma $(\Delta\Sigma)$ modulator used in conventional fractional-N PLLs [4]. The other technique involves the combination of a charge pump offset and a sampled loop filter.

The paper consists of four main sections. Section II describes the mechanisms by which the two types of spurious tones, reference spurs and fractional spurs, arise in fractional-N PLLs. Section III describes the successive requantizer. Section IV describes the charge pump offset and sampled loop filter. Section V presents additional circuit details and measurement results.

II. Spurious Tones and Their Causes in Fractional-N PLLs

A. Fractional-N PLL Overview

The purpose of a fractional-N PLL is to generate a periodic output signal with frequency $f_{\rm out} = (N + \alpha)f_{\rm ref}$, where N is an integer, α is a fractional value between 0 and 1, and $f_{\rm ref}$ is the frequency of a reference oscillator (e.g., the crystal frequency). As shown in Fig. 1, a typical fractional-N PLL consists of a phase-frequency detector (PFD), a charge pump, a loop filter, a voltage controlled oscillator (VCO), a frequency divider, and a digital $\Delta\Sigma$ modulator clocked by the divider output [5]–[7]. The divider output is a two-level signal in which the nth and $(n+1)$th rising edges are separated by $N + y[n]$ periods of the VCO output, where $y[n]$ is an integer-valued sequence from the $\Delta\Sigma$ modulator. As indicated in the figure for the case where the PLL is locked, if the nth rising edge of the reference signal, $v_{\rm ref}(t)$, occurs before that of divider output, $v_{div}(t)$, the charge pump generates a current pulse of nominal amplitude I and a duration equal to the time difference between the two edges. Otherwise, the situation is similar except the polarity of the current pulse is reversed. The PLL's feedback adjusts the output frequency so as to zero the DC component of the charge pump output. This

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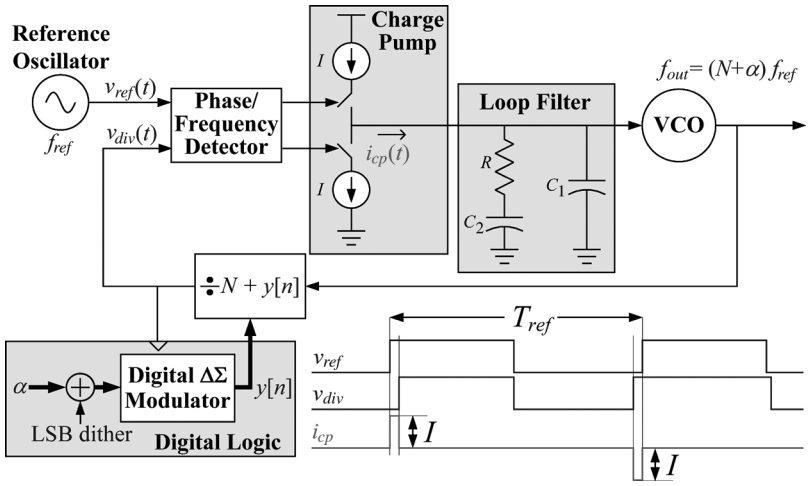


Fig. 1. Block diagram of a typical fractional-N PLL.

causes the output frequency to settle to $f_{\rm ref}$ times the sum of N and the average of $y[n]$.

If $y[n]$ could be set to α directly, then the output frequency of the PLL would settle to $(N+\alpha)f_{\rm ref}$, thereby achieving the goal of the fractional-N PLL. Unfortunately, this is not possible. The divider can only count integer VCO cycles so $y[n]$ is restricted to integer values whereas α is a fractional value. To circumvent this problem $y[n]$ is designed to be a sequence of integers that *average* to α. The input to the $\Delta\Sigma$ modulator is α plus pseudo-random least significant bit (LSB) dither, so its output has the form $y[n] = \alpha + s[n]$, where $s[n]$ is a zero-mean sequence consisting of spectrally shaped $\Delta\Sigma$ quantization noise and LSB dither. As proven in [8], the dither prevents $s[n]$ from containing spurious tones that would otherwise show up as spurious tones in the PLL's output. Hence, the output frequency settles to an average $(N+\alpha)f_{\rm ref}$, as desired, although $s[n]$ introduces phase noise.

The $s[n]$ sequence causes an amount of charge equal to $T_{VCO}\cdot I\cdot t[n]$ to be added to the nth charge pump pulse, where T_{VCO} is the period of the VCO output (for a given value of α, T_{VCO} is well-modeled as a constant) and

$$t[n] = \sum_{k=0}^{n} s[k] \tag{1}$$

is the *running sum* of $s[n]$. Hence, the PLL's phase noise contains a lowpass filtered version of $t[n]$. The bandwidth of the lowpass filtering operation is called the *loop bandwidth* of the PLL. Usually, the quantization noise transfer function of the $\Delta\Sigma$ modulator is highpass shaped with at least one zero at DC. Therefore, $t[n]$ is bounded and shaped with an order of one less than that of the $\Delta\Sigma$ modulator's quantization noise transfer function. Provided the loop bandwidth is sufficiently low, the resulting phase noise is suppressed below that from other noise sources in the PLL. Alternatively, a DAC can be used to cancel $t[n]$ prior to the loop filter, thereby minimizing its contribution to the PLL's phase noise so that a much larger loop bandwidth can be used [9]–[13]. Such fractional-N PLL's are called *phase noise cancelling* fractional-N PLLs.

B. Reference Spurs

Reference spurs are spurious tones in the PLL's output that occur at multiples of $f_{\rm ref}$ from $f_{\rm out}$. They result mainly from periodic disturbances of the loop filter voltage introduced by the charge pump. Therefore, the loop bandwidth and the reference frequency both affect the power of the reference spurs. Widening the loop bandwidth for a given reference frequency or decreasing the reference frequency for a given loop bandwidth both have the effect of reducing the loop filter's attenuation of the disturbances, thereby increasing the power of the reference spurs.

Mismatches between the positive and negative current sources in the charge pump are the primary causes of the disturbances that cause reference spurs. A typical PFD turns on both current sources in the charge pump each reference period for a minimum duration, T_D, where T_D is large enough to ensure that both current sources fully settle before they are turned off. Each reference period the PFD turns on the positive current source when the reference edge occurs and the negative current source when the divider edge occurs, and turns them both off simultaneously T_D seconds after the later of the two edges. The difference between the positive and negative current pulses is the charge pump output current pulse. By ensuring that both current sources have time to settle, a major source of charge pump nonlinearity is avoided [14]. However, inevitable transient and amplitude mismatches between the two current sources give rise to an error component in each charge pump pulse that is constant from period to period. Although the PLL's feedback nulls out the DC component of the constant error pulse by adjusting the phase of the VCO, the result is a zero-mean periodic disturbance of the VCO's control voltage which causes a reference spur.

In theory, the disturbance and, therefore, the reference spur could be eliminated by performing an ideal sample-and-hold operation between the loop filter and the VCO once per reference period. The sampled loop filter presented in Section IV provides a practical means of achieving this result to a high degree of accuracy.

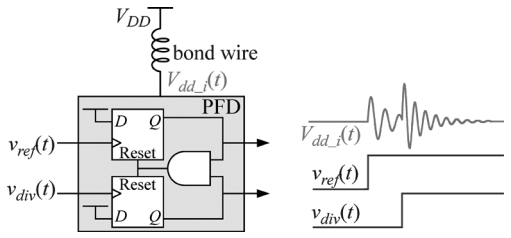


Fig. 2. Example of a nonlinear coupling path in the PFD.

C. Fractional Spurs

Fractional spurs are spurious tones in the PLL's output that occur at multiples of $\alpha f_{\rm ref}$ from $f_{\rm out}$.[1] Typically, the most significant fractional spurs are the result of disturbances on the loop filter voltage introduced through the charge pump. Therefore, the power of a fractional spur usually depends on both its frequency and the loop bandwidth. In conventional fractional-N PLLs, fractional spurs within the loop bandwidth tend to be large, typically well above -60 dBc, while fractional spurs at higher frequencies usually are attenuated by the loop filter. Hence, the power of the fractional spur at $\alpha f_{\rm ref}$ can be reduced by reducing the loop bandwidth for any given values of $f_{\rm ref}$ and α. In conventional fractional-N PLLs the application's spurious tone suppression requirements typically dictate restrictions on the choice of reference frequency and loop bandwidth so as to ensure that $\alpha f_{\rm ref}$ is sufficiently outside the loop bandwidth for every desired output frequency.

As described in the remainder of this section, fractional spurs arise from two distinct mechanisms. The techniques presented in Sections III and IV respectively address each mechanism to reduce the power of the fractional spurs.

Fractional Spur Mechanism 1: It is well known that nonlinear parasitic coupling between the VCO output signal and harmonics of the reference signal result in fractional spurs. For example, if the Nth harmonic of the reference signal intermodulates with the VCO output signal through a parasitic coupling path in the circuit, the intermodulation product is a spurious tone at $\alpha f_{\rm ref}$.

The potential for such coupling is greatest in the PFD and charge pump, as these blocks handle signals aligned with the reference signal as well as those aligned with the VCO output [10]. The hard-switching that occurs within these blocks induces disturbances on the local power supply lines because of the bond wire inductance. This modulates the switching threshold of the digital gates powered by these supplies. As illustrated in Fig. 2, the two flip-flops in the PFD capture the phase difference between the divider and reference edges. For small phase differences, the disturbance induced by the earlier edge does not have time to die out before the later edge arrives, so it can modulate the delay through the flip-flop of the later edge, thereby corrupting the phase difference measurement. The resulting error contains intermodulation products of the VCO output and reference signal which are injected into the loop filter and cause fractional spurs. Similar coupling effects occur within the charge pump circuitry.

[1]A fractional spur in the the PLL output at a frequency of $f_{\rm out} + f_{spur}$ is often said to *occur at frequency* f_{spur} because it appears at frequency f_{spur} in a phase noise plot. This terminology is used in the remainder of the paper.

Fractional Spur Mechanism 2: Surprisingly, the digital $\Delta\Sigma$ modulator in a fractional-N PLL is a fundamental source of spurious tones in the PLL's output [3], [4], [9], [15]. This is true even though dither is used to prevent spurious tones in the $\Delta\Sigma$ modulator's output. Regardless of how dither is applied, spurious tones are induced when the $\Delta\Sigma$ modulator's quantization noise is subjected to nonlinear distortion. This is particularly problematic in fractional-N PLLs wherein the output sequence from the $\Delta\Sigma$ modulator is converted to analog form and both $s[n]$ and its running sum, $t[n]$, are subjected to nonlinear operations because of non-ideal circuit behavior.

A digital $\Delta\Sigma$ modulator often used in fractional-N PLLs is shown in Fig. 3(a) as a demonstration vehicle. It is an all-digital structure consisting of two accumulators, a round-to-the-nearest-integer quantizer, and two negative feedback paths. It is well known that if the $\Delta\Sigma$ modulator input is kept between 0 and 1, then the output is restricted to the integers: $\{-1, 0, 1, 2\}$, and $s[n] = d[n-2]+e_q[n]-2e_q[n-1]+e_q[n-2]$, where $e_q[n]$ is additive error from the round-to-the-nearest-integer operation of the quantizer. Therefore, $e_q[n]$ is subjected to the equivalent of a three tap FIR filter with a pair of zero-frequency zeros.

As shown in [8], if the dither sequence, $d[n]$, is an equiprobable two-level, white, random sequence of any non-zero magnitude, then $e_q[n]$ is guaranteed to be asymptotically white and zero mean. In this case, $e_q[n]$, and, hence, $s[n]$, are guaranteed to be free of spurious tones. Moreover, the three tap FIR filtering causes the power spectral density (PSD) of the quantization noise component of $s[n]$ to increase at 12 dB per octave in frequency. For example, the simulated PSD of $s[n]$ is shown in the left plot in Fig. 3(b) for the case where $\alpha = 0.002$, $d[n]$ is a white pseudo-random sequence that takes on values of 0 and 2^{-17} with equal probability, and the sample rate is 20 MHz. In this case, the magnitude of the dither is sufficiently small that it is not visible in the PSD plot, yet its presence ensures that spurious tones are avoided in $s[n]$. However, as shown in the right plot of Fig. 3(b), spurious tones are clearly present in the PSD of $(s[n])^2$. Similar results occur for other types of nonlinear distortion and all other $\Delta\Sigma$ modulators and dither methods known to the authors. For example, the problem occurs even if the dither sequence is white with a triangular probability density function that extends from -1 to 1 and is added directly to the input of the quantizer.

If it seems counter-intuitive that spurious tones can occur when a spur-free sequence is subjected to nonlinear distortion, consider a random sequence given by

$$q[n] = \begin{cases} \pm 1(\text{chosen randomly}), & \text{if } n \text{ is even}, \\ 0, & \text{if } n \text{ is odd}. \end{cases} \tag{2}$$

It is easy to verify that $q[n]$ is white and, hence, free of spurious tones. However, $(q[n])^2$ is 1 for even values of n and 0 for odd values of n, so $(q[n])^2$ is nothing but a spurious tone at half the sample rate and a constant offset. In this simple case, $q[n]$ has "sufficient randomness" to avoid spurious tones in the absence of nonlinear distortion but not when subjected to even-order nonlinear distortion.

The situation is conceptually similar, but more complicated, for the case of a $\Delta\Sigma$ modulator. The interaction of the constant

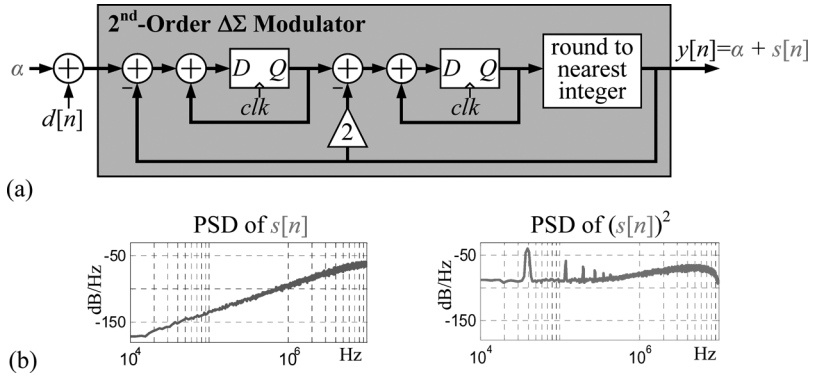


Fig. 3. (a) A second-order digital $\Delta\Sigma$ modulator, and (b) an example in which $s[n]$ is free of spurious tones but a nonlinearly distorted version of $s[n]$ contains spurious tones.

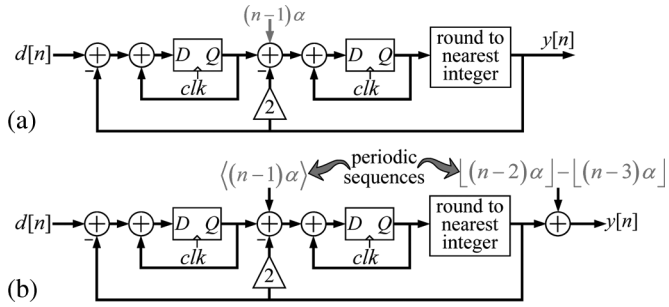


Fig. 4. Structures that are both equivalent to that of Fig. 3(a).

input and the first accumulator gives rise to "hidden periodicities" as indicated in Fig. 4. Both structures in Fig. 4 are equivalent to that of Fig. 3(a) in that they generate the same $y[n]$ sequence. The structure of Fig. 4(a) differs from that of Fig. 3(a) in that in Fig. 4(a) the α input has been replaced by its delayed running sum, $(n-1)\alpha$, added after the first accumulator. This sequence can be written as

$$(n-1)\alpha = \lfloor (n-1)\alpha \rfloor + \langle (n-1)\alpha \rangle \tag{3}$$

where $\lfloor x \rfloor$ denotes the largest integer less than or equal to x, and $\langle x \rangle$ denotes the fractional part of x. The round-to-the-nearest-integer quantizer has no effect on integer-valued components of its input, and the transfer function from the input of the second accumulator to the output of the $\Delta\Sigma$ modulator is $z^{-1}(1-z^{-1})$ so the integer-valued component of (3) can be moved after the feedback loops as shown in Fig. 4(b). The significance is that both additive sequences in Fig. 4(b) associated with α are periodic with a period that depends on α, so they are each made up entirely of spurious tones (i.e., their Fourier series components). The dither provides sufficient randomness to avoid spurious tones in $s[n]$ as proven in [8], but not to avoid spurious tones when $s[n]$ is subjected to nonlinear distortion as demonstrated in Fig. 3(b).

III. A Delta-Sigma Modulator Replacement

The fractional-N PLL presented in this paper uses a successive requantizer in place of a $\Delta\Sigma$ modulator to circumvent fractional spur mechanism 2 [4]. The successive requantizer performs coarse quantization with spectrally shaped quantization noise like a $\Delta\Sigma$ modulator, but its quantization noise is less susceptible to nonlinearity-induced spurious tones as described below.

A high-level view of the successive requantizer is shown in Fig. 5. It quantizes a 19-bit input sequence by 16 bits to generate a 3-bit output sequence [3], [4]. By design convention, the input and output of the successive requantizer are integer-valued. For the fractional-N PLL application, the goal is to quantize α, which is a fractional value between 0 and 1, and in this design α is taken to be a constant multiple of 2^{-16}. Therefore, α is scaled by 2^{16} prior to the successive requantizer to convert it into an integer. As explained below, the 3-bit integer-valued output of the successive requantizer is $y[n] = \alpha + s[n]$, where $s[n]$ is quantization noise.

As shown in Fig. 5(a) the successive requantizer consists of 16 *quantization blocks*, each of which simultaneously halves its input and quantizes the result by one bit every sample period. The general form of each quantization block is shown in Fig. 5(b) wherein all variables are integer-valued two's complement numbers. The output of the dth quantization block is $x_{d+1}[n] = (x_d[n] + \mathrm{s}_d[n])/2$, where $s_d[n]$ is a sequence generated within the quantization block. At each time n, $s_d[n]$ is chosen such that $x_d[n] + \mathrm{s}_d[n]$ does not exceed the range of a (20-d)-bit two's complement integer, and the parity of $s_d[n]$ is the same as that of $x_d[n]$. The parity restriction ensures that $x_d[n] + \mathrm{s}_d[n]$ is an even number so its LSB is zero. Discarding the LSB simultaneously halves the quantization block's input value and quantizes the result by one bit. The resulting quantization noise is $\mathrm{s}_d[n]/2$, so the successive requantizer's overall quantization noise is

$$s[n] = \sum_{d=1}^{16} 2^{d-17} s_d[n]. \tag{4}$$

Therefore, $s[n]$ is a linear combination of the $s_d[n]$ sequences, so it inherits the properties of the $\mathrm{s}_d[n]$ sequences.

A key feature of the successive requantizer is that the properties of its quantization noise can be engineered by appropriate design of the $\mathrm{s}_d[n]$ sequences. So far, the only restriction on the $s_d[n]$ sequences is that they must be chosen such that $x_d[n] + s_d[n]$ is a (20-d)-bit two's complement even integer for each n and d. This leaves considerable flexibility in the design of the

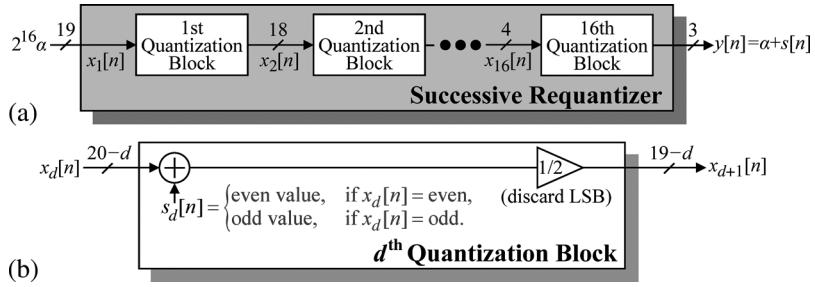
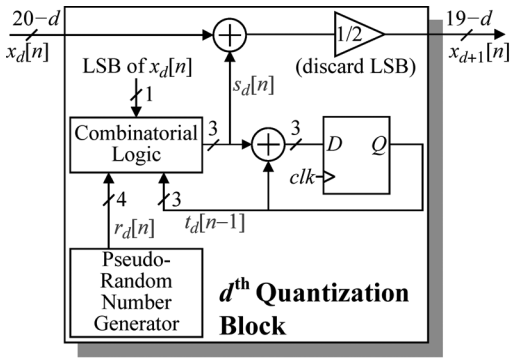


Fig. 5. High-level diagram of an example successive requantizer.



Combinatorial Logic Truth Table:

LSB of $x_d[n]$ = 0			LSB of $x_d[n]$ = 1		
$t_d[n-1]$	$r_d[n]$	$s_d[n]$	$t_d[n-1]$	$r_d[n]$	$s_d[n]$
2	≥ 0 and ≤ 3	0	2	≤ −1 or ≥ 4	−1
2	≤ −1 or ≥ 4	−2	2	≥ 0 and ≤ 3	−3
1	≤ −1 or ≥ 6	0	1	≥ 1 and ≤ 3	1
1	≥ 0 and ≤ 5	−2	1	≤ −1 or ≥ 4	−1
0	0 or 1	2	1	0	−3
0	≤ −1 or ≥ 4	0	0	≥ 0	1
0	2 or 3	−2	0	≤ −1	−1
−1	≤ −1 or ≥ 6	0	−1	≥ 1 and ≤ 3	−1
−1	≥ 0 and ≤ 5	2	−1	≤ −1 or ≥ 4	1
−2	≥ 0 and ≤ 3	0	−1	0	3
−2	≤ −1 or ≥ 4	2	−2	≤ −1 or ≥ 4	1
			−2	≥ 0 and ≤ 3	3

Fig. 6. Implementation of each quantization block for a successive requantizer with $s^p[n], p = 1, 2, 3, 4, 5$, and $t^p[n], p = 1, 2, 3$, that are free of spurious tones.

$s_d[n]$ sequences which is exploited to achieve the desired quantization noise properties.

The successive requantizer partially exploits this flexibility to ensure that the running sum of each $s_d[n]$ sequence, i.e.,

$$t_d[n] = \sum_{k=0}^{n} s_d[k] \tag{5}$$

is bounded for all n, and each $s_d[n]$ has a smooth PSD that increases monotonically with frequency. This implies that $s[n]$ is highpass shaped quantization noise that is free of spurious tones and the PSD of $s[n]$ is zero at $\omega = 0$.

This still leaves flexibility in the design of the $s_d[n]$ sequences which is exploited as described below to ensure that the sequences

$$(s[n])^p \text{ for } p = 1, 2, 3, 4, 5, \text{ and } (t[n])^p \text{ for } p = 1, 2, 3 \tag{6}$$

are free of spurious tones, where $t[n]$ is the running sum of $s[n]$ given by (1). The objective is to ensure that the successive requantizer's quantization noise does not introduce significant spurious tones when subjected to the degree of nonlinear distortion expected from the analog circuits within the PLL. Circuit simulations were used during the PLL's design to verify that preventing spurious tones from occurring in the sequences given by (6) is sufficient to achieve this objective.

The register transfer level details of the dth quantization block are shown in Fig. 6. Each value of $s_d[n]$ is calculated via the combinatorial logic shown in the figure as a function of the previous value of $t_d[n]$, the parity of the current value of $x_d[n]$, and the current value of a 4 bit pseudo-random sequence, $r_d[n]$, where $\{r_d[n], d = 1, 2, \ldots, 16, n = 0, 1, 2, \ldots\}$ well-approximate independent identically distributed random variables. For this design the range of values taken on by $s_d[n]$ and $t_d[n]$ are

$$s_d[n] \in \{-3, -2, -1, 0, 1, 2, 3\}, \text{ and } t_d[n] \in \{-2, -1, 0, 1, 2\}. \tag{7}$$

It can be verified that $t_d[n]$ is a discrete-valued Markov random sequence conditioned on the parity of $x_d[n]$. Whenever $x_d[n]$ is odd the one-step state transition matrix for $t_d[n]$ is given by

$$\mathbf{A_o} = [P\{t_d[n] = T_j | t_d[n-1] = T_i, o_d[n] = 1\}]_{5\times 5} \tag{8}$$

and whenever $x_d[n]$ is even the one-step state transition matrix for $t_d[n]$ is given by

$$\mathbf{A_e} = [P\{t_d[n] = T_j | t_d[n-1] = T_i, o_d[n] = 0\}]_{5\times 5} \tag{9}$$

where $P\{X|Y\}$ denotes the conditional probability of event X given event Y, $o_d[n]$ is the LSB of $x_d[n]$, and $T_1 = -2$, $T_2 = -1$, $T_3 = 0$, $T_4 = 1$, $T_5 = 2$. The specific state transition matrices corresponding to the quantization block shown in Fig. 5 are

$$\mathbf{A_o} = \begin{bmatrix} 0 & 3/4 & 0 & 1/4 & 0 \\ 3/16 & 0 & 3/4 & 0 & 1/16 \\ 0 & 1/2 & 0 & 1/2 & 0 \\ 1/16 & 0 & 3/4 & 0 & 3/16 \\ 0 & 1/4 & 0 & 3/4 & 0 \end{bmatrix} \quad \text{and}$$

$$\mathbf{A_e} = \begin{bmatrix} 1/4 & 0 & 3/4 & 0 & 0 \\ 0 & 5/8 & 0 & 3/8 & 0 \\ 1/8 & 0 & 3/4 & 0 & 1/8 \\ 0 & 3/8 & 0 & 5/8 & 0 \\ 0 & 0 & 3/4 & 0 & 1/4 \end{bmatrix}. \tag{10}$$

As derived in [4], these state transition matrices ensure that the sequences in (6) are free of spurious tones because each is a random process whose autocorrelation function converges to a constant as its time spread increases. Furthermore, the PSD of $s_d[n]$ has a zero at $\omega = 0$ and increases at 6 dB per octave as ω increases from zero. In this respect, the quantization noise shaping of this version of the successive requantizer is comparable to that of a first-order $\Delta\Sigma$ modulator.

Successive requantizers with higher than first-order quantization noise shaping can also be designed. For example, second-order quantization noise shaping can be achieved by quantization blocks that calculate $s_d[n]$ as a function the running sum of $t_d[n]$ in addition to $t_d[n]$, a random sequence, and the parity of $x_d[n]$. However, the fractional-N PLL in this work is a phase noise cancelling fractional-N PLL, so higher than first-order shaping is not necessary because most of the quantization noise is removed prior to the loop filter via a DAC.

A drawback of the quantization block shown in Fig. 6 is that its reduced susceptibility to nonlinearity-induced spurious tones comes at the expense of increased quantization noise power. For example, if it is desired to have quantization noise with a first-order highpass spectral shape, but it is not necessary to prevent nonlinear distortion from inducing spurious tones in the quantization noise and its running sum, a quantization block that implements

$$s_d[n] = \begin{cases} 0, & \text{if } x_d[n] = \text{even} \\ p_d[n], & \text{if } x_d[n] = \text{odd and } t_d[n-1] = 0, \\ 1, & \text{if } x_d[n] = \text{odd and } t_d[n-1] = -1, \\ -1, & \text{if } x_d[n] = \text{odd and } t_d[n-1] = 1, \end{cases} \tag{11}$$

can be used, where $p_d[n]$ is an independent random sequence that takes on the values 1 and -1 with equal probability. In this case $s_d[n]$ takes on values of -1, 0, and 1, whereas the $s_d[n]$ generated by the quantization block of Fig. 6 takes on values of $-3, -2, -1, \ldots, 3$. Consequently, the power of the quantization noise from a quantization block based on (11) is significantly lower than that from the quantization block of Fig. 6.

This example suggests what is likely to be a fundamental tradeoff: reduced susceptibility to nonlinearity-induced spurious tones comes at the expense of increased quantization noise power. The tradeoff has yet to be proven theoretically, but it is exhibited by all variants of the successive requantizer developed to date by the authors. In each case, generating $s_d[n]$ sequences with reduced susceptibility to nonlinearity-induced spurious tones has required choices to be made that increase the power of the $s_d[n]$ sequences. This is not a significant problem in phase noise cancelling fractional-N PLLs, but it is likely to be an issue in fractional-N PLLs without phase noise cancellation. Analytical quantification of the tradeoff and its effect on the performance of fractional-N PLLs without phase noise cancellation are ongoing subjects of research.

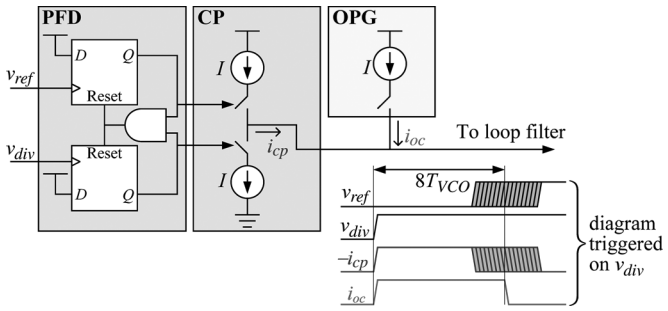


Fig. 7. The phase-frequency detector, charge pump, offset pulse generator and the associated timing diagram.

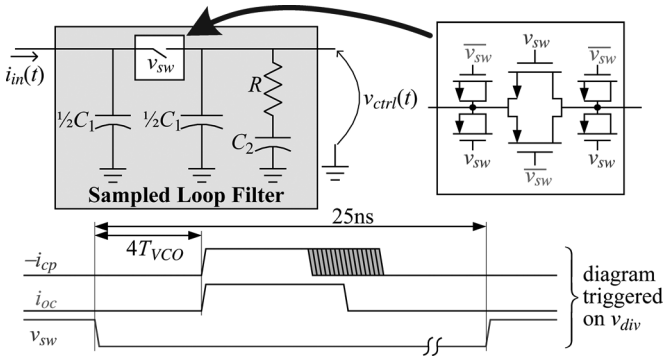


Fig. 8. The sampled loop filter and the associated timing diagram.

IV. A Charge Pump Offset and Sampled Loop Filter

The fractional-N PLL presented in this paper injects a constant current pulse into the loop filter each reference period as a means of mitigating fractional spur mechanism 1 [10]. As shown in Fig. 7, an offset pulse generator in parallel with the charge pump introduces a positive current pulse of amplitude I starting from the rising edge of the divider output and extending for 8 VCO periods. The offset current pulses cause a fixed VCO phase shift such that in each reference period the divider edge always occurs at least 6 VCO periods prior to the reference edge. Separating the edges in this fashion gives the power supply disturbance described in Section III time to die out between the edges, thereby alleviating the coupling problem.

Unfortunately, the offset current pulse technique has a severe side effect if used with a conventional loop filter: transient and amplitude mismatches between the current source in the offset pulse generator and the negative current source in the charge pump add significant power to the reference spur. The effect is more severe than that caused by mismatches between the positive and negative charge pump current sources in a conventional configuration because of the increased duration of the pulses.

The side effect is avoided in this work by the sampled loop filter shown in Fig. 8. It differs from the conventional loop filter shown in Fig. 1 only in that the C_1 capacitor has been split into two parallel half-sized capacitors separated by a CMOS transmission gate switch. Thus, it reduces to a conventional loop filter when the switch is closed. As indicated in Fig. 8, the switch is opened once per reference period for a duration of approximately 25 ns starting 4 VCO periods prior to the rising edge of the divider. This ensures that it is open whenever the loop filter's

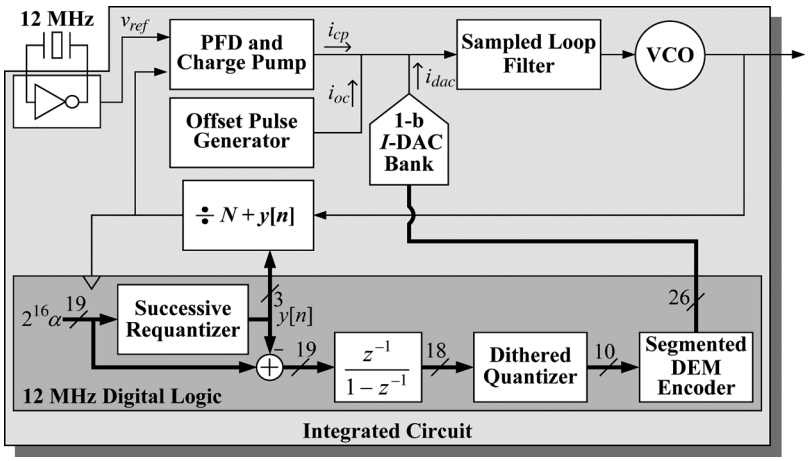


Fig. 9. High-level diagram of the integrated circuit prototype.

input current is non-zero. Once the PLL has settled, the voltage across the switch just before it closes each reference period depends only on circuit noise and quantization noise from the successive requantizer. Therefore, to the extent that the switch is ideal, closing the switch each period does not inject periodic disturbances at the reference frequency so reference spurs are avoided. As with other sampled loop filter designs, this design also eliminates reference spurs caused by mismatches between the current sources in the charge pump [11], [16].

The switch is implemented as a transmission gate with half size dummy transmission gates on either side as shown in Fig. 8. The dummy transmission gates are shorted and driven in opposite polarity to the main transmission gate. Their purpose is to cancel charge injection from the main transmission gate that would otherwise cause a reference spur.

One way to ensure precise cancellation of the charge injection in such a switch configuration is to design the loop filter and surrounding circuitry so the impedances from the two switch terminals to ground are equal. This could have been achieved by placing a series resistance of $2R$ and capacitance of $C_2/2$ from each side of the switch to ground instead of the series resistance of R and capacitance of C_2 on just the right side of the switch as shown in Fig. 8. However, doing so would have prevented the voltage on the left side of the switch from settling to a constant each reference period prior to closing the switch, thereby negating the reference frequency suppression property of the sampling process.

Fortunately, the charge injection is well cancelled despite the asymmetry from the series combination of R and C_2. The edges of the signals that control the transmission gates are sharp, so the charge injected by each MOS transistor is in the form of short-duration, and, hence, high-bandwidth pulses of current. For such a pulse, the impedance of the $(1/2)C_1$ capacitors is much lower than that of the resistor except over a small low-frequency portion of its bandwidth. Therefore, the resistor acts approximately like an open circuit with respect to charge injection pulses, so the series combination of R and C_2 has little effect with respect to charge injection.

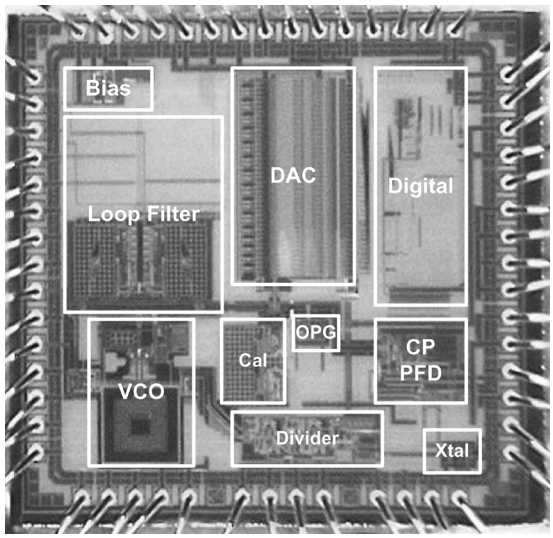


Fig. 10. Die photograph.

V. Additional Circuit Details and Measurement Results

A simplified functional diagram of the phase noise cancelling fractional-N PLL IC prototype is shown in Fig. 9 and a die photograph of the IC is shown in Fig. 10. Its reference frequency is 12 MHz, and its output frequency range covers the 2.4 GHz ISM band. The phase noise cancellation enables a loop bandwidth of 975 kHz which is close to the $f_{\rm ref}/10$ loop bandwidth upper limit for stability [17].

The IC is a modified version of that presented in [13]. The primary modifications are that the successive requantizer shown in Figs. 5 and 6, the offset pulse generator shown in Fig. 7, and the sampled loop filter shown in Fig. 8 have been included. The other circuit blocks of the PLL described in [13] have been reused with relatively minor changes. For comparison, the PLL includes the $\Delta\Sigma$ modulator shown in Fig. 2(a) which can optionally be used instead of the successive requantizer, the offset pulse generator can be enabled or disabled, and the loop filter's

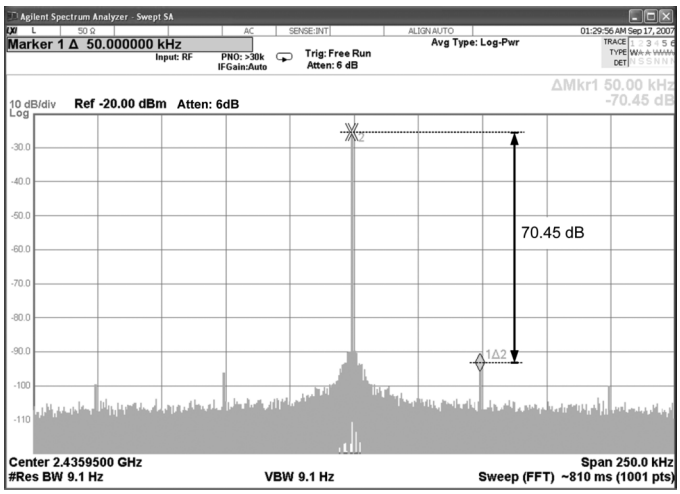


Fig. 11. Representative measured close-in output spectrum for the case of $\alpha f_{\mathrm{ref}} = 50\,\mathrm{kHz}$.

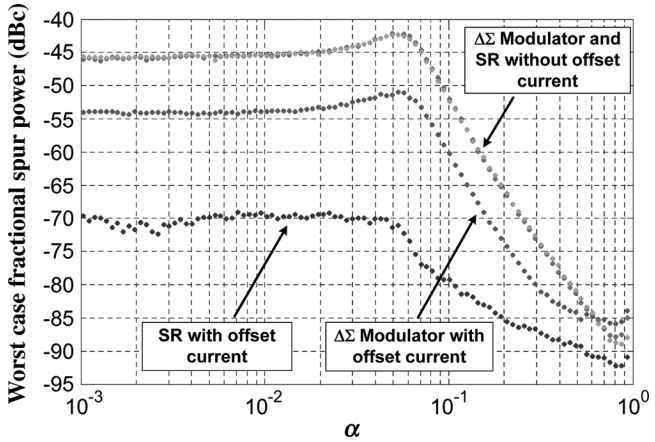


Fig. 12. Power levels of the largest measured fractional spurs with and without the enhancements enabled for 100 PLL frequency offsets in the range $0 < \alpha f_{\mathrm{ref}} < 12\,\mathrm{MHz}$.

sampling can be enabled or disabled. With sampling disabled, the loop filter reduces to a conventional loop filter.

The divider is similar to that presented in [13] except with minor changes to provide timing signals that control the offset current generator and open the loop filter switch each reference period. As described in [13] the necessary timing signals are obtained from a chain of flip-flops clocked at half the VCO frequency. The timing signal used to close the loop filter switch each reference period could have been similarly derived, but an RC one-shot circuit with a nominal duration of 25 ns is used instead for simplicity. Provided the switch is open when the loop filter's input current is non-zero, the PLL dynamics are relatively insensitive to the length of time it is open.

A representative close-in PSD plot of the PLL's output with the successive requantizer, offset pulse generator, and sampled loop filter enabled and α chosen such that $\alpha f_{\mathrm{ref}} = 50\,\mathrm{kHz}$ is shown in Fig. 11. As expected fractional spurs occur at multiples of 50 kHz. Although the fractional spurs are well inside the 975 kHz loop bandwidth, they are all below -70 dBc in power.

To evaluate the fractional spur performance of the PLL comprehensively it is necessary to perform the measurement shown in Fig. 11 for many values of α ranging between 0 and 1. Fig. 12 presents the results of such measurements for four cases: 1) the $\Delta\Sigma$ modulator enabled and the offset pulse generator disabled, 2) the successive requantizer enabled and the offset pulse generator disabled, 3) the $\Delta\Sigma$ modulator enabled and the offset pulse generator enabled, and 4) the successive requantizer enabled and the offset pulse generator enabled. For each case, the figure shows the measured power of the largest spurious tone in the PLL's phase noise for each of 100 values of α ranging between 0 and 1.

As shown in Fig. 12, the fractional spur powers for the two cases in which the offset pulse generator is disabled are almost identical, and are much higher than the corresponding fractional spur powers for the two cases in which the offset pulse generator is enabled. This suggests that fractional spur mechanism 1 is dominant over fractional spur mechanism 2. With the $\Delta\Sigma$ modulator, enabling the offset pulse generator reduces the fractional spur powers by a maximum of 9 dB, and with the successive requantizer, enabling the offset pulse generator reduces the fractional spur powers by a maximum of 27 dB. This suggests that once fractional spur mechanism 1 is circumvented, fractional spur mechanism 2 becomes significant. By circumventing fractional spur mechanism 2, the successive requantizer results in a maximum fractional spur power reduction of 18 dB relative to the $\Delta\Sigma$ modulator case.

As indicated in Fig. 12, in each case the fractional spur powers are relatively constant for small values of α but decrease as α increases above about 0.055. This is expected because the frequencies of the fractional spurs increase with α, so after a point they move outside the loop bandwidth and are attenuated. An unusually large loop bandwidth has been used in this work to provide a worst-case scenario in which to demonstrate the spurious tone suppression techniques presented in the paper. The roll-offs shown in Fig. 12 would start at smaller values of α if the loop bandwidth were decreased.

Representative measured PSD plots of the PLL output over a 25 MHz span are shown in Fig. 13 for the PLL with the sampled loop filter and the PLL with the conventional loop filter. With the conventional loop filter the reference spur power is -40 dBc, which is large because of the large loop bandwidth and low reference frequency. With the sampled loop filter, the reference spur drops to -70 dBc.

Furthermore, it can be seen in Fig. 13 that the phase noise away from the carrier is lower for the case of the sampled loop filter than for the case of the conventional loop filter. This is expected [18]. As described in [9], practical circuit limitations dictate that the current pulses from the charge pump have a fixed amplitude but variable widths whereas those from the DAC have a fixed width but variable amplitudes. Therefore, even if the charge contained in each DAC current pulse perfectly cancels the charge associated with quantization noise in the corresponding charge pump current pulse, a current transient occurs when the charge pump and DAC current pulses are non-zero which disturbs the loop filter voltage. Without sampling, the disturbance modulates the VCO, thereby increasing the phase noise. With sampling, the VCO is shielded from the disturbance.

TABLE I
PERFORMANCE TABLE. SPUR MEASUREMENTS REPRESENT THE WORST CASE RESULTS OVER THE FOUR ICS TESTED

Design Details		
Technology	0.18 um 1P6M CMOS	
Package and Die area	32 pin TQFN, 2.2 mm × 2.2 mm	
Vdd	1.8 V	
Reference frequency	12 MHz	
Output frequency	2.4 – 2.5 GHz	
Measured loop bandwidth	975 kHz	
Measured Current Consumption		
VCO and Divider Buffer	5.9 mA	Core 27.1 mA
Divider	7.3 mA	
Charge Pump, PFD, and Buffers	8.6 mA	
Offset Current	0.6 mA	
Digital	1.9 mA	
DAC	2.8 mA	
Bandgap Bias Generator	5.4 mA	9.8 mA
Crystal Buffer	2.7 mA	
External Buffer	1.7 mA	
Measured Integer-N Performance		
Phase Noise at 100 kHz	-103 dBc/Hz	
Phase Noise at 3 MHz	-125 dBc/Hz	
Reference spur without sampling enabled	-58 dBc	
Reference spur with sampling enabled	-70 dBc	
Measured Fractional-N Performance		
Phase Noise at 100 kHz	-98 dBc/Hz	
Phase Noise at 3 MHz	-121 dBc/Hz	
Worst case in-band fractional spur with ΔΣ modulator	-45 dBc	
Worst case in-band fractional spur with SR	-64 dBc	
Reference spur without sampling enabled	-40 dBc	
Reference spur with sampling enabled	-70 dBc	

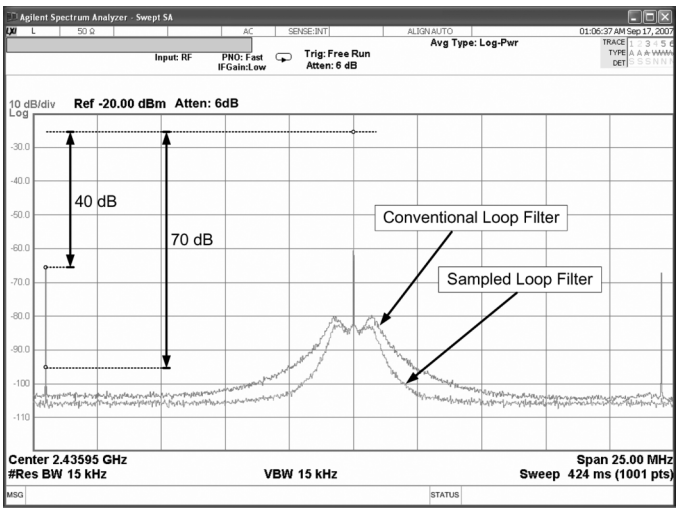


Fig. 13. Representative measured spectra with the sampled loop filter enabled and disabled.

Four copies of the IC were tested. Table I shows the worst-case measurements taken from the four ICs. The fractional spur results for one of the ICs are shown in Fig. 12, and two other of the ICs exhibited very similar results. However, one of the ICs exhibited a worst case fractional spur power of −64 dBc at a small number of frequencies near the edge of the loop bandwidth. At all other frequencies, it behaved similarly to the other three ICs.

An IC wiring mistake disabled the DAC calibration circuitry described in [13], so the measurements described above were made after a one-time manual adjustment of the DAC gain. To confirm the diagnosis of the mistake, it was corrected in one copy of the IC by FIB microsurgery, but with the anticipated side effect of a coupling path that increased the measured in-band phase noise, 3 MHz phase noise, and largest in-band fractional spur by 10 dB, 3 dB, and 3 dB, respectively, above those shown in Table I.

TABLE II
COMPARISON OF REFERENCE SPUR PERFORMANCE TO THE PREVIOUSLY PUBLISHED STATE-OF-THE-ART

Reference frequency (MHz)	Loop bandwidth (kHz)	Reference spur magnitude (dBc)	Normalized reference spur (dBc)	Reference
12	975	-70	-70	This work
8	120	-81	-52	[19]
50	1000	-74	-50	[11]
12	730	-53	-48	[13]
1	40	-62	-50	[16]

Table II compares the PLL's reference spur performance to the previously published state-of-the-art. To a good approximation, the loop filter disturbance that causes reference spurs in a PLL is attenuated by −40 dB per decade in frequency above the loop bandwidth. Therefore, to compare the reference spur powers of any two PLLs meaningfully, the difference between their reference-frequency-to-loop-bandwidth ratios must be considered. For each PLL, Table II shows both the measured reference spur power as well as the *normalized reference spur power*, which is the power that the reference spur would have had the reference frequency-to-loop-bandwidth ratio been 12 MHz/975 kHz as in this paper. As shown in the table, the reference spur performance of the PLL presented in this paper exceeds the previous state-of-the-art by 18 dB.

TABLE III
COMPARISON OF FRACTIONAL SPUR PERFORMANCE TO THE PREVIOUSLY PUBLISHED STATE-OF-THE-ART

Reference frequency (MHz)	Loop bandwidth (kHz)	Reported fractional spur		Equivalent in-band fractional spur (dBc)	Reference
		Frequency (kHz)	Magnitude (dBc)		
12	975	50	-70		This work
50	1000	"In-band"	-45		[11]
35	700	8.5	-60		[10]
50	500	400	-42		[20]
50	390	98	-48		[21]
12	730	1000	-47	-42	[13]
25	1000	3125	-55	-36	[22]
33	200	257	-40	-36	[23]
26	35	2080	-100	-20	[15, 24, 25]

Table III compares the PLL's fractional spur performance to the previously published state-of-the-art. Unfortunately, comprehensive fractional spur measurement results such as shown in Fig. 12 are rare in the previously published literature. In most cases, fractional spur powers are only reported for a small number of frequencies, often above the loop bandwidth. In cases where the power of a fractional spur within the loop bandwidth has been reported, the value is shown in Table III and it is assumed to be representative of all fractional spurs within the loop bandwidth. In cases for which the power of a fractional spur within the loop bandwidth is not reported, Table III provides an *equivalent in-band fractional spur power* obtained by adding the attenuation imposed by the PLL on the fractional spur given its position relative to the loop bandwidth. As in the case of the reference spur, the attenuation is taken to be -40 dB per decade in frequency above the loop bandwidth. As shown in the table, the fractional spur performance of the PLL presented in this paper exceeds the previous state-of-the-art by 10 dB [19]–[25].

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