19.2 Spurious -Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHz Fractional-*N* PLL

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A major problem with fractional-*N* PLLs is that their phase noise contains *fractional spurs*, i.e., spurious tones at multiples of f_{ref} times the fractional part of f_{out}/f_{ref}, where f_{out} and f_{ref} are the PLL output and reference frequencies, respectively. In prior fractional-*N* PLLs fractional spurs within the loop BW tend to be large, typically well above –60dBc [1-4]. Fractional spurs at higher frequencies are attenuated by the loop filter, so for any choice of f_{ref} and f_{out} fractional spur power can be reduced by sufficiently reducing the loop BW. This is the conventional approach to fractional spur suppression once f_{ref} is chosen, but is often undesirable because it increases in-band phase noise, settling time, susceptibility to VCO pulling, and loop filter size.

This paper describes a fractional-*N* PLL IC based on a new digital quantizer that replaces the ΔΣ modulator (ΔΣM) used in conventional designs. In combination with a charge pump offset technique and a sampled loop filter the new quantizer enables state-of-the-art fractional spur performance without sacrificing BW.

Surprisingly, the ΔΣM is a major source of fractional spurs in conventional fractional-*N* PLLs. Regardless of how dither is applied, all ΔΣMs known to the authors introduce spurious tones when their quantization noise is subjected to the non-linear distortion inevitably introduced by the PLL's analog circuitry. To avoid this problem, a completely different type of noise-shaped quantizer, called a *successive requantizer* (SR), is used [5].

The SR is shown in Fig. 19.2.1 with all variables represented as integer-valued two's complement numbers. It quantizes a 19-bit input of $2^{16}\alpha$ to a 3-bit output sequence, $y[n] = \alpha + s[n]$, where α is the fractional part of f_{out}/f_{ref} and $s[n]$ is quantization noise. It consists of 16 quantization blocks that perform quantization 1 bit at a time. The output of the dth quantization block is $x_{d+1}[n] = (x_d[n] + s_d[n])/2$, where $x_d[n]$ is the block's input, and $s_d[n]$ is a 3-bit sequence generated as shown in Fig. 19.2.1. A property of $s_d[n]$ is that it has the same parity as $x_d[n]$, so $x_d[n] + s_d[n]$ is an even number, which implies that its LSB is zero. Division by 2 is performed without error by discarding the LSB and right shifting the remaining bits via wiring. Hence, $x_{d+1}[n]$ can be viewed as a quantized by 1-bit version of $x_d[n]/2$ with quantization noise $s_d[n]/2$.

A key feature of the SR approach is that the properties of its quantization noise can be engineered by appropriate design of the $s_d[n]$ sequences. In the present design $s_d[n]$ is chosen by combinatorial logic as a function of the LSB of $x_d[n]$, the running sum of the previous values of $s_d[n]$ ("$t_d[n]$"), and a 4-bit pseudo-random number as shown in Fig. 19.2.1. This ensures that $s_d[n]$ is a random process constrained such that $|t_d[n]|$ is bounded for all n and, therefore, has a 1st-order highpass spectral shape. Furthermore, it exploits flexibility in satisfying the spectral shaping constraint to ensure that $(s_d[n])^p$, for $p = 1, 2, \ldots, 5$, and $(t_d[n])^p$, for $p = 1, 2, 3$, are free of spurious tones, thereby ensuring that the SR's quantization noise does not introduce spurious tones when subjected to the nonlinearities expected from the PLL's analog circuits. As explained in [5], this is achieved because $(s_d[n])^p$ and $(t_d[n])^p$ are random processes with autocorrelations that converge to constants as their time spreads increase.

A completely different source of fractional spurs in a fractional-*N* PLL is parasitic coupling between the VCO output signal and harmonics of the reference signal. The potential for such coupling is greatest in the phase-frequency detector (PFD) and charge pump (CP), as these blocks handle signals aligned with the reference signal as well as those aligned with the divider output and, hence, the VCO output [1]. The hard-switching that occurs within these blocks induces disturbances on the local power supply lines because of the bond wire inductance, thereby modulating the switching thresholds of gates powered by these supplies. In a conventional PFD, the two flip-flops (Fig. 19.2.2) capture the phase difference, $\Delta\Phi$, between the divider and reference edges. For small $\Delta\Phi$, the disturbance from the earlier edge does not have time to die out before the later edge arrives, so it can modulate the delay through the flip-flop of the later edge, hence corrupting the phase error measurement. Similar coupling effects occur within the CP circuitry. The result is that intermodulation products of the VCO output and reference signal are injected into the loop filter and cause fractional spurs.

In this work the coupling problem is addressed by injecting an offset current (OC) pulse into the loop filter each reference period [1] and using a sampled loop filter to block the periodic disturbance on the VCO control voltage that would otherwise result. The OC pulses cause a constant VCO phase shift such that each clock edge of the reference signal occurs well after the corresponding edge of the divider output. Separating the edges gives the disturbances described above time to die out between the edges, thereby alleviating the coupling problem.

As indicated in Fig. 19.2.2, the loop filter switch is open for the duration of the CP and OC pulses, and closed otherwise. When open, it isolates capacitor C_{1A} from the rest of the loop filter, and when closed, the loop filter reduces to a conventional PLL loop filter. Dummy switches are used to cancel charge injection from the actual switch. It can be shown that the sampled loop filter eliminates periodic disturbances on the VCO control voltage, and therefore reference spurs, that would otherwise be caused by mismatches between the OC pulse generator and the CP. As with similar published sampled loop-filter designs, this design also eliminates a number of other reference spur generation mechanisms [4,6,7].

The enhancements described above are applied to a 2.4GHz phase-noise cancelling PLL IC with a 975kHz loop BW and f_{ref} = 12MHz based on the design presented in [2]. A simplified functional diagram of the IC is shown in Fig. 19.2.3. For comparison purposes, the IC can be configured with either the SR or a 2nd-order ΔΣM, and the OC pulse generator and loop filter switching can each be enabled or disabled.

Results are shown in Figures 19.2.4 to 19.2.7. In particular, Fig. 19.2.5 plots the largest fractional spurs measured with and without the enhancements for PLL frequency offsets in the range $0 < f_{ref} < f_{ref}$. Over all in-band frequencies, the techniques together provide a worst-case fractional spur reduction of 18dB. The worst case reference spur over these measurements is –70dBc. An IC wiring mistake disabled the DAC calibration circuitry described in [2], so the measurements above were made after a one-time manual adjustment of the DAC gain. This circuit was repaired by FIB microsurgery, but with the anticipated side effect of a coupling path that increased the measured in-band phase noise, 3MHz phase noise, and largest in-band fractional spur by 10dB, 3dB and 3dB, respectively.

References:

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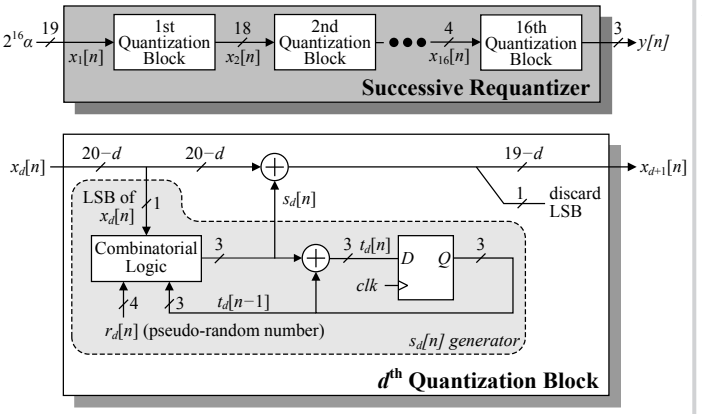

Combinatorial Logic Truth Table:

LSB of $x_d[n] = 0$			LSB of $x_d[n] = 1$		
$t_d[n-1]$	$r_d[n]$	$s_d[n]$	$t_d[n-1]$	$r_d[n]$	$s_d[n]$
2	≥ 0 and ≤ 3	0	2	≤ −1 or ≥ 4	−1
2	≤ −1 or ≥ 4	−2	2	≥ 0 and ≤ 3	−3
1	≤ −1 or ≥ 6	0	1	≥ 1 and ≤ 3	1
1	≥ 0 and ≤ 5	−2	1	≤ −1 or ≥ 4	−1
0	0 or 1	2	1	0	−3
0	≤ −1 or ≥ 4	0	0	≥ 0	1
0	2 or 3	−2	0	≤ −1	−1
−1	≤ −1 or ≥ 6	0	−1	≥ 1 and ≤ 3	−1
−1	≥ 0 and ≤ 5	2	−1	≤ −1 or ≥ 4	1
−2	≥ 0 and ≤ 3	0	−1	0	3
−2	≤ −1 or ≥ 4	2	−2	≤ −1 or ≥ 4	1
			−2	≥ 0 and ≤ 3	3

Figure 19.2.1: The successive requantizer used in place of a ΔΣ modulator.

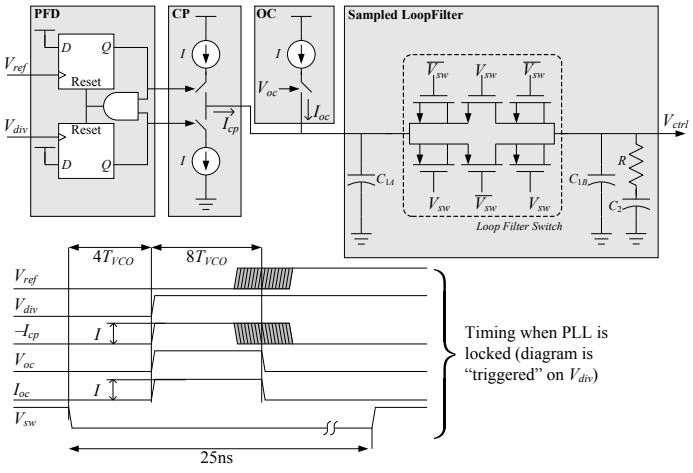

Figure 19.2.2: Functionality and timing of the phase frequency detector (PFD), charge pump (CP), offset current pulse generator (OC) and loop filter.

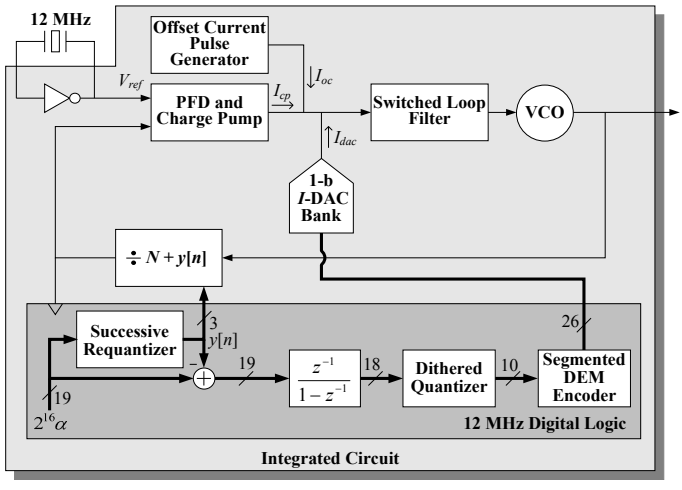

Figure 19.2.3: A simplified functional diagram of the IC.

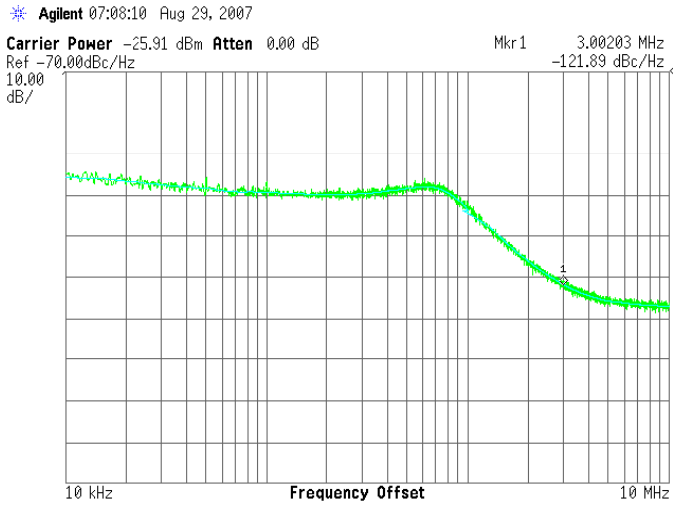

Figure 19.2.4: Representative measured phase noise of the PLL's output signal (f_{out} = 2.436GHz +50kHz).

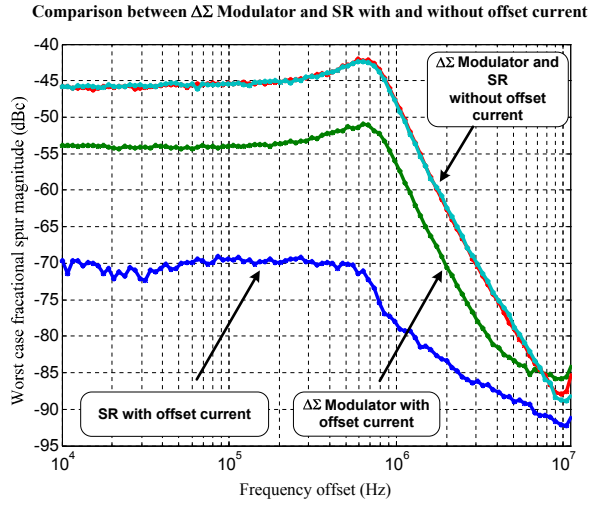

Figure 19.2.5: Plots of the largest measured fractional spurs for 100 PLL frequency offsets in the range 0<αf_{ref} <12MHz with and without the enhancements enabled.

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Design Details		
Technology	0.18 um 1P6M CMOS	
Package and Die area	32 pin TQFN, 2.2 mm × 2.2 mm	
Vdd	1.8 V	
Reference frequency	12 MHz	
Output frequency	2.4 – 2.5 GHz	
Measured loop bandwidth	975 kHz	
Measured Current Consumption		
VCO and Divider Buffer	5.9 mA	Core 27.1 mA
Divider	7.3 mA	
Charge Pump, PFD, and Buffers	8.6 mA	
Offset Current	0.6 mA	
Digital	1.9 mA	
DAC	2.8 mA	
Bandgap Bias Generator	5.4 mA	9.8 mA
Crystal Buffer	2.7 mA	
External Buffer	1.7 mA	
Measured Integer-N Performance		
Phase Noise at 100 kHz	-103 dBc/Hz	
Phase Noise at 3 MHz	-125 dBc/Hz	
Reference spur without sampling enabled	-58 dBc	
Reference spur with sampling enabled	-70 dBc	
Measured Fractional-N Performance		
Phase Noise at 100 kHz	-98 dBc/Hz	
Phase Noise at 3 MHz	-121 dBc/Hz	
Worst case in-band fractional spur with ΔΣ modulator	-45 dBc	
Worst case in-band fractional spur with SR	-64 dBc	
Reference spur without sampling enabled	-40 dBc	
Reference spur with sampling enabled	-70 dBc	

Figure 19.2.6: Performance summary. Spur measurements represent the worst case results over the four ICs tested.

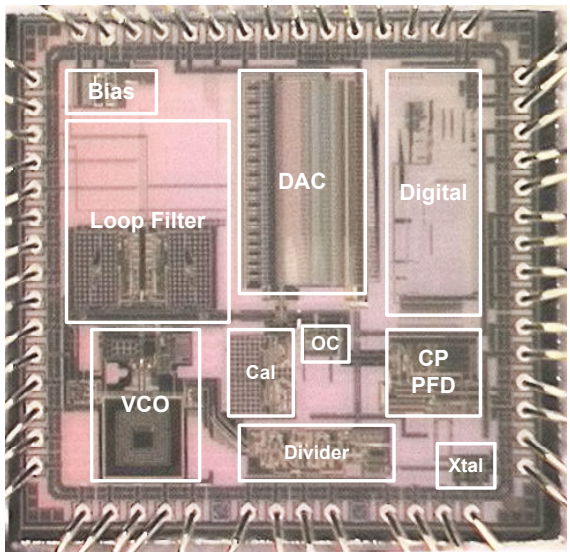

Figure 19.2.7: Die micrograph.

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