A 150MS/s 14-bit Segmented DEM DAC with Greater than 83dB of SFDR Across the Nyquist band

Kok Lim Chan, Jianyu Zhu, Ian Galton
University of California, San Diego, La Jolla, CA 92093, USA

Abstract

A segmented DEM technique that allows an efficient tradeoff between encoder complexity and the number of unit current-steering cells enables a 150MS/s DAC with greater than 83dB of SFDR across the Nyquist band. The 0.18μm CMOS IC has an active area of 3mm^2 and dissipates 127mW.

Paper Body

In [1], dynamic element matching (DEM) is shown to prevent harmonic distortion in a Nyquist-rate current-steering (CS) DAC that would otherwise arise from pulse shape, amplitude, and timing errors caused by component mismatches, and a fully segmented DEM technique is demonstrated that avoids the exponential relationship between the number of bits and circuit complexity inherent to non-segmented DEM. However, fully-segmented DEM has the disadvantage that it requires twice the number of unit CS cells than would be required if non-segmented DEM were used. This paper presents a segmentation technique that allows designers to trade off the advantages and disadvantages of these two extremes, and a highly-linear 150 MS/s Nyquist-rate DAC enabled by the technique. The DAC achieves higher linearity over the Nyquist band for signals above 45 MHz than all other CMOS DACs known to the authors, and dissipates 42% less power than the fully segmented DEM DAC presented in [1].

The DAC consists of a segmented DEM encoder followed by a bank of weighted 1-bit DACs (Fig. 1). The ith 1-bit DAC is controlled by the 1-bit sequence, $x_i[n]$, and has a weight of K_i. K_i is the number of unit CS cells that are connected in parallel within the 1-bit DAC. For example, the 19th 1-bit DAC contains K_{19} = 512 unit CS cells connected in parallel that simultaneously steer their current in the positive direction when $x_{19}[n]$ = 1 and in the negative direction when $x_{19}[n]$ = 0.

The DAC input, $x_{DAC}[n]$, specifies the total number of unit CS cells that must be steered in the positive direction during the nth sample period. There are 18430 unit CS cells in the 1-bit DACs, so $x_{DAC}[n]$ is restricted to the range {0, 1, …, 18430}, and the DEM encoder sets its output bits, $x_1[n]$, …, $x_{36}[n]$, such that the sum of all the $K_i x_i$ equals $x_{DAC}[n]$. As a consequence, $x_i[n]$ can be written as

$$x_i = m_i x_{DAC}[n] + \varepsilon_i[n] \qquad (1)$$

where m_i is a constant and $\varepsilon_i[n]$ a sequence that satisfy

$$\sum_{i=1}^{36} K_i m_i = 1, \quad \text{and} \quad \sum_{i=1}^{36} K_i \varepsilon_i[n] = 0 \qquad (2)$$

For most values of $x_{DAC}[n]$, there are several different choices of $x_1[n]$, …, $x_{36}[n]$ that satisfy these conditions. The DEM encoder makes the choice pseudo-randomly such that the $\varepsilon_i[n]$ sequences in are uncorrelated with $x_{DAC}[n]$ and free of spurious tones. This ensures that mismatches among the 1-bit DACs will not cause harmonic distortion [1-2].

The DEM encoder consists of segmenting and non-segmenting switching blocks (SBs), $S_{k,r}$, as shown in Fig. 1. The segmenting SBs are $S_{14,1}$, $S_{13,1}$, …, $S_{6,1}$, and $S_{5,1}$, and are responsible for segmentation in that they allow 1-bit DACs with different weights. A straightforward, but tedious, analysis indicates that m_i = 1/16384 for i between 21 and 36, and m_i = 0 otherwise, and each $\varepsilon_i[n]$ sequence is a linear combination of the $q_{k,r}[n]$ and $s_{k,r}[n]$ sequences which are functions of independent pseudo-random, white, ±1 sequences, $d_1[n]$, …, $d_{14}[n]$, as shown in Fig 1. It can be verified that the $q_{k,r}[n]$ and $s_{k,r}[n]$ sequences, and, therefore, the $\varepsilon_i[n]$ sequences are uncorrelated with $x_{DAC}[n]$ and free of spurious tones as required. Unfortunately, achieving this goal comes at the price of restricting the usable input range of the DAC. As mentioned above, having 18430 unit CS cells implies that $x_{DAC}[n]$ is restricted to the range {0, 1, …, 18430}. However, the DEM encoder further restricts this range to {1023, 1024, …, 17407}. As an example of what can go wrong if $x_{DAC}[n]$ is outside this range, suppose that $x_{DAC}[n]$ = 17408 and d_1[n], …, $d_{14}[n]$ all equal −1 at some time n. Then it can be verified from Fig. 1 that $x_{21}[n]$ = 2, which is illegal because it is required to be either 0 or 1. Such illegal results will occur only for certain values of the $d_1[n]$, …, $d_{14}[n]$ sequences. However, constraining the $d_1[n]$, …, $d_{14}[n]$ sequences to avoid such illegal results is not a viable option because it causes them to be non-linearly correlated with $x_{DAC}[n]$ which introduces harmonic distortion.

In contrast, a non-segmented DEM DAC with the same input dynamic range requires 16384 unit CS cells, but they must be individually controlled as unity-weighted 1-bit DACs with a DEM encoder that contains 16383 SBs. Compared to the DEM DAC in Fig. 1, this represents a savings of 2046 unit CS cells, but the circuit complexity of the DEM encoder and 1-bit DAC wiring is excessive. At the other extreme, the fully segmented DEM DAC in [1] has the same input dynamic range, but requires 14336 additional unit CS cells while saving only 8 SBs relative to the architecture of Fig. 1. Thus, the architecture of Fig. 1 represents a reasonable tradeoff between the two extremes. Other tradeoff points between fully-segmented and non-segmented DEM can be achieved by varying the number of segmenting SBs according to Fig. 2.

The 1-bit DAC circuits consist of K_i unit CS cells controlled by one or more parallel unit switch drivers (SDs). For example, the 15th 1-bit DAC consists of K_{15} = 128 unit CS cells and L_{15} = 2 unit SDs, as shown in Fig. 3. The unit SD and CS cell circuitry generate a return-to-zero output waveform as in [1]. For optimal pulse-shape matching, the best choice is to have $K_i = L_i$ for each i, where L_i is the number of parallel unit SDs. However, pulse-shape mismatches do not degrade linearity because of the DEM. Therefore, to avoid excessive digital switching noise the number of SDs has been minimized. Specifically, L_i = 1 for i = 1, …, 14, after which it scales with K_i to a maximum value of 16.

A high-level diagram of the IC is shown in Fig. 4. In addition to the DEM encoder and 1-bit DACs, it contains a 14-bit LVDS receiver, a direct digital synthesizer (DDS), a pseudo-random number generator, and a clock buffer. Optionally, $x_{DAC}[n]$ can be provided from off chip via the LVDS receiver, or by the DDS which generates a high spectral-purity full-scale sinusoid.

The emphasis of the design and layout is to ensure that coupling from digital to analog circuits is minimized or data-independent. Five power supply domains separately power the CS cells, the flip-flops in the SDs, the NAND gates in the SDs, the clock buffer, and the remaining digital logic, respectively. Wide supply and ground lines, and multiple supply pins with double bonding are used to minimize parasitic resistance and inductance. All ground lines are down-bonded to the exposed paddle of the QFN package.

Process, package, and measured performance details of the IC are summarized in Fig.7. A representative power spectrum plot and a comparison to other relevant CMOS DACs are shown in Fig.5, and a die photograph is shown in Fig.6.

References

1. K. Chan, I. Galton, "A 14b 100MS/s DAC with Fully Segmented Dynamic Element Matching," *IEEE ISSCC Dig. Tech. Papers*, pp. 582-483, 675, February, 2006.

2. J. Welz, I. Galton, "Necessary and sufficient conditions for mismatch shaping in a general class of multibit DACs", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 12, pp. 748-759, December, 2002.

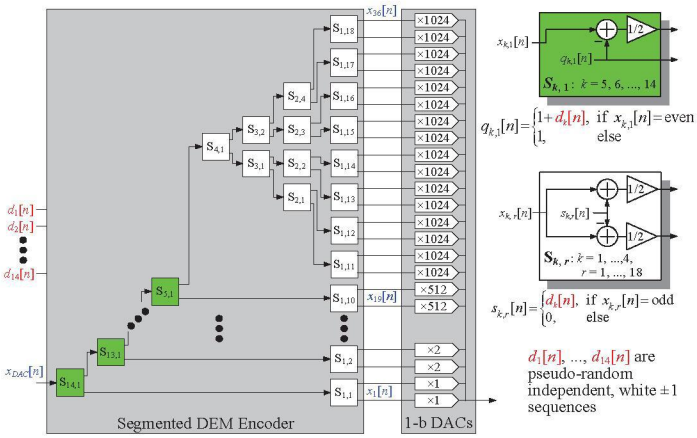

Figure 1: Signal processing details of the segmented DEM DAC.

Number of Seg. SBs	Number of Non-Seg. SBs	Number of Unit Current Steering Cells	Seg. SBs: $S_{k,1}$ k =	1-bit DAC Weights, K_i = $\begin{cases} K_{max}, & \text{if } M < i < N, \\ 2^{\lfloor (i-1)/2 \rfloor}, & \text{if } 1 < i < M. \end{cases}$		
				K_{max}	M	N
0 (non-segmented)	16383	16384	N/A	1	1	16384
1	8192	16386	14	2	2	8194
2	4097	16390	13, 14	4	4	4100
3	2050	16398	12, 13, 14	8	6	2054
4	1027	16414	11, 12, 13, 14	16	8	1032
5	516	16446	10, 11, ..., 14	32	10	522
6	261	16510	9, 10, ..., 14	64	12	258
7	134	16638	8, 9, ..., 14	128	14	142
8	71	16894	7, 8, ..., 14	256	16	80
9	40	17406	6, 7, ..., 14	512	18	50
10 (this work)	25	18430	5, 6, ..., 14	1024	20	36
11	18	20478	4, 5, ..., 14	2048	22	30
12	15	24574	3, 4, ..., 14	4096	24	28
13 (fully segmented)	14	32766	2, 3, ..., 14	8192	26	28

Figure 2: Segmentation tradeoff options for 14-bit DEM DACs (i.e., DEM DACs with an input dynamic range of 16535 levels).

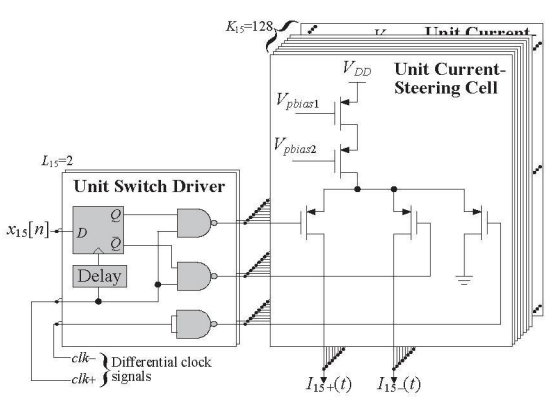

Figure 3: Simplified circuit diagram of the 15th 1-bit DAC.

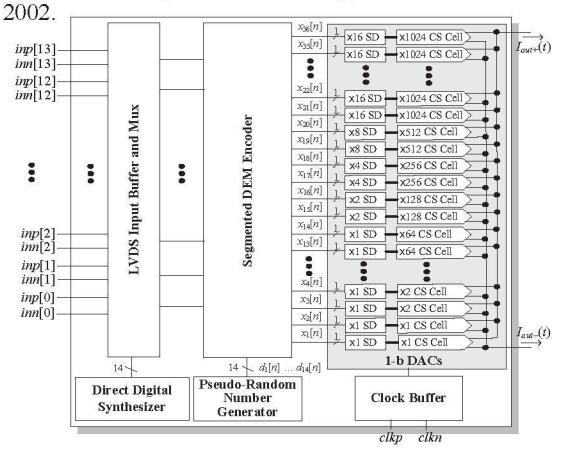

Figure 4: High-level diagram of IC.

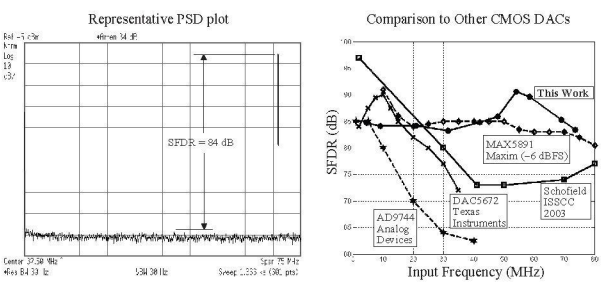

Figure 5: Representative measured power spectrum and measured SFDR versus signal frequency of DAC in comparison to other published CMOS DACs.

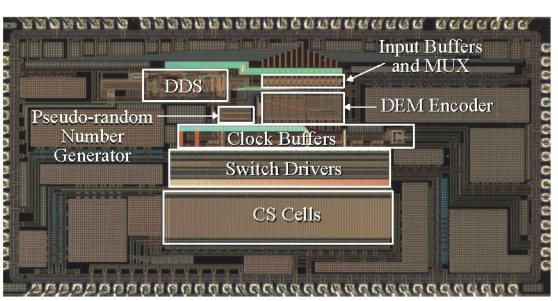

Figure 6: Die Photograph.

Technology	TSMC 0.18μm 1P6M CMOS
Package	QFN 64 with Exposed Paddle
Single-Tone SFDR @ 150MS/s, 0dBFS	>83dB across Nyquist Band >77dB across 2nd Nyquist Band
Two-Tone IMD @ 150MS/s, –6dBFS	>84dB ($f_{out2} - f_{out1}$ = 1MHz)
DNL @ 150 MS/s	±1LSB
INL @ 150 MS/s	+2.5/–3.5LSB
SNR @ 150 MS/s	57dB
Full-Scale Current	16mA
Voltage Supply	1.8V Analog, 2V Digital
Power Dissipation @ 150 MS/s	127mW
Power Dissipation @ 100 MS/s	102mW
Total Die Area (including bond pads with ESD protection on all pins)	4.8mm × 2.4mm
Active Die Area	3mm^2

Figure 7: Summary of Performance.