A Wide-Bandwidth 2.4 GHz ISM Band Fractional-N PLL With Adaptive Phase Noise Cancellation

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***Abstract*—A fast-settling adaptive calibration technique is presented that makes phase noise cancelling $\Delta\Sigma$ fractional-N PLLs practical for the low reference frequencies commonly used in wireless communication systems. The technique is demonstrated as an enabling component of a 2.4 GHz ISM band CMOS PLL IC with a 730 kHz bandwidth, a 12 MHz reference, and an on-chip loop filter. In addition to the adaptive calibration technique, the IC incorporates a dynamic charge pump biasing technique to reduce power dissipation. The worst-case phase noise of the IC is -101 dBc/Hz and -124 dBc/Hz at 100 kHz and 3 MHz offsets, respectively, and the adaptive phase noise cancellation technique has a worst-case settling time of 35 μs. The IC is implemented in 0.18 μm CMOS technology. It measures 2.2 $\times$2.2 mm^2, and its core circuitry consumes 20.9 mA from a 1.8 V supply.**

***Index Terms*—Calibration, CMOS analog integrated circuits, phase-locked loops (PLLs).**

I. Introduction

PHASE NOISE cancellation makes it possible to greatly widen the loop bandwidth of a $\Delta\Sigma$ fractional-N PLL without the massive increase in phase noise that would otherwise be caused by the $\Delta\Sigma$ quantization noise [1]–[3], [5]. This allows the loop filter to be integrated on-chip, reduces sensitivity of the VCO to pulling and noise, better attenuates in-band VCO noise, and makes direct digital frequency modulation practical in wireless applications such as GSM and Bluetooth. However, good phase noise cancellation requires good matching of the cancellation and signal paths, and the matching precision required for a given level of performance increases dramatically as the reference frequency is decreased. For example, if the reference frequency of a $\Delta\Sigma$ fractional-N PLL is halved without changing the PLL bandwidth or the cancellation path matching accuracy, then the power of the output phase noise arising from imperfect cancellation increases by $6(L-(1/2))$ dB where L is the $\Delta\Sigma$ modulation order (usually $L=2$ or 3). To date, PLLs with phase noise cancellation based on passive matching have required reference frequencies of 35 MHz, 48 MHz, and 50 MHz to achieve 15 dB, 20 dB, and 29 dB of phase noise cancellation, respectively [1]–[3]. The need for such high reference frequencies represents a major limitation of phase noise cancellation with passive matching in wireless applications.

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An adaptive calibration technique that addresses this problem is presented in this paper and demonstrated to enable 33 dB of phase noise cancellation in a PLL with a 12 MHz reference frequency [4]. A different adaptive calibration technique is presented in [5], but its settling time is approximately one second which makes it impractical for many applications. In contrast, the calibration technique presented in this paper settles within 35 μs.

Despite the above-mentioned advantages of widening the bandwidth of a $\Delta\Sigma$ fractional-N PLL, a disadvantage is that noise from the charge pump becomes more significant. As the bandwidth of a $\Delta\Sigma$ fractional-N PLL is increased, less of the charge pump noise is filtered by the PLL, so it becomes a more significant component of the overall PLL phase noise. A dynamic charge pump bias circuit is used in this work to achieve low noise performance without excessive power dissipation.

The paper consists of four main sections. Section II briefly reviews $\Delta\Sigma$ fractional-N PLLs and phase noise cancellation, Section III describes the proposed adaptive calibration technique, Section IV describes circuit issues and details of the prototype IC, and Section V presents measurement results.

II. The Phase Noise Cancellation Problem

The block diagram of a conventional $\Delta\Sigma$ fractional-N PLL is shown in Fig. 1 [6]–[8]. The purpose of the system is to generate an output signal of frequency $(N+\alpha)f_{\rm ref}$ where N is a positive integer, α is a constant fractional value between 0 and 1 (or a sequence of such values), and $f_{\rm ref}$ is the frequency of a reference oscillator. The system consists of a phase-frequency detector (PFD), a charge pump, a loop filter, a voltage controlled oscillator (VCO), a multi-modulus divider, and a digital $\Delta\Sigma$ modulator. The divider output, $v_{\rm div}(t)$, is a two-level signal in which the nth and $(n+1)$th rising edges are separated by $N+y[n]$ periods of the VCO output, for $n=1,2,3,\ldots$, where $y[n]$ is a sequence of integers generated by the $\Delta\Sigma$ modulator. As indicated in the figure for the case where the PLL is locked, if the nth rising edge of the reference signal, $v_{\rm ref}(t)$, occurs before that of $v_{\rm div}(t)$, the charge pump generates a positive current pulse of magnitude $I_{\rm CP}$ with a duration equal to the time difference between the two edges. This increases the VCO control voltage, $v_{\rm ctrl}(t)$, thereby increasing the VCO output frequency. Alternatively, if the nth rising edge of $v_{\rm ref}(t)$, occurs after that of $v_{\rm div}(t)$, the situation is similar except the polarity of the current pulse is negative, which decreases the VCO frequency.

If $y[n]$ could be set directly to the desired fractional value, α, then the output frequency of the PLL would settle to $(N+\alpha)f_{\rm ref}$. Unfortunately, $y[n]$ is restricted to integer values because the divider is only able to count integer VCO cycles. To

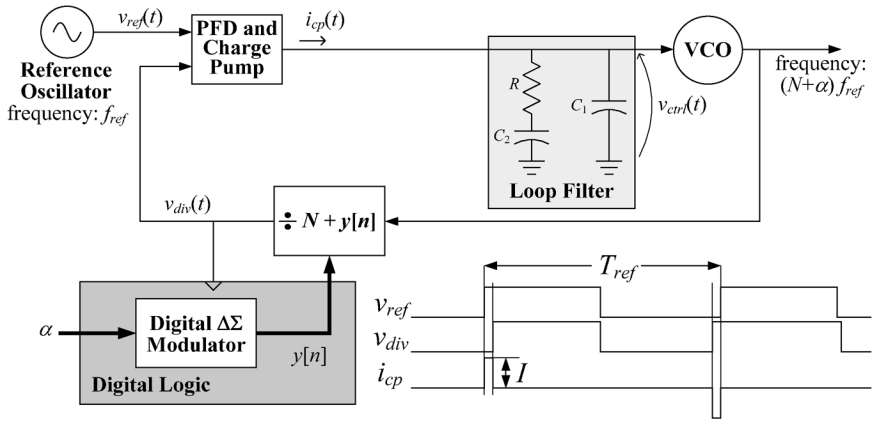

Fig. 1. Block diagram of a fractional-N PLL.

circumvent this limitation, the $\Delta\Sigma$ modulator generates a sequence of integer values that *average* to α. The sequence can be written as $y[n] = \alpha + e_{\Delta\Sigma}[n]$, where $e_{\Delta\Sigma}[n]$ is zero-mean *quantization noise*. Thus, the PLL output frequency settles to $(N+\alpha)f_{\rm ref}$ as desired, although a price is paid in terms of added phase noise resulting from the quantization noise.

As shown in [9], in terms of its effect on the PLL phase noise, the quantization noise can be modeled as a sequence of additive charge samples, $Q_{cp-\Delta\Sigma}[n]$, that get injected into the loop filter once every reference period. Neglecting a constant offset associated with the initial conditions of the loop filter, it can be shown that $Q_{cp-\Delta\Sigma}[n]$ is given by

$$Q_{cp-\Delta\Sigma}[n] = T_{\rm VCO} I_{\rm CP} \sum_{k=n_0}^{n-1} e_{\Delta\Sigma}[k] \tag{1}$$

where $T_{\rm VCO}$ is the period of the VCO output (for a given value of α, $T_{\rm VCO}$ is well-modeled as a constant) and $n_0 < n$ is an arbitrary initial time index. The PLL has the effect of low-pass filtering $Q_{cp-\Delta\Sigma}[n]$ in the process of converting it to output phase noise.

The $\Delta\Sigma$ modulator quantizes its input in such a way that $e_{\Delta\Sigma}[n]$ is spectrally shaped with most of its power concentrated at high frequencies. For example, in a properly dithered second-order $\Delta\Sigma$ modulator, $e_{\Delta\Sigma}[n]$ has a power spectral density (PSD) equal to that of discrete-time white noise with variance 1/12 passed through a high-pass filter with transfer function $(1-z^{-1})^2$ [10]. It follows from (1) that this causes $Q_{cp-\Delta\Sigma}[n]$ to have a PSD equal to that of discrete-time white noise with variance $(T_{\rm VCO}I_{\rm CP})^2/12$ passed through a high-pass filter with transfer function $1-z^{-1}$. Hence, the PSD of $Q_{cp-\Delta\Sigma}[n]$ has a zero at DC and rises at 6 dB per octave in frequency until nearly half the reference frequency. Provided the bandwidth of the PLL is very narrow, most of the power in $Q_{cp-\Delta\Sigma}[n]$ is suppressed by the PLL so it has only a small effect on the overall PLL phase noise. However, as the PLL bandwidth is increased, less of the power in $Q_{cp-\Delta\Sigma}[n]$ is suppressed by the PLL, so its contribution to the PLL phase noise becomes more dominant. Thus, there is a fundamental bandwidth versus phase noise tradeoff in conventional $\Delta\Sigma$ fractional-N PLLs.

Phase noise cancelling $\Delta\Sigma$ fractional-N PLLs attempt to circumvent this tradeoff by cancelling the quantization noise prior to the loop filter, thereby eliminating the need for narrowband filtering by the PLL to suppress the quantization noise. As shown in Fig. 2, the idea is to add a phase noise cancellation path to a conventional $\Delta\Sigma$ fractional-N PLL. The phase noise cancellation path discrete-time integrates the $\Delta\Sigma$ quantization noise to obtain the digital sequence

$$e_{cp}[n] = \sum_{k=n_0}^{n-1} e_{\Delta\Sigma}[n] \tag{2}$$

and converts $-e_{cp}[n]$ via a DAC into a current pulse of duration $T_{\rm DAC}$ and amplitude $-e_{cp}[n]T_{\rm VCO}I_{\rm CP}/T_{\rm DAC}$. To the extent that this can be done accurately, it follows from (1) that the charge in each DAC pulse cancels the $Q_{cp-\Delta\Sigma}[n]$ portion of the charge in the corresponding charge pump pulse.

In practice, the gain of the DAC is never perfectly matched to that of the signal path through the PFD and charge pump, so the cancellation of quantization noise is imperfect. Component mismatches and non-ideal circuit behavior cause both amplitude and transient mismatches between the signals generated by the DAC and the charge pump. This can be modeled by considering the actual amount of charge in each DAC pulse to deviate from its ideal value of $-e_{cp}[n]T_{\rm VCO}I_{\rm CP}$ by a factor of $(1+\beta)$, where β is a small constant that represents the cancellation path mismatch. As shown in [11], the PSD of the component of the PLL phase noise resulting from imperfect cancellation of the quantization noise is given approximately by

$$S_{\theta_{\rm PLL}}(j2\pi f)|_{\Delta\Sigma\ \rm only} = \beta^2 \frac{\pi^2}{3f_{\rm ref}} \left| 2\sin\left(\frac{\pi f}{f_{\rm ref}}\right)\right|^{2(L-1)} \times |A_\theta(j2\pi f)|^2 \quad {\rm rad}^2/{\rm Hz} \tag{3}$$

where $A_\theta(s)$ is the low-pass transfer function of the PLL from the phase of the reference oscillator to the phase of the PLL output normalized to unity at $s=0$, and L is the order of the $\Delta\Sigma$ modulator.

In general, $A_\theta(j2\pi f)$, has a bandwidth much less than the reference frequency. Given that $\sin(x) \approx x$ when $|x| \ll 12$, it follows from (3) that the integrated phase noise associated with

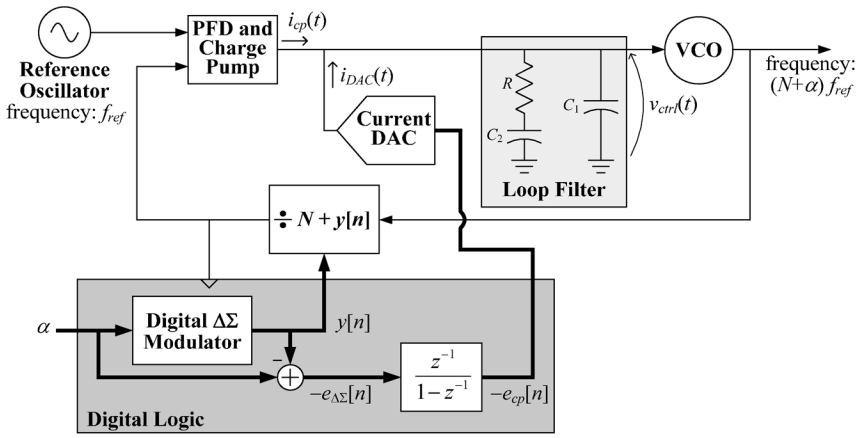

Fig. 2. Block diagram of a phase noise cancelling fractional-N PLL.

imperfect quantization noise cancellation is approximately proportional to $\beta^2/f_{\rm ref}^{2L-1}$. This indicates how the matching accuracy required for a given level of phase noise cancellation depends on the reference frequency. For example, suppose two phase noise cancelling PLLs have equal bandwidths and $\Delta\Sigma$ modulator orders, but their reference frequencies and DAC gain mismatches are given by $f_{\rm ref1}$ and $f_{\rm ref2}$ and β_1 and β_2, respectively. To ensure that the portions of their integrated phase noise powers associated with imperfect quantization noise cancellation are equal, it follows that the relation

$$\frac{\beta_1^2}{f_{\rm ref1}^{2L-1}} = \frac{\beta_2^2}{f_{\rm ref2}^{2L-1}} \tag{4}$$

must hold. In particular, if $f_{\rm ref2} = f_{\rm ref1}/2$, then $\beta_2 = \beta_1/2^{L-1/2}$. Thus, phase noise cancellation becomes increasingly difficult as the reference frequency is decreased. The purpose of the adaptive calibration technique presented in the following section is to address this problem by adaptively adjusting the DAC gain to minimize $|\beta|$.

In addition to the gain mismatch problem described above, another type of mismatch between the charge pump and DAC occurs in practice. Specifically, the charge pump pulses have a fixed amplitude and variable widths, whereas the DAC pulses have a fixed width and variable amplitudes. Unfortunately, this discrepancy is dictated by circuit limitations; to date it has not been practical to generate the timing signals needed to implement width-modulated DAC pulses that have sufficient accuracy. The result of the discrepancy is illustrated in Fig. 3 for the ideal matching case of $\beta = 0$. The component of $v_{\rm ctrl}(t)$ corresponding to quantization noise indeed goes to zero *between* DAC and charge pump pulses, but the cancellation is imperfect *during* the DAC and charge pump pulses. Thus, even if $|\beta|$ is made negligibly small, the quantization noise cancellation is imperfect in practice. Fortunately, as described further in Section IV, the resulting phase noise is very small provided $T_{\rm DAC}$ is relatively small and the DAC pulses are timed so as to overlap the charge pump pulses as much as possible. Alternatively, a sampled loop filter configuration can be used to address the problem as described in [3].

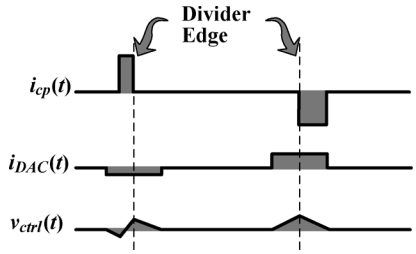

Fig. 3. Effect of cancelling pulse-width modulated charge pump pulses using pulse-amplitude modulated DAC pulses.

III. Adaptive Calibration

In principle, the sign-error LMS algorithm can be used to adaptively adjust the DAC gain to minimize $|\beta|$ [12]. Whenever the DAC gain is not ideal, imperfect cancellation of the quantization noise causes the charge pump and DAC pulses to inject an undesired net charge of $\beta Q_{cp-\Delta\Sigma}[n] = \beta T_{\rm VCO} I_{\rm CP} e_{cp}[n]$ into the loop filter each reference period. Suppose that a copy of these current pulses were multiplied by the sign of $e_{cp}[n]$, i.e., by

$$\mathrm{sgn}\,\{e_{cp}[n]\} = \begin{cases} 1, & \text{if } e_{cp}[n] \geq 0 \\ -1, & \text{if } e_{cp}[n] < 0 \end{cases} \tag{5}$$

and then injected into an integrating low-pass filter (i.e., a low-pass filter with a pole at $s = 0$). In general, $\mathrm{sgn}\{e_{cp}[n]\}$ has zero mean and is uncorrelated with all the noise sources in the PLL other than the quantization noise. Moreover, $e_{cp}[n]\mathrm{sgn}\{e_{cp}[n]\} = |e_{cp}[n]|$. Therefore, if $\beta > 0$, the output of the integrating low-pass filter would ramp up over time, and if $\beta < 0$, it would ramp down over time. If the output of the integrating low-pass filter were used to control the gain of the DAC in a stable negative feedback configuration, then the feedback loop would continuously adjust the DAC gain toward the ideal case of $\beta = 0$.

In practice, however, creating sufficiently accurate copies of the DAC and charge pump pulses multiplied by $e_{cp}[n]$ is challenging. This problem is circumvented in [5] by simply multiplying a buffered copy of $v_{\rm ctrl}(t)$ by $\mathrm{sgn}\{e_{cp}[n]\}$ as depicted

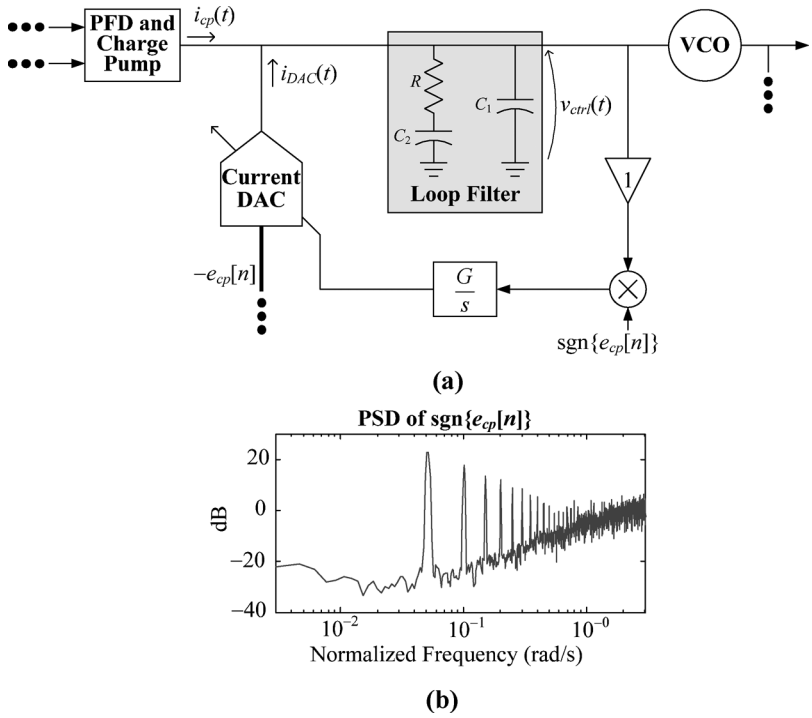

Fig. 4. (a) Block diagram of the adaptive calibration technique proposed in [5]. (b) Simulated discrete-time PSD of the sign of $e_{cp}[n]$.

in Fig. 4(a). It can be shown that the resulting system implements an approximate version of the sign-error LMS algorithm described above. Although the feedback loop can be made to work properly, a practical problem arises because of the DC component in $v_{\mathrm{ctrl}}(t)$. The DC component is necessary because it sets the frequency of the VCO, and the range of values it can take on as a function of the desired output frequency tends to be large. The problem is that the DC component gets multiplied by $\mathrm{sgn}\{e_{cp}[n]\}$ and then fed back through the integrator to control the DAC gain. If the feedback loop bandwidth is not sufficiently small, the resulting modulation of the DAC gain severely degrades the phase noise performance of the PLL. Unfortunately, as demonstrated via simulation results shown in Fig. 4(b), the PSD of $\mathrm{sgn}\{e_{cp}[n]\}$ tends to have large spurious tones. The tones arise from the strong nonlinearity imposed by the $\mathrm{sgn}\{\}$ function, even when the $\Delta\Sigma$ modulator's quantization noise is free of spurious tones [2]. The tone frequencies are multiples of αf_{ref}, so they decrease with the fractional frequency value, α. Therefore, the LMS feedback loop bandwidth must be made very small to sufficiently attenuate the tones, and this results in very slow adaptive calibration settling. For example, the settling time reported in [5] is approximately 1 second.

The proposed adaptive calibration technique avoids this problem via the split loop filter architecture shown in Fig. 5. Two half-sized loop filters separately drive half-sized parallel varactors in the VCO and also drive a differential integrator in the LMS feedback loop. The two varactor capacitances add together in the VCO tank, so the VCO frequency depends on the common-mode loop filter voltage and is relatively insensitive to differential-mode voltage. In contrast, the differential integrator operates on the differential-mode voltage from the two loop filters but rejects their common-mode voltage.

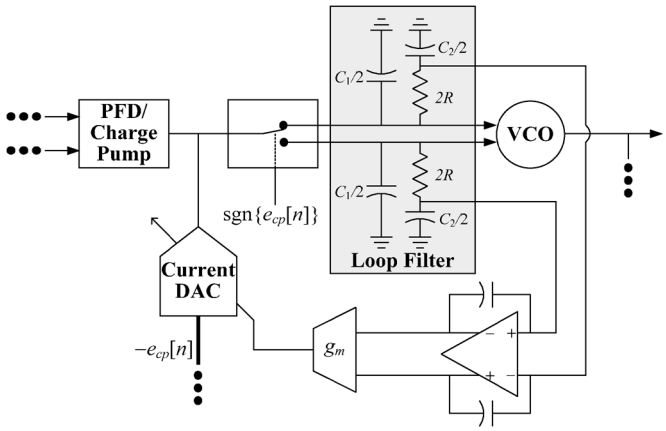

Fig. 5. Block diagram of the proposed adaptive calibration technique.

Since the differential-mode voltage is DC-free, the problem mentioned above is avoided. Multiplication by $\mathrm{sgn}\{e_{cp}[n]\}$ is achieved by steering the DAC and charge pump current to the top loop filter whenever $\mathrm{sgn}\{e_{cp}[n]\} = 1$ and to the bottom loop filter whenever $\mathrm{sgn}\{e_{cp}[n]\} = -1$. Hence, the dynamics of the LMS calibration loop are determined by the differential-mode half circuit, and those of the PLL are determined by the common-mode half circuit, both of which are shown in Fig. 6.

The operation of the LMS calibration loop can be seen from the differential-mode half circuit in Fig. 6. The current steering operation effectively multiplies the charge pump and DAC pulses each reference period by $\mathrm{sgn}\{e_{cp}[n]\}$. The two pulses are then filtered and integrated as shown in the figure to generate a current, ΔI_{bias}, which is used to adjust the bias

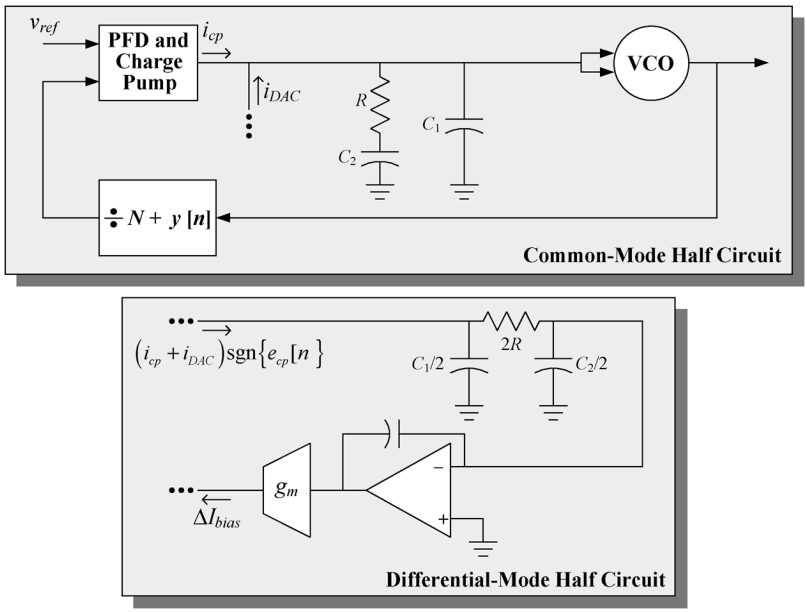

Fig. 6. Half-circuit representations of the PLL and the LMS calibration loop.

current, and therefore the gain, of the DAC. Since the charge pump and DAC pulses are multiplied by $\text{sgn}\{e_{cp}[n]\}$ prior to filtering, the system implements the true sign-error LMS algorithm described above. By avoiding the DC offset problem, the signal that gets integrated by the LMS feedback loop does not contain a term proportional to $\text{sgn}\{e_{cp}[n]\}$. Therefore, the LMS feedback loop bandwidth can be relatively large without significantly degrading the PLL's phase noise performance.

The dynamics of the PLL are implied by the common-mode half circuit shown in Fig. 6, which is equivalent to the core of a conventional phase noise cancelling PLL. To the extent that the two loop filter half circuits and the two varactor halves are matched, respectively, the current steering operation controlled by $\text{sgn}\{e_{cp}[n]\}$ has no affect the common-mode half circuit. Although mismatches between the two loop filter halves and between the two varactor halves do cause some degradation of the PLL's phase noise in practice, simulation and measurement results indicate that the phase noise resulting from such mismatches is well below that caused by other noise sources in the PLL. Furthermore, careful analysis and simulation indicate that even high levels of differential-mode to common-mode and common-mode to differential-mode conversion do not cause the PLL or the LMS feedback loop to become unstable.

IV. Circuit Details

A. Overview

A block diagram of the IC is shown in Fig. 7. With the exception of the crystal, all blocks shown in the figure are integrated on chip, as well as a 3-wire digital interface to control the IC, a VCO output buffer and a buffer connected between the VCO and the divider.

The IC is implemented in the TSMC 0.18 μm single poly, six metal CMOS technology with thin top metal, metal-insulator-metal (MiM) capacitor, poly resistor, and deep n-well process options. All circuitry is operated from a 1.8 V supply, and electrostatic discharge (ESD) protection circuitry is included for all the pads. Separate deep n-wells and supply domains are used to help provide isolation.

B. Divider and DAC Pulse Timing

The divider core consists of seven stages of divide-by-two pulse-swallowing blocks as shown in Fig. 8 [13]. The two highest frequency blocks are implemented with current-mode logic (CML) and the remaining five blocks are implemented with CMOS logic. The output of the divider core is resynchronized to the output of the first CML block to remove jitter from the last six pulse-swallowing blocks, and to reduce modulus-dependent divider delays, i.e., differences between the ideal and actual times of the divider's output edges that depend on $N + y[n]$ [2]. The purpose of the two flip-flops shown in Fig. 8 that are clocked by the outputs of the second and third pulse-swallowing blocks, respectively, is to avoid race conditions in the resynchronization circuitry. In addition to $v_{\text{div}}(t)$, the divider generates enable signals for the charge pump dynamic bias and DAC circuits, which are discussed below.

As mentioned in Section II, the use of fixed-width DAC pulses to cancel the quantization noise in fixed-amplitude charge pump pulses causes imperfect cancellation while the pulses are active. To date, most published phase noise cancelling $\Delta\Sigma$ fractional-N PLLs align the rising edge of each DAC pulse with a rising edge of $v_{\text{div}}(t)$ as shown in Fig. 9(a) [1], [2], [5]. To the extent that the DAC and charge pump pulses do not overlap, the loop filter is disturbed significantly before the charge delivered by the two pulses cancel each other. For example, if the charge pump pulse occurs before the DAC pulse as shown in Fig. 9(a), the entire charge pump pulse is injected into the loop filter before its charge is cancelled by the DAC pulse. This disturbs $v_{\text{ctrl}}(t)$ and contributes to the overall PLL phase noise more than would occur if the charge pump

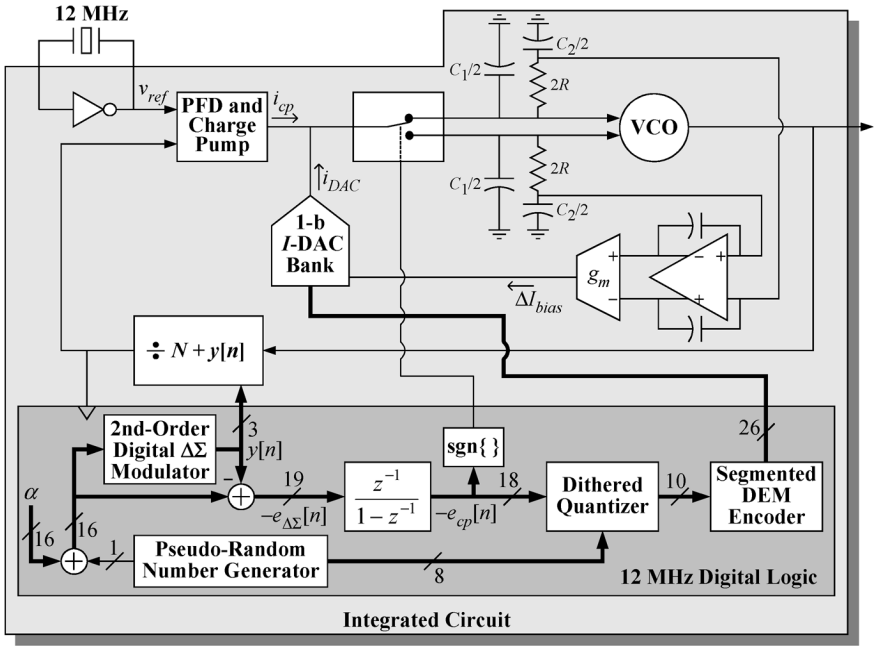

Fig. 7. Block diagram of integrated circuit.

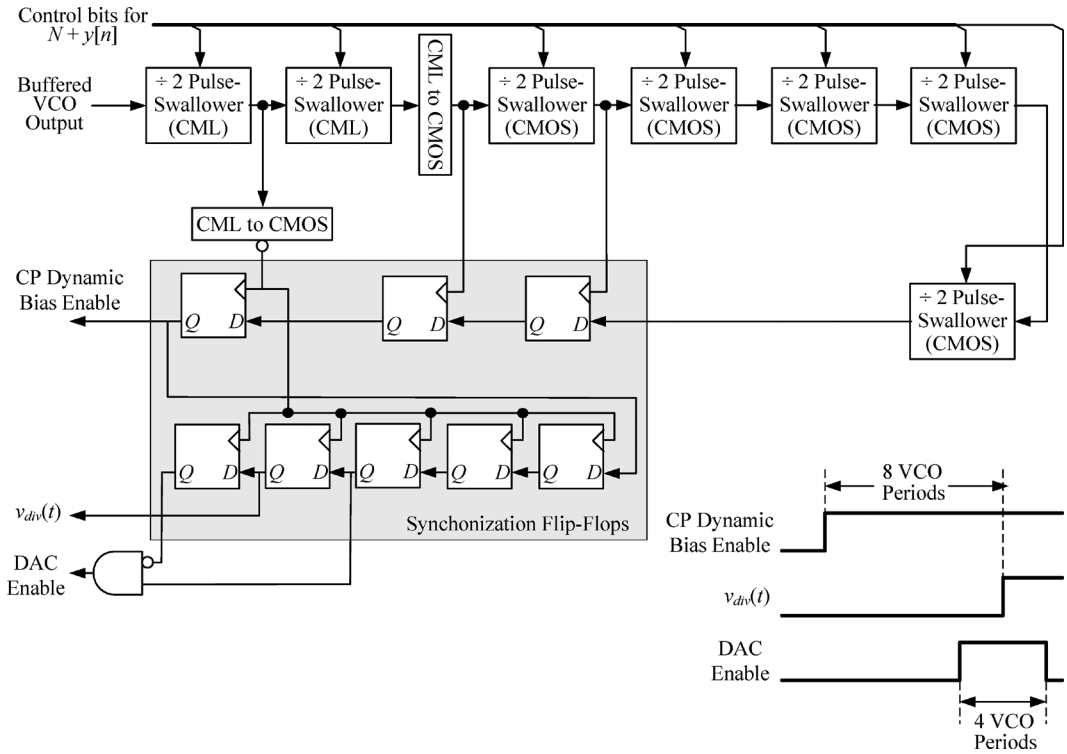

Fig. 8. Divider architecture.

and DAC pulses were timed to overlap each other as shown in Fig. 9(c).

Simulated PSDs of the PLL phase noise caused by the disturbance of $v_{\rm ctrl}(t)$ during the charge pump and DAC pulses for the two cases shown in Fig. 9(a) and (c) are shown in Fig. 9(b) and (d), respectively. As suggested by the simulation results, the simple timing modification implemented in this work relative to the designs described in [1], [2], and [5] significantly reduces the phase noise resulting from the inherent mismatch between the amplitude modulated DAC pulses and the width-modulated charge pump pulses.

C. Cancellation Path Circuitry

The architecture of the 10-bit current-steering DAC is shown in Fig. 10. The DAC consists of a segmented dynamic element matching (DEM) encoder followed by two banks of 26

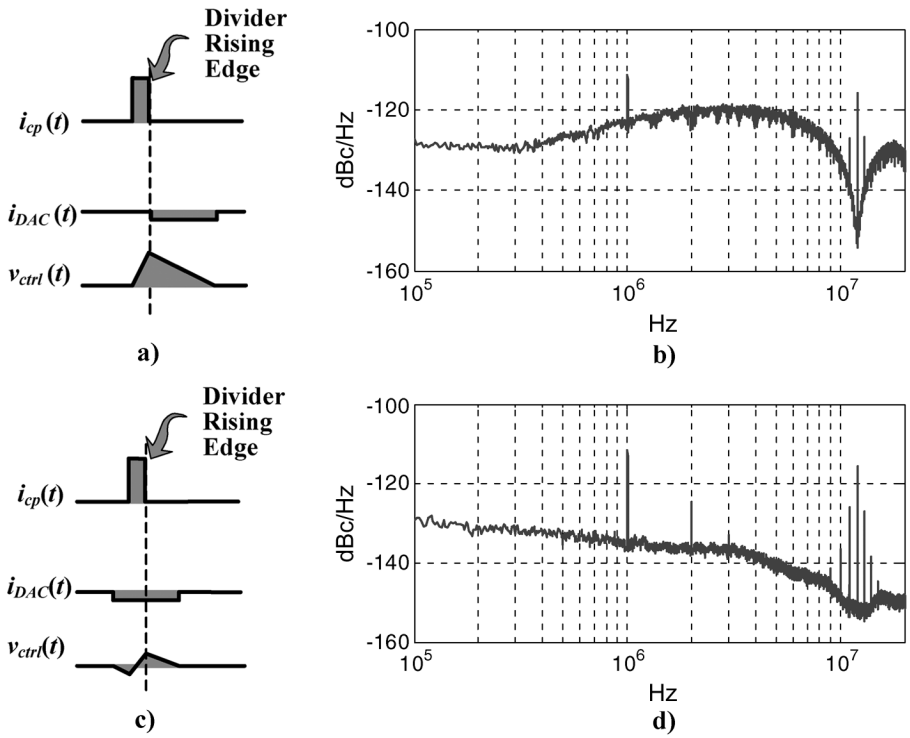

Fig. 9. (a) DAC pulse aligned with divider rising edge. (b) Simulated PLL phase noise for DAC pulse timing in (a). (c) DAC pulse overlapping divider rising edge. (d) Simulated PLL phase noise for DAC pulse timing in (c).

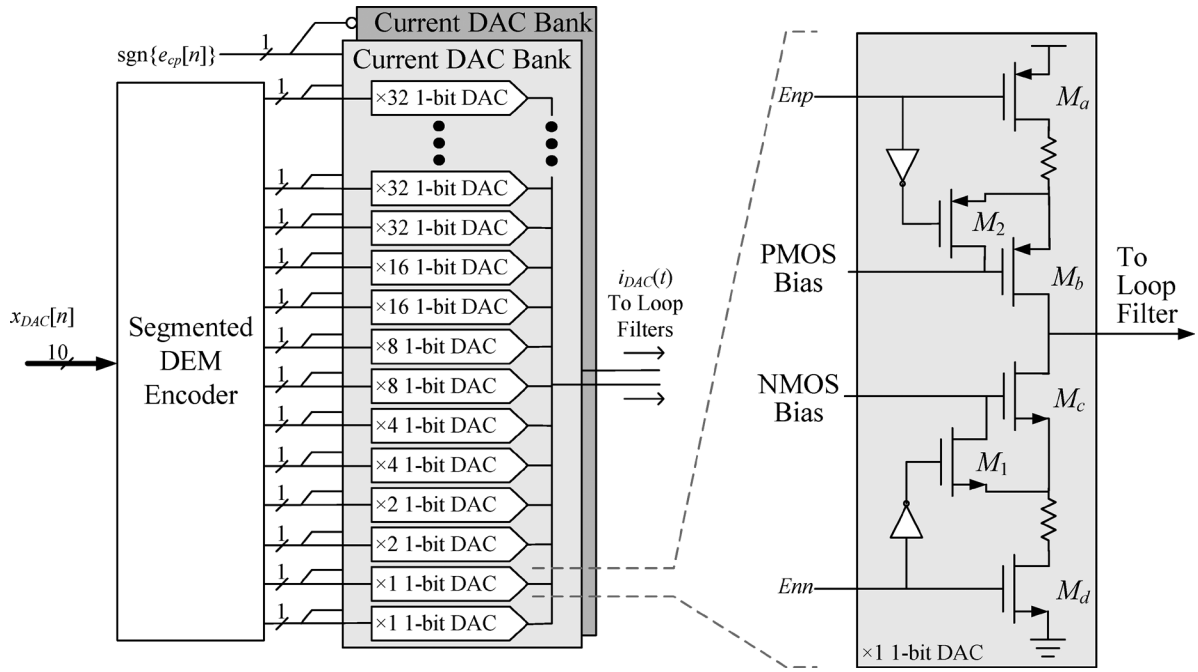

Fig. 10. DAC architecture and circuit.

weighted, return-to-zero, one-bit current DACs. The outputs of the one-bit current DACs in each bank are connected to one of the two loop filter halves. During each reference period, one or the other of the two banks of one-bit current DACs is enabled depending upon the sign of $\mathrm{sgn}\{e_{cp}[n]\}$. This implements the effect of the current steering switch shown in Fig. 7 for the current pulses from the 10-bit DAC. In each of the DAC banks, there are 16 one-bit current DACs with a weight of 32 LSBs, and five pairs of one-bit current DACs with weights of 1, 2, 4, 8, and 16 LSBs, respectively.

Each one-bit current DAC consists of two resistively degenerated current sources that are enabled in a manner similar to that of the charge pump. Large devices are used to minimize mismatches. Unfortunately, this causes the channel charge contained in M_a, M_b, M_c and M_d to be large relative to the charge in the current pulse from the one-bit DAC. When the current

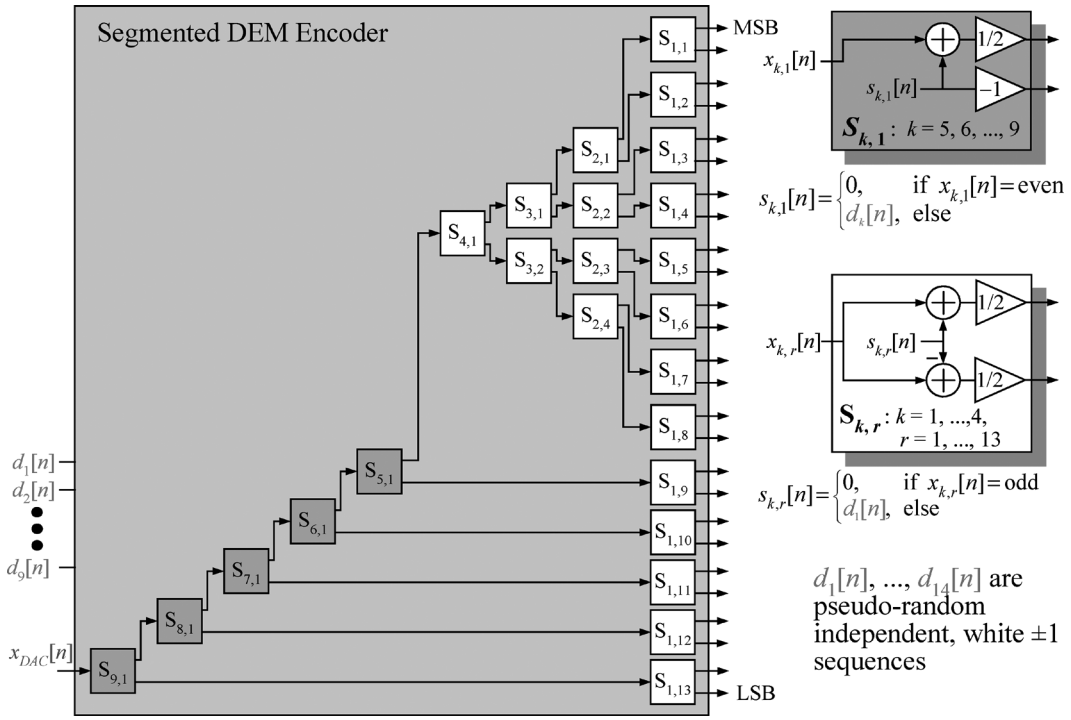

Fig. 11. Segmented dynamic element matching encoder.

source is switched off, this unwanted channel charge is injected into the loop filter. To mitigate this problem, transistors M_1 and M_2 are used to short the source and gate of M_b and of M_c at the end of each DAC current pulse. This causes most of the channel charge to be injected into the DAC bias line instead of the loop filter. The resulting disturbance of the DAC bias occurs at the end of the DAC current pulse, and the bias voltages have enough time to settle to their correct values prior to the next pulse, at which time M_1 and M_2 are opened.

The purpose of the DEM encoder is to prevent amplitude and transient errors arising from component mismatches among the one-bit current DACs from introducing harmonic distortion. The details of the DEM encoder are shown in Fig. 11. Its architecture and functionality are similar to those of the DEM encoder presented [14].

Although $e_{cp}[n]$ is an 18-bit digital number as shown in Fig. 7, it is requantized to 10 bits to reduce the required precision of the DAC. An 8-bit pseudo-random sequence is added to the least significant bits of $e_{cp}[n]$, and the result is truncated to 10 bits to ensure that the requantization process does not introduce harmonic distortion [15].

D. Charge Pump Noise Issues in Wide Bandwidth PLLs

A PLL's charge pump can be viewed as the combination of two blocks: a charge pump bias generator, and a charge pump output stage. Each current source in the charge pump output stage is mirrored from a reference current generated in the charge pump bias generator. Therefore, the charge pump output noise has a component with a power equal to x^2 times the power of any noise on the reference current, where x is the ratio of the current mirror. The unfortunate consequence is that each time a charge pump output stage's current is doubled without changing the bias generator, noise from the bias generator is increased by 6 dB. In general, to minimize the overall noise contribution from the two blocks, it is usually desirable to have $x \leq 1$ (i.e., to have the reference currents at least as large as the charge pump output currents).

If the charge pump current were doubled by doubling the width of all the transistors in both the bias generator and the output stage, then the total charge pump noise power would increase by 3 dB. However, the power of the charge pump signal would increase by 6 dB, so the total signal-to-noise ratio would improve by 3 dB. Thus, in order to increase the signal-to-noise ratio of a charge pump by 3 dB for a given set of current mirror ratios, its total current consumption must be doubled.

As a PLL's bandwidth is increased, less of the charge pump noise is low-pass filtered by the PLL so charge pump noise becomes a more dominant component of the PLL's total phase noise. In particular, each time the PLL's bandwidth is doubled, the component of its phase noise arising from charge pump noise increases by 3 dB. Thus, to double a PLL's bandwidth without increasing the power of the phase noise arising from charge pump noise generally requires the total current consumption of the charge pump to double.

Consequently, the total current consumption of the charge pump becomes significant as the PLL bandwidth is widened. For example, in order to achieve the desired target specifications, the charge pump bias generator and the charge pump output stage in the IC were designed to consume peak currents of 10 mA and 2 mA, respectively. The average current consumed by the charge pump output stage is very low, because the charge pump is only on for a small portion of each reference period. However, in most designs the charge pump bias generator is left on.

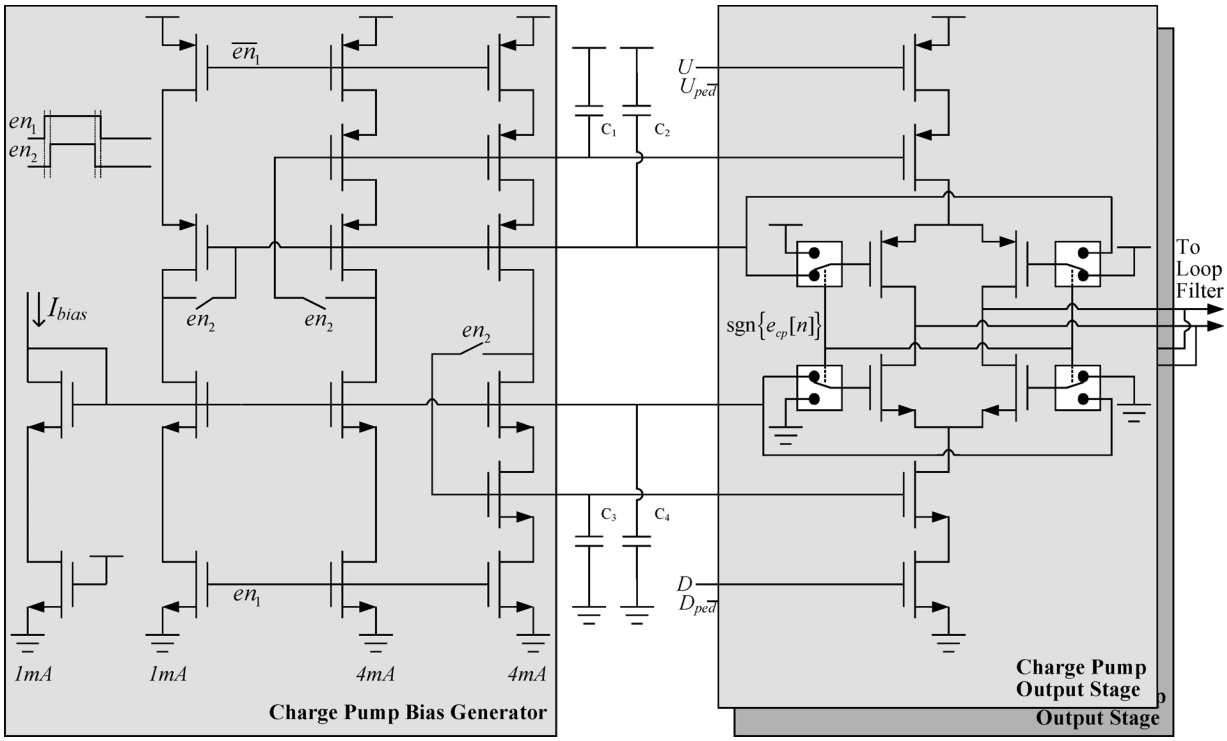

Fig. 12. CP circuit with dynamic bias technique.

Had this been done on the IC, the charge pump would have consumed an average current of just over 10 mA which is more than 50% of the current consumed by all the other circuit blocks in the PLL combined.

Instead, current is saved by powering up most of the circuitry in the charge pump bias generator for only 1/8 of each reference period just before the charge pump output stage is turned on. The dynamic biasing idea was proposed in [16] without a description of the circuit details. The circuit used to implement dynamic biasing in this work is shown in Fig. 12. On average, the dynamic biasing circuit reduces the average current consumption of the charge pump by almost 8 mA.

The PFD is identical to that described in [2]. It generates signals U, D, U_{ped}, and D_{ped} which control the two charge pump output stages shown in Fig. 12. Together, the PFD and charge pump realize a linearization scheme that reduces errors from mismatches between the positive and negative charge pump currents.

E. Other Circuitry

All other circuitry in the IC is relatively conventional. The VCO is a negative-g_m CMOS LC oscillator with a differential spiral inductor stacked in metal layers 5 and 6. Two equal MOS varactors provide tuning over a 0.6–1.2 V range with a nominal $K_{\rm VCO}$ of 60 MHz/V from each input. Coarse digital tuning is provided by switching MIM capacitors of 20 fF and 80 fF into the VCO tank. This allows the VCO to operate over the full 2.4 GHz ISM band [17]. Two buffers are ac coupled to the VCO, and separately drive the divider and an off-chip 50 Ω load. The fully integrated loop filter consists of two 5 kΩ polysilicon resistors, two 18 pF MiM capacitors, and two 282 pF pMOS capacitors. Coarse digital tuning is provided to account for process variations. A folded cascode, single-stage OTA followed by a simple voltage to current converter is used in the LMS feedback loop.

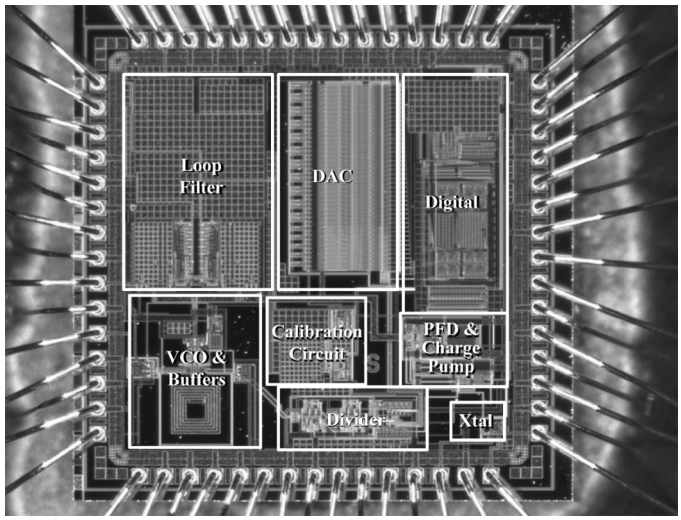

Fig. 13. Die photograph.

V. Measurement Results

A photograph of the IC die is shown in Fig. 13. The die measures 2.2 mm by 2.2 mm including ESD devices and pads. The IC was tested in a 32 pin QFN package.

The current consumption of the PLL circuitry in the IC is 20.9 mA with the dynamic charge pump bias technique enabled. When the dynamic charge pump bias technique is disabled, the total current consumption increases by 8 mA although neither

TABLE I
PERFORMANCE SUMMARY

Design Details		
Technology	TSMC 0.18 μm 1P6M CMOS	
Package and Die Area	32 pin TQFN, 2.2×2.2 mm^2	
Reference Frequency	12 MHz	
Output Frequency	2.4 – 2.5 GHz	
Measured Loop Bandwidth	> 730kHz	
Measured Current Consumption (at 1.8V)		
VCO and Divider Buffer	6.9 mA	20.9 mA
Divider	5.8 mA	
CP (with dynamic biasing), PFD and buffers	2.7 mA	
Digital	0.5 mA	
DAC	3.6 mA	
Calibration	1.4 mA	
Crystal Buffer	4.1 mA	9.4 mA
External Buffer	5.3 mA	
Measured Integer-*N* Performance		
Phase Noise @ 100 kHz	-104 dBc/Hz	
Phase Noise @ 3 MHz	-126 dBc/Hz	
Measured Performance, DAC and Calibration Technique Disabled		
Phase Noise @ 3 MHz	-91 dBc/Hz	
Fractional Spur @ 1 MHz	-40 dBc	
Fractional Spur @ 2 MHz	-42 dBc	
Fractional Spur @ ≥3 MHz	-45 dBc	
Measured Performance, DAC and Calibration Technique Enabled		
Phase Noise @ 100 kHz	-101 dBc/Hz	
Phase Noise @ 3 MHz	-124 dBc/Hz	
Fractional Spur @ 1 MHz	-47 dBc	
Fractional Spur @ 2 MHz	-57 dBc	
Fractional Spur @ ≥3 MHz	-62 dBc	
Reference Spur	-53 dBc	

TABLE II
COMPARISON OF PUBLISHED PHASE-NOISE CANCELING FRACTIONAL-N PLLS

	[1]	[2]	[3]	[5]	This Work
Output Frequency	2.1 GHz	2.4 GHz	3.6 GHz	1.8 GHz	2.4 GHz
Reference Frequency	35 MHz	48 MHz	50 MHz	14.33 MHz	12 MHz
Loop Bandwidth	700 kHz	460 kHz	1 MHz	400 kHz	730 kHz
Inband Phase Noise	-104 dBc/Hz	-96 dBc/Hz	-98 dBc/Hz	-98 dBc/Hz	-101 dBc/Hz
Phase Noise at 3MHz offset	-123 dBc/Hz	-121dBc/Hz	-120 dBc/Hz	-123 dBc/Hz	-124 dBc/Hz
Calibration Settling Time	No calibration	No calibration	No calibration	1 s	35 μs
Phase Noise Cancellation	15 dB	20 dB	29dB	30 dB	33 dB
Power Consumption	28 mW	67 mW	110 mW	29 mW	38 mW
Die Area	3.4 mm^2	6.5 mm^2	7.3 mm^2	2 mm^2	4.8 mm^2
Technology	0.18μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS

the phase noise or spurious performance change measurably. Therefore, all of the measured results described below were obtained with the dynamic charge pump bias technique enabled.

The IC was tested at 1 MHz frequency steps from 2.4 to 2.48 GHz. Table I summarizes the worst case performance of the IC over these frequencies with the adaptive phase noise cancellation technique enabled and disabled. The measured loop bandwidth was 730 kHz in all cases. The worst case spot phase noise with the adaptive phase noise cancellation technique enabled is −101 dBc/Hz and −124 dBc/Hz at 100 kHz and 3 MHz offsets, respectively, with no significant variation over the tested frequencies. Table II summarizes the performance of the PLL compared with relevant prior art.

Figs. 14 and 15 show representative PSD plots of the PLL's phase noise and output signal, respectively, for an output frequency of 2.423 GHz. Fig. 14 shows the phase noise with the DAC disabled, the DAC enabled without adaptive calibration, and the DAC enabled with adaptive calibration. The difference of 20 dB between the first two cases corresponds to the native cancellation path matching. Enabling the calibration technique

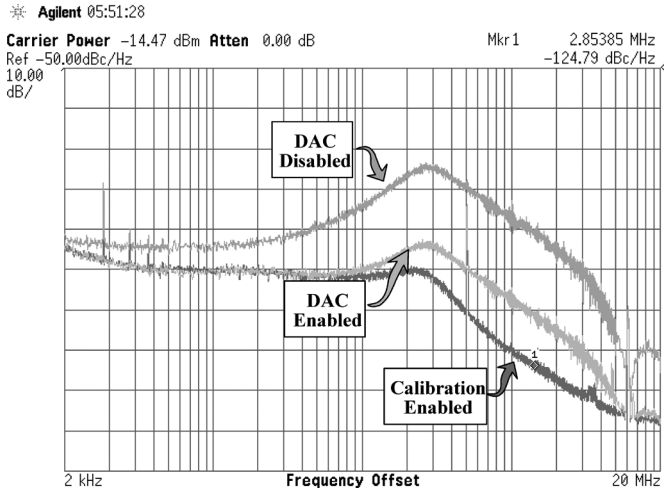

Fig. 14. Phase noise for an output frequency of 2.423 GHz.

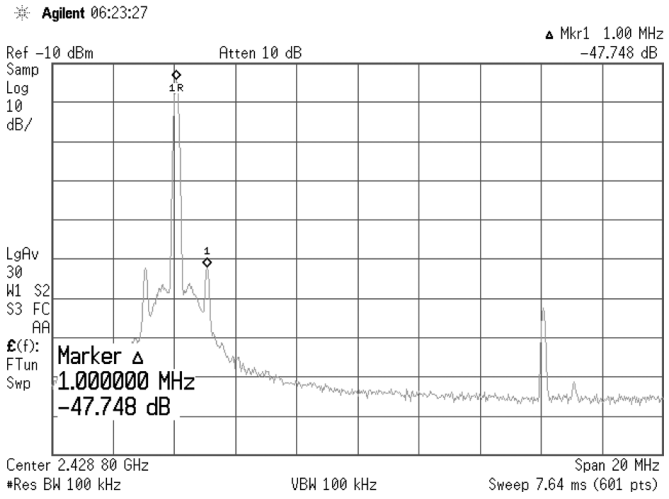

Fig. 15. Representative PLL output spectrum for an output frequency of 2.423 GHz.

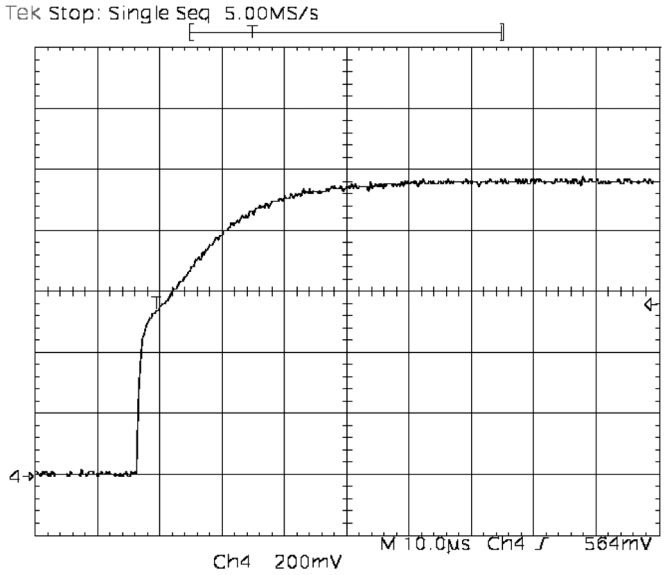

Fig. 16. Settling performance of the calibration loop.

further reduces the phase noise by 13 dB. The measured reduction in spot phase noise at a 3 MHz offset resulting from the phase noise cancellation with adaptive calibration enabled is 33 dB.

The worst-case fractional spur and reference spur have powers of −47 dBc and −53 dBc, respectively. Enabling and disabling the calibration technique does not measurably affect the power of the spurious tones. For the ISM-band frequencies at multiples of 1 MHz, the lowest-frequency fractional spurs are offset from the carrier by 1 MHz, and the largest such spur observed during measurement had a power of −47 dBc. With its loop bandwidth set to 730 kHz, the PLL provides 5 dB of attenuation at 1 MHz relative to its passband. Therefore, had the fractional spur fallen inside the PLL bandwidth, it would be expected to have a power of −42 dBc. This hypothesis was tested by setting the PLL to several frequencies other than multiples of 1 MHz in the ISM band to find the largest in-band fractional spur. The worst-case fractional spur thus found had a power of −39 dBc at a frequency offset of 250 kHz, which occurred for a PLL frequency of 2.43625 GHz. It is suspected that the 3 dB difference between the expected versus measured in-band fractional spur power for this worst-case situation is the result of coupling between the VCO output signal and a harmonic of the reference signal.

The output of the calibration loop's OTA optionally can be connected to an output pin through a MOS transistor switch for calibration settling time measurements. A representative waveform from this pin measured as the calibration loop settled is shown in Fig. 16 and indicates a settling time of 35 μs. Several such measurements were made for different PLL output frequencies. The results show that the settling time does not vary significantly as a function of the PLL's output frequency.

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