17.1 A Wide-Bandwidth 2.4GHz ISM-Band Fractional-N PLL with Adaptive Phase-Noise Cancellation

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Phase-noise cancellation makes it possible to greatly widen the loop bandwidth of a ΔΣ fractional-*N* PLL without the massive increase in phase noise that would otherwise be caused by the ΔΣ quantization noise [1-4]. This allows the loop filter to be integrated on-chip, reduces sensitivity of the VCO to pulling and noise, better attenuates in-band VCO noise, and makes direct digital frequency modulation practical in wireless applications such as GSM and Bluetooth. However, good phase-noise cancellation requires good matching of the cancellation signal paths, and the matching required for a given level of performance increases by 9dB each time the reference frequency is halved. To date, PLLs with phase-noise cancellation based on passive matching have required reference frequencies of 35MHz, 48MHz, and 50MHz to achieve 15dB, 20dB, and 29dB of phase-noise cancellation, respectively [1-3]. The need for such high reference frequencies represents a major limitation of phase-noise cancellation with passive matching in wireless applications.

An adaptive calibration technique that addresses this problem is presented in this paper and shown to enable 33dB of phase-noise cancellation in a PLL with a 12MHz reference frequency. A different adaptive calibration technique is presented in [4], but it's settling time is approximately 1s, which makes it impractical for many applications. In contrast, the calibration technique presented here settles within 35μs.

A byproduct of the ΔΣ modulation in a fractional-*N* PLL is that each charge pump output pulse contains an error term proportional to

$$e_{cp}[n] = \sum_{k=0}^{n-1} e_{\Delta\Sigma}[k],$$

where $e_{\Delta\Sigma}[n]$ is ΔΣ quantization noise. Rather than suppressing this term with a narrow-band loop filter as in a conventional fractional-*N* PLL, it can be cancelled as shown in Fig. 17.1.1 provided that the DAC gain is well matched to that of the charge pump.

A sign-error LMS algorithm can be used to adaptively match the gains [5]. A direct approach is to multiply a buffered copy of the loop filter voltage by

$$\mathrm{sgn}\{e_{cp}[n]\} = \begin{cases} 1, & \text{if } e_{cp}[n] \geq 0, \\ -1, & \text{if } e_{cp}[n] < 0, \end{cases}$$

and adjust the DAC gain with a lowpass filtered version of the result. Unfortunately, this is impractical unless very slow calibration settling can be tolerated, because the DC component of the loop filter voltage causes a large term proportional to $\mathrm{sgn}\{e_{cp}[n]\}$, which contains low-frequency noise and spurious tones, to appear in the LMS feedback loop. Unless the LMS loop bandwidth is made extremely low to suppress this term, the PLL phase noise is severely degraded [4].

This problem is avoided in this work via the split-loop filter design shown in Fig. 17.1.2. Two half-sized loop filters separately drive half-sized parallel varactors in the VCO and also drive a differential integrator in the LMS feedback loop. The two varactor capacitances add together in the VCO tank, so the VCO frequency depends on the common-mode (CM) loop filter voltage and is relatively insensitive to differential-mode (DM) voltage. In contrast, the differential integrator operates on the DM voltage from the two loop filters but rejects their CM voltage. Since the DM voltage is DC-free, the problem mentioned above is avoided. Multiplication by $\mathrm{sgn}\{e_{cp}[n]\}$ is achieved by sending the DAC and charge pump currents to the top loop filter whenever $\mathrm{sgn}\{e_{cp}[n]\} = 1$ and to the bottom loop filter whenever $\mathrm{sgn}\{e_{cp}[n]\} = -1$. Hence, the dynamics of the main PLL are determined by the CM half circuit whereas those of the LMS calibration loop are determined by the DM half circuit, both of which are shown in Fig. 17.1.3. Careful analysis and simulation indicate that both loops are stable even with high levels of DM-to-CM and CM-to-DM conversion.

Conceptually, the operation of the LMS calibration loop can be seen from the DM half circuit in Fig. 17.1.3. Whenever the DAC and charge pump are not perfectly matched, their sum contains a residual term proportional to $e_{cp}[n]$. Multiplication by $\mathrm{sgn}\{e_{cp}[n]\}$ causes this term to be proportional to $|e_{cp}[n]|$ if the DAC gain is too low, or $-|e_{cp}[n]|$ if the DAC gain is too high. This term gets filtered and integrated so the DAC gain is ramped up or down as necessary to cancel the error term.

The charge pump details are shown in Fig. 17.1.4. For low phase noise with such a wide loop bandwidth and low reference frequency, the charge pump and its bias circuitry require 2mA and 10mA of current, respectively, when powered up. However, the charge pump is on only for a small fraction of each reference period, so current is saved by powering up its bias circuitry only for 1/8 of each reference period just before the charge pump is turned on. This *dynamic biasing* reduces the average current consumption by 7.7mA. Charge pump linearization is achieved as described in [2] with two half-size charge pumps controlled by signals U, D, U_{ped}, and D_{ped} from a modified PFD.

The 10b DAC consists of a segmented tree-structured dynamic element matching (DEM) encoder and 26 weighted return-to-zero 1b DAC elements, each with an on-duration of 4 VCO periods. The DEM encoder is an extension of those presented in [2], [6], and [7] with 1b DAC weights of 1, 2, 4, 8, 16, and 32. Each 1b DAC is a resistively degenerated charge pump with large transistor sizes to reduce DAC element mismatches, and fast turn-off circuitry to minimize the injection of channel charge into the loop filter. The DAC circuitry is optimized for good inter-element matching whereas the charge pump is optimized for fast settling. The resultant poor matching between the DAC and charge pump is not a problem because of the adaptive calibration.

All other circuitry on the IC is relatively conventional. The VCO is a negative-g_m CMOS LC oscillator with a differential spiral inductor stacked in metal layers 5 and 6. Two equal MOS varactors provide tuning over a 0.6 to 1.2V range with a nominal K_{VCO} of 60MHz/V at each input. Coarse digital tuning is provided by switching MIM capacitors of 20fF and 80fF into the VCO tank. The divider consists of 7 pulse-swallowing divide-by-two stages as in [2]. Current-mode logic (CML) is used for the first two stages and standard CMOS logic is used for the remaining stages. The divider output is resynchronized to the output of the first CML stage to suppress modulus-dependent delays. The on-chip loop filter consists of two 5kΩ polysilicon resistors, two 18pF MiM capacitors, and two 282pF pMOS capacitors. Coarse digital tuning is provided to account for process variations. A folded-cascode single-stage OTA followed by a simple voltage-to-current converter is used in the LMS feedback loop. The output of the OTA optionally can be connected to an output pin through a MOS transistor switch for calibration settling time measurements. ESD protection circuitry is used on all pins.

The PLL's performance was tested across the 2.4GHz ISM band at 80 frequencies spaced by intervals of 1MHz. Figure 17.1.5 provides a summary of the worst-case measured performance over this range as well as the technology and package details. The performance does not appear to vary significantly from chip-to-chip, and is not sensitive to supply voltages between 1.5 and 2V. Figure 17.1.6 shows measured plots of the PLL output spectrum and its phase noise. A die micrograph is shown in Fig. 17.1.7.

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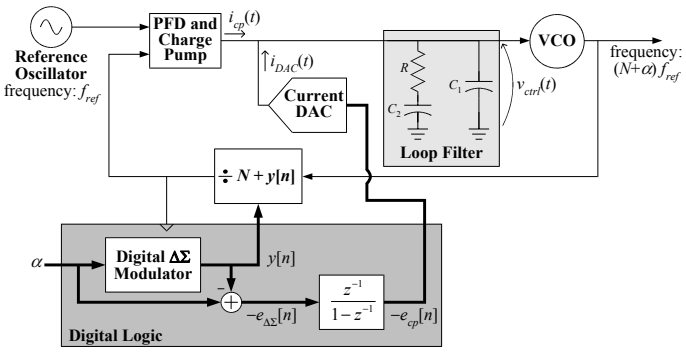

Figure 17.1.1: A generic fractional-*N* PLL with phase-noise cancellation.

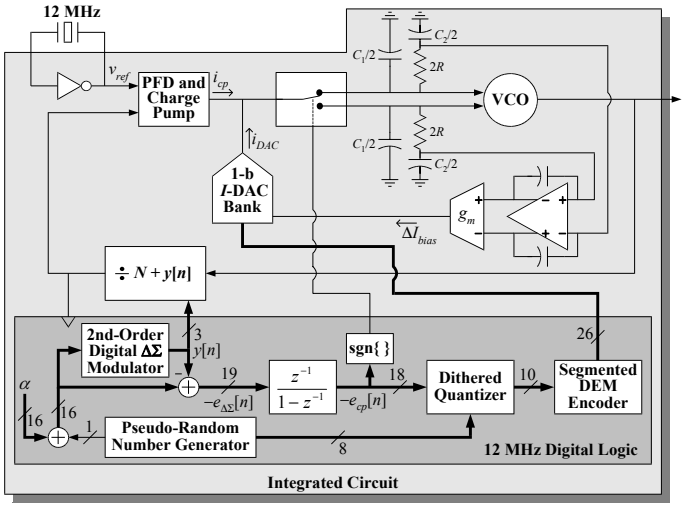

Figure 17.1.2: A high-level functional diagram of the integrated circuit.

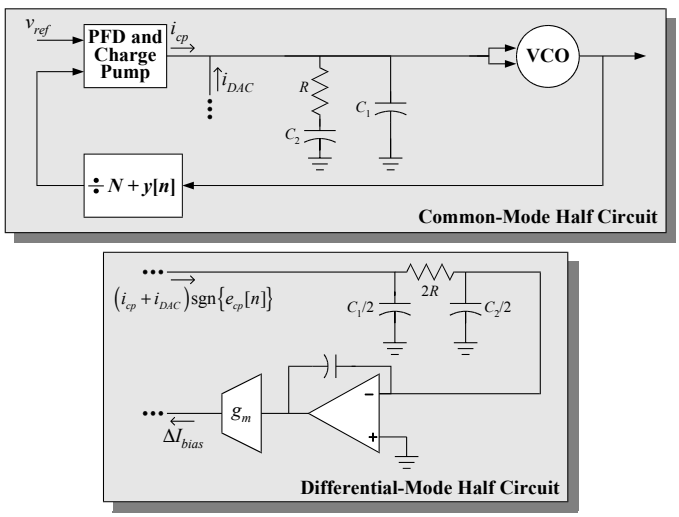

Figure 17.1.3: Half-circuit representations of the PLL and the LMS calibration loop.

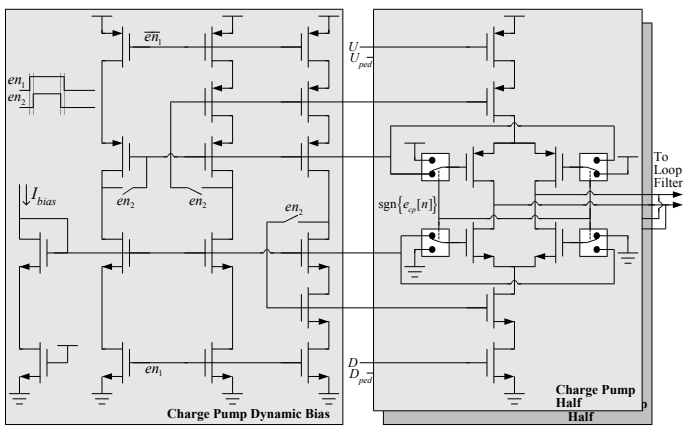

Figure 17.1.4: Charge pump and dynamic bias circuitry.

Design Details		
Technology	TSMC 0.18 µm 1P6M CMOS	
Package and Die Area	32 pin TQFN, 2.2 × 2.2 mm^2	
Reference Frequency	12 MHz	
Output Frequency	2.4 – 2.5 GHz	
Loop Bandwidth	> 730 kHz	
Measured Current Consumption (at 1.8V)		
VCO and Divider Buffer	6.9 mA	20.9 mA
Divider	5.8 mA	
CP (dynamic biasing enabled)	2.7 mA	
Digital	0.5 mA	
DAC	3.6 mA	
Calibration	1.4 mA	
Crystal Buffer	4.1 mA	9.4 mA
External Buffer	5.3 mA	
Measured Worst Case Integer-*N* Performance		
Phase Noise @ 100 kHz	−104 dBc/Hz	
Phase Noise @ 3 MHz	−126 dBc/Hz	
Reference Spur	−55 dBc	
Measured Worst Case Performance with DAC and Calibration Disabled		
Phase Noise @ 100 kHz	−88 dBc/Hz	
Phase Noise @ 3 MHz	−91 dBc/Hz	
Fractional Spur @ 1 MHz	−40 dBc	
Fractional Spur @ 2 MHz	−42 dBc	
Fractional Spur @ ≥3 MHz	−45 dBc	
Reference Spur	−52 dBc	
Measured Worst Case Performance with DAC and Calibration Enabled		
Phase Noise @ 100 kHz	−101 dBc/Hz	
Phase Noise @ 3 MHz	−124 dBc/Hz	
Fractional Spur @ 1 MHz	−47 dBc	
Fractional Spur @ 2 MHz	−57 dBc	
Fractional Spur @ ≥3 MHz	−62 dBc	
Reference Spur	−53 dBc	

Figure 17.1.5: Performance Table.

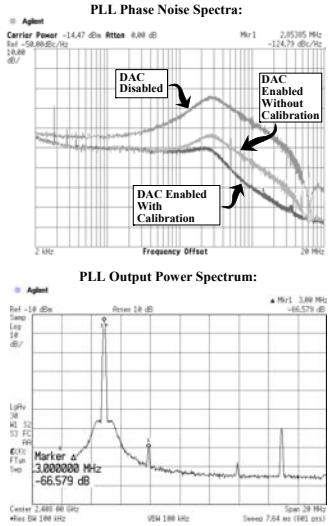

Figure 17.1.6: Representative measured PLL phase-noise plots and output power spectrum.

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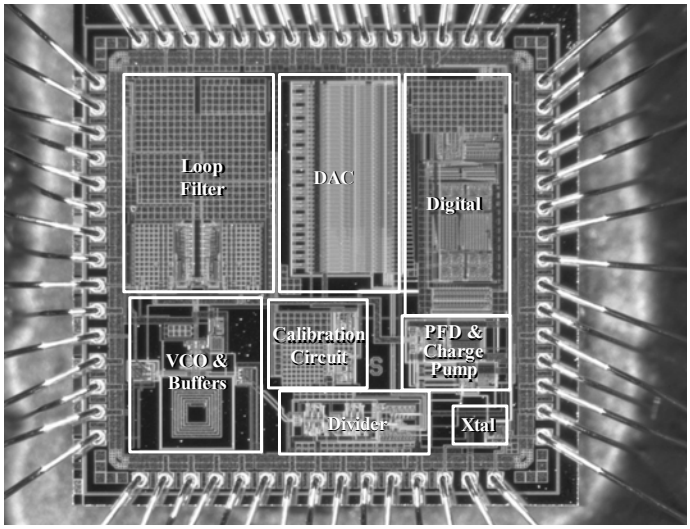

Figure 17.1.7: Die micrograph.

