Fractional-N Direct Digital Frequency Synthesis with a 1-Bit Output

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Abstract **— A novel digital frequency synthesis (DDS) architecture with a 1-bit output is proposed, simulated, and demonstrated. A new noise shaping quantization algorithm is also evaluated and used within the proposed DDS system. Large tuning ranges and rapid (open loop) response characteristics are achieved with only a static reference frequency input, without the use of analog components, allowing easy integration in digital CMOS processes. Across a tuning range of 10% f_{ref}, a noise floor of -80 dBc/Hz and spurious tones lower than -50 dBc are possible with this system.**

Index Terms **— Frequency synthesizers, Sigma-delta modulation, Quantization, CMOS digital integrated circuits.**

I. Introduction

Frequency synthesis is a pervasive requirement in wireless communication systems. Traditional frequency synthesis techniques include phased locked loops (PLL) and direct digital synthesizers (DDS), whose design is challenged by steadily increasing application requirements including high frequency output, large tuning range, small settling time, easy integration with digital systems, and simple implementation.

One of the issues with many current frequency synthesis techniques is the use of tuned analog circuitry or complicated high-resolution, high-speed digital-to-analog converters (DACs). Analog circuits can be difficult and inefficient to implement in many of today's digital IC processes. Today's systems need to be easily integrated into existing CMOS systems. Current efforts are underway to implement highly integrable frequency synthesizers [1].

The DDS method proposed here is simple to implement and consists entirely of digital circuitry making integration into existing systems-on-chips much easier. The present system is an open-loop based system, offering nearly instantaneous settling. Low settling time allows a designer to modulate the output signal by simply varying the input to the frequency synthesizer at the modulation rate. Today's wireless systems have steadily increasing data rates, demanding wider bandwidth modulation systems, often exceeding the settling time of closed-loop frequency synthesis systems.

The architecture discussed in this work, with its flexibility and integrability, has potential applications in software defined radio systems. The system's speed combined with large scale digital integration also would allow for generation of complex waveforms for phased array radar and instrumentation applications.

II. Fractional-N Direct Frequency Synthesis

The system proposed here to generate arbitrary frequencies comprises a reference frequency (f_{ref}) driving a programmable divide-by-N counter where the modulus, b[n], is supplied by a quantization system, see Fig. 1. In the simplest implementation, the output of the divide-by-N counter clocks in the next number in the b[n] sequence. Clocking the quantization system with the output of the frequency synthesizer alleviates the need for the phase accumulator and the phase-to-sinusoid lookup table. As a result of this clocking scheme, the synthesizer will only change frequencies at the zero crossings.

The system is similar to the existing feedback circuitry found in standard, closed-loop fractional-N phased locked loops (PLL's). Unlike the previous work, here the system is used outside of a feedback loop and more divider states are employed than in a typical closed-loop fractional-N PLL application.

Due to this DDS system's lack of phase noise suppression, in practice the output of the multi-modulus divider should be retimed with the reference clock to ensure low output jitter (not shown in Fig. 1).

During operation, the frequency selection word, inputted to the quantization system determines the output frequency (f_{out}). The tuning step of the system is only limited by the quantization system, and can be arbitrarily increased at the cost of complexity.

Inasmuch as the output only affects the clocking of the quantization system, the DDS system can be considered to be open-loop. Due the absence of settling time in open-loop systems, the output can be modulated rapidly with any constant envelope technique by rapidly varying the frequency selection word. Such systems eliminate the need for mixers, and allow the DDS to become a de facto transmitter, which can couple directly to a power amplifier and antenna for systems with constant envelope signals.

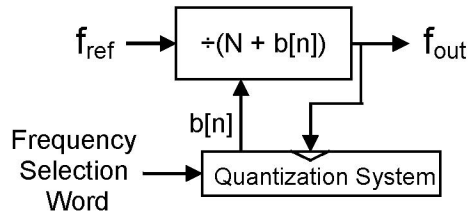

Fig. 1. Fractional-N Direct Frequency Synthesizer.

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The programmable multi-modulus divider only instantaneously generates outputs that are integer submultiples of the reference frequency. Frequencies that are non-integer submultiples of the reference frequency are generated by employing a quantization scheme. Typically the quantizer hops between the different integer submultiples in such a way that the outputs average to the desired frequency. Creating arbitrary values by hopping between integer values creates unwanted power, or quantization noise, as a side effect. This quantization noise needs to be shaped in the frequency domain to remove it from the vicinity of the desired tone and spread it evenly throughout the band to keep the in-band noise and spurs low.

Unfortunately, the amount of quantization noise generated by this system is a dynamic, signal-dependent value, inasmuch as the spacing between the quantized frequency values changes as a function of N and b[n]. For example, when N is 6, there is a much larger frequency difference between outputs when b[n] transitions between -2 to -3 than when it transitions from 1 to 0. For this reason, the quantization noise increases as a fraction of the total power as the synthesis system is tuned to higher frequencies. This effect is only pronounced when operating at high f_{outmax}- f_{outmin} to f_{ref} ratios.

When the system is tuning to frequencies greater than one-half of the Nyquist frequency, it is possible for outputs from the quantizer system to be greater than or equal to the N value of the divider. In this case, two choices can be made: 1) the out-of-range outputs can be limited, or 2) they can simply swallow previous pulses, i.e. when N=6 and b[n] = -7, one previous pulse would need to be swallowed. A sum of zero would just be dropped from the sequence. Limiting the values keeps clocking simple, but limits the upper range of the system. Allowing the out-of-range quantizer outputs to swallow adjacent pulses makes it possible for the output range to tune almost up to the Nyquist rate of the system.

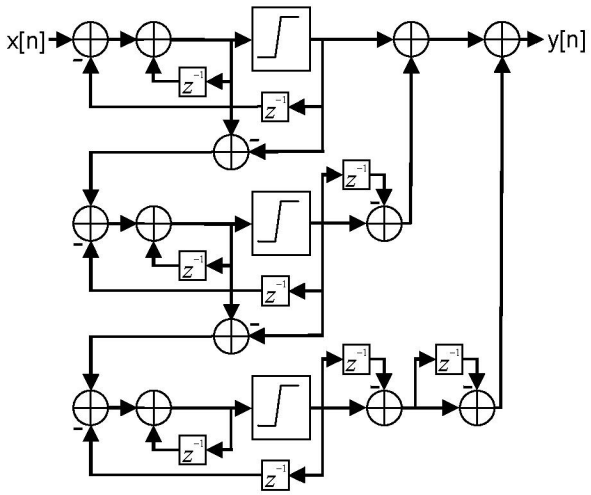

Fig. 2. MASH delta-sigma architecture.

Unfortunately, this complicates the clocking scheme because at higher rates, when many out-of-range outputs occur in a row, the quantization system needs to run at a different data-rate than the output of the multi-modulus divider.

These clocking issues can be solved by placing a buffer between the quantizer and the divider. The quantization system still must run at a higher frequency, but is no longer directly clocked by the output. A timing feedback method is necessary to keep the buffer from emptying or overflowing. For a given tuning range, this is a tradeoff between reference clock speed and system complexity.

In this work, two different quantization systems are demonstrated along with the aforementioned simple non-swallowing fractional division system: delta-sigma and segmented quantization. The performance of each system is simulated, and for the last system, it is also tested in a hardware demonstration for a more realistic verification of the simulated results.

III. Delta-Sigma Based Fractional-N Direct Frequency Synthesis

Here, a low-pass delta-sigma modulator selects the value of b[n] using the frequency selection word as the input. Many different variants of delta-sigma modulators exist; here a multi-stage noise-shaping (MASH) architecture is chosen because of its enhanced stability and lower sensitivity to idle tones with constant inputs [2]-[3].

The reference frequency (f_{ref}) was set at 6GHz. The MASH delta-sigma modulator was setup with three quantizers, and a word-length of sixteen bits. The eight possible output combinations of this MASH system were set to b[n] values of {-4, -3, -2, -1, 0, 1, 2, 3}. The N value was chosen as 7. The LSB of the first integrator has a one-bit dither signal injected to suppress tones.

The maximum and minimum frequency outputs of this delta-sigma based system are limited by the stable operating range of the MASH modulator. The system operates stably from 330 MHz to 425 MHz, see Fig. 3. The noise floor shape changes slightly over the band, but is no worse than -85

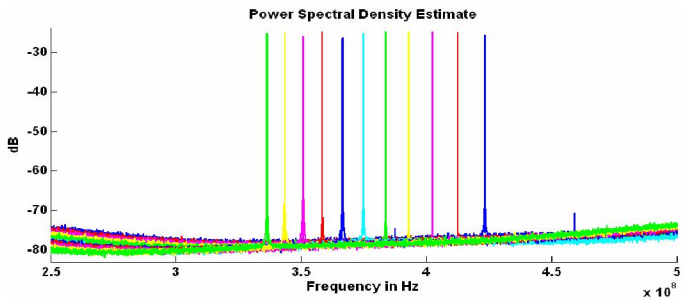

Fig. 3. MASH based frequency synthesizer maximum and minimum simulated outputs (32.3 kHz bin width).

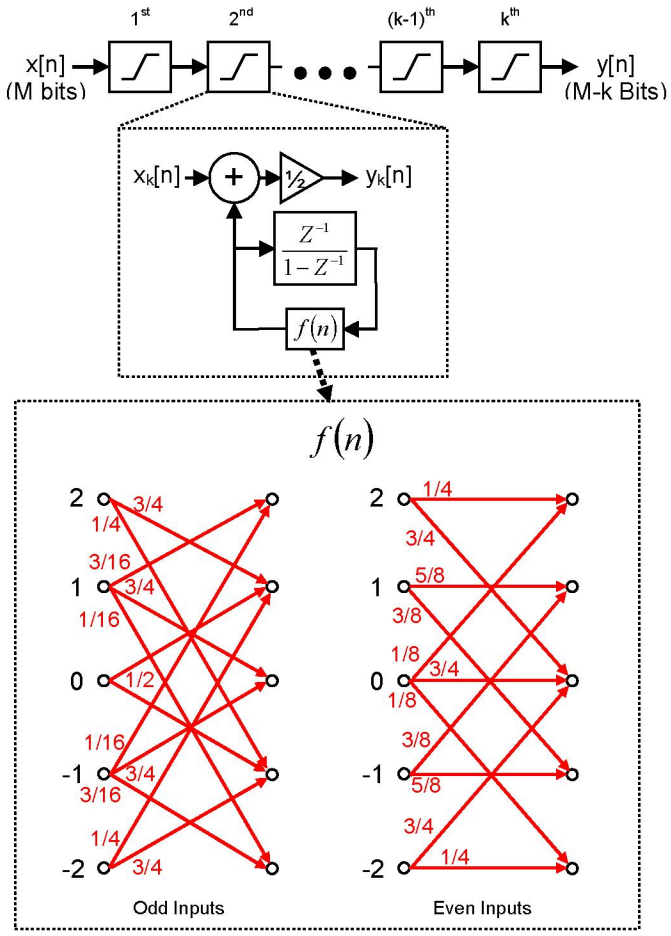

Fig. 4. First order noise shaping segmented quantization diagram. The state diagram of f(n) is detailed graphically on the right. The fractions denote the relative probability of the transition.

dBc/Hz. In-band spurious tones are observed at -50 dBc, as well as near-band spurs at -45 dBc.

The system tuning range here is limited by the stability of the delta sigma modulator, and spurs encroaching on the band-of-interest. Increasing the stability range is difficult, as stabilizing techniques tend to radically alter the noise shaping properties over the tuning range of the system. A quantization system that is stable over all inputs would allow for a much higher performance system.

IV. Segmented Quantization

Segmented quantization is a technique first introduced in [4] as a digital common-mode rejection technique for an analog-to-digital converter. It has been further extended as an improvement for more traditional fractional-N PLLs in [5].

In segmented quantization, the quantization operation is broken into steps, where each step reduces the number of states by a factor of two, see Fig. 4. Individual quantizers are added to form a cascade of quantizers until the desired level of overall quantization is reached.

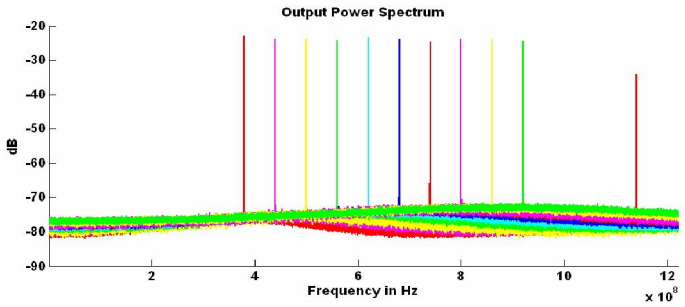

Fig. 5. Segmented quantization based frequency synthesizer simulated outputs (28.6 kHz bin width).

The individual quantizers work by adding a sequence of numbers to the input, f(n), in a way that always results in an even number (after which the least significant bit, a zero, can be discarded). The noise shaping in the frequency domain is achieved by bounding the cumulative sum of f(n).

The spreading of the quantization noise is achieved by using probabilistic state transitions in f(n). To avoid spurious tones, the expected value of the magnitude of the state transitions needs to be independent of the input and the modulator state. This also ensures the quantization noise is independent of the modulator's input history. Lastly, the expected value of the magnitude of the state transitions needs to be balanced, not only in the linear domain, but also for any nonlinearity in the system. Failing to compensate for nonlinearities will result in spurious tones being generated from the quantization noise passing through a nonlinear system.

Here we have a five state system, bounded by ±2. This results in a maximum output given by:

$$|Y_{\max}| \le \left[\frac{X_{\max}}{2^k} + \sum_{r=-1}^{k} \frac{1}{2^r} \right] \quad (1)$$

Advantages of this system include constant quantization noise; spur free operation (assuming a good source of random numbers is used); and stable operation over the entire input range of the system.

V. Segmented Quantization Based Fractional-N Direct Frequency Synthesizer

Here the segmented quantization system described above is demonstrated within the frequency synthesizer. The system was simulated with a reference frequency of 6 GHz, see Fig. 5. This particular addition sequence yields a frequency output of:

$$f_{out} = \frac{f_{clk}}{2\left[\frac{x_{in}}{2^k} + N\right]} \quad (2)$$

In this case, the tuning range is limited by the third harmonic encroaching on the band of interest on the low end, and the divider's smallest allowable value of b[n] on the high end (since this system cannot tolerate values of N + b[n] less than two). In this particular case, limiting the tuning range from 380 MHz to 960 MHz gives a simulated noise floor of -85 dBc/Hz and spurious performance of better than -60 dBc. For this frequency plan, all observed spurious tones occur out-of-band. To differentiate in simulation between quantization noise and spurs below -60 dBc across the entire band is very computationally intensive.

VII. Measurements

The above simulated system was tested in a hardware demonstration in order to verify performance. Signals generated in MATLAB were loaded into the 2^{23} bit pattern memory of an Agilent 71612C bit error rate tester (BERT). The signals were then played back at 6 Gbit/sec to verify that the signals can be generated, and ascertain the real world performance.

The measured results degraded slightly, see Fig. 6. The worst case noise floor was -80 dBc/Hz. There were no spurs distinguishable from the noise floor. Due to the open-loop nature of the system, jitter on the frequency reference of the system is not attenuated in magnitude by this frequency synthesis technique.

VIII. Conclusion

A novel frequency synthesis technique with a large tuning range and open loop tuning response has been proposed. The frequency synthesis system is well suited for wide bandwidth systems using constant-envelope modulations (or, with additional amplitude modulation methods, for arbitrary modulation formats). In these cases, employing this architecture can simplify the design of the transmitter, and ease integration with other digital systems, since this frequency synthesis system can be implemented entirely in digital logic. This system also eases the task of frequency band migration, since the same design can operate at different reference frequencies without any change.

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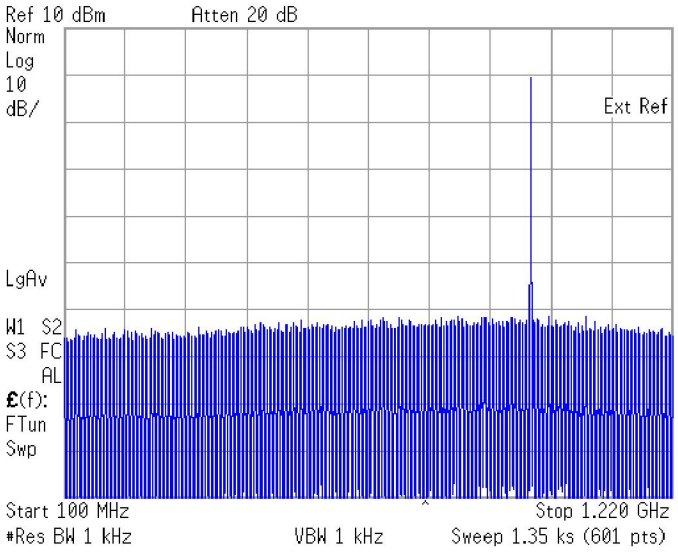

Fig. 6. Segmented quantization based frequency synthesizer measured output at f_{out} = 960 MHz.

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