Stochastic Analog-to-Digital Conversion

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***Abstract*—This paper suggests a stochastic approach to data conversion. It is applicable to serial, parallel, two-step as well as delta-sigma ADCs and DACs. In the serial implementation of this scheme, a sample-and-hold circuit, a noise source and a comparator are combined with an accumulate-and-dump digital stage to perform serial multibit A/D conversion. In the parallel ADC, *M* nominally identical primitive converter cells with the same input signal, *x(t)*, but with different and uncorrelated random dither signals, $d_i(t)$ *(i = 1, 2, ..., M)*, are combined to perform the data conversion. Possible combination of the two methodologies is also outlined.**

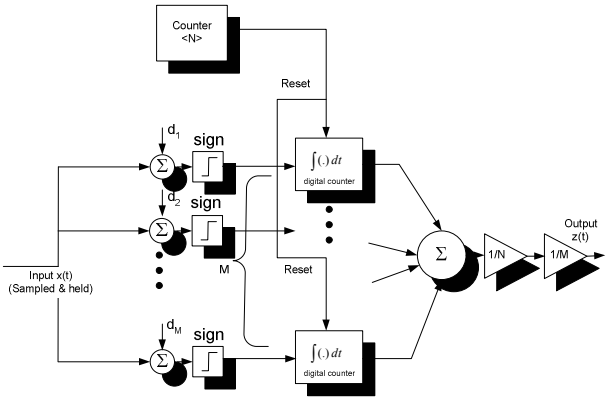
I. Introduction

In biological systems, often a large number of low-complexity unit cells combine to perform a fairly exact function. Applying this idea to the circuits and systems domain, we propose to use a set of coarse quantizers (i.e. 2- or 3-level comparators) combined to obtain robust and highly linear multibit analog-to-digital (ADC) [1], and digital-to-analog (DAC) converters.

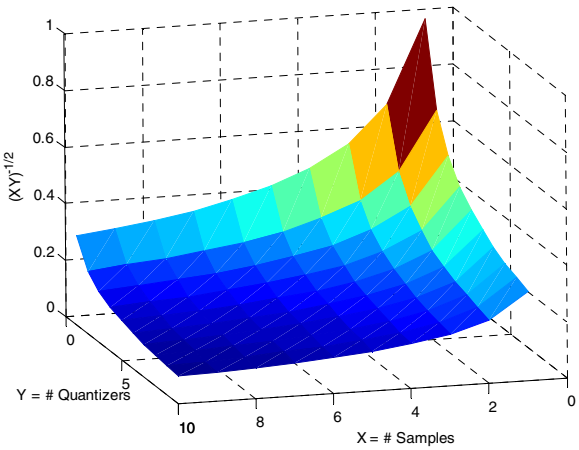
Figure 1 shows the generalized stochastic quantizer. It has *M* branches, each one containing a one-bit quantizer, an independent identically distributed (i.i.d.) random noise source (*di*) added with the sampled and held input signal, *x(t)*. Each digital output is followed with a digital integrator (up/down counter) controlled with a common modulo *N* counter. Those blocks will perform the accumulate and dump process (temporal averaging), while the parallel combination will provide a spatial averaging. Assuming the power of one individual quantizer to be q^2, after averaging *M* times spatially and *N* times temporally, the equivalent quantizer noise power at the output, q^2_{av}, will be:

$$q_{av}^2 \cong \frac{q^2 N M}{(N M)^2} \qquad (1)$$

Considering a linearized model, the output signal power will be equal to the input signal power, which means an increase in the signal to noise ratio (SNR) equal to *N.M*, or in other words, a reduction of the quantization noise power by the same factor.



(a)



(b)

Figure 1: a) Time-Spatial averaging quantizer. The noise sources are uncorrelated and i.i.d. The integrators are up/down counters. Scaling factors are at the output. b) RMS noise as a function of the number of samples and the number of parallel branches.

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The noise will decrease as the number of quantizer branches or the modulo of the counter increases, as depicted in Fig. 1-b. The tradeoffs depend on speed and power/area relations. It should be noted that for a given complexity, the maximum reduction of quantization noise is achieved when $N = M$.

II. Spatial Averaging – Analyis

In the rest of the paper, we shall discuss only the spatial averaging idea (i.e., the counters will be disregarded in the mathematical development that follows). First, the application will be presented for an open loop configuration, but after that the emphasis will be put on delta sigma modulators.

Based on the scheme of Fig. 1, and assuming no time averaging (N=1), the overall system becomes a parallel combination of M one-bit quantizer branches [1]. It should be pointed out that the simple *sign(x)* quantizer could be replaced with a 3-level (1.5 bit) quantizer, obtaining improved performance. Also, different pdfs (probability density functions) can be used to generate the random dithering and uncorrelating noise sources. The general case will be discussed next.

Assuming a linear operation over a continuous random variable (r.v.) d, with pdf $f_d(d)$:

$$y = x + a\,d \tag{2}$$

where a and x are constants[1], then the pdf of the new r.v. y is given by [2]

$$f_y(y) = \frac{1}{|a|} f_d\left(\frac{y-x}{a}\right) \tag{3}$$

Without loss of generality, considering a=1, it is known that $f_y(y)$ will be the convolution of $f_d(d)$ with a Dirac's delta centered at x, i.e, the new pdf will be equal to the original one but shifted.
On the other hand, the overall system output is given by

$$z = \frac{1}{M}\sum_{i=0}^{M-1}\text{sign}(x+d_i) = \frac{1}{M}\sum_{i=0}^{M-1}\text{sign}(y_i) \tag{4}$$

For large M, and using the law of large numbers, z tends to:

$$z \cong \overline{\text{sign}(x+d_i)} = \overline{\text{sign}(y_i)} = \overline{w};\ \ w = \text{sign}(y_i) \tag{5}$$

The mean value, or first moment, of a r.v. is defined as

$$\overline{w} \equiv \int_{-\infty}^{\infty} w\, f_w(w)\, dw \tag{6}$$

Using the sign(*arg*) definition (+1 if *arg* ≥ 0, -1 otherwise), combined with the previous formulas [4],

$$\begin{aligned}\overline{w} \equiv &-\int_{-\infty}^{0} f_y(y)\, dw + \int_{0}^{\infty} f_y(y)\, dw = \\ &-\int_{-\infty}^{0} f_d(y-x)\, dy + \int_{0}^{\infty} f_d(y-x)\, dy = \\ &-\int_{-\infty}^{-x} f_d(\alpha)\, d\alpha + \int_{-x}^{\infty} f_d(\alpha)\, d\alpha\end{aligned} \tag{7}$$

results.

From (7), it can be easily inferred that for a uniform distribution, the output is linearly related to the input. For other kind of distributions, look-up tables may be used to optimize the use of the quantizers.

III. Sigma Delta Modulators Using the Spatial Quantizer

The first design to be presented is a delta sigma ADC, schematically depicted in Fig. 2-a. In this case, to avoid excessive delays, the fast feedback toward the input addition point is made individually from each comparator. The addition in the digital domain is performed out of the loop, where delays can be tolerated. The system was simulated using realistic models for the opamps (offsets in the order of +/-5mV, DC gains of 70~80dB, plus nonlinear characteristics were implemented in Simulink®). The FFT output for a second order system using 16 3-level comparators is shown in Fig. 2-b, together with the results obtained using a conventional 3-bit second order sigma delta sigma ADC. It should be noted that the shape of the pdf in this case is of no importance (the high loop gain tends to linearize the nonlinear quantizer characteristic). Moreover, offsets are tolerated.

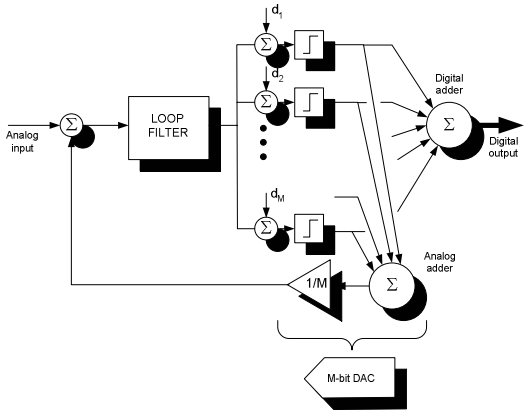
For this example, the improvement in the signal-to-noise ratio (SNR) is evident using (1). The output V of the system for any bandlimited input U is then given by

$$V = STF\,U + NTF\left(q/\sqrt{\text{M}}\right) = U + \left(1-z^{-1}\right)^2\left(q/\sqrt{\text{M}}\right) \tag{8}$$

Here STF and NTF stand for the signal- and for the noise-transfer functions, respectively, and q is the quantization noise of a 3-level quantizer [3].

A first modification could be to use, instead of a simple 3-level quantizer, a first order delta sigma modulator for each branch. Figure 3 shows the system together with its simulation results. Again, nonideal effects were taken

[1] *Here, x* is the sampled input value.



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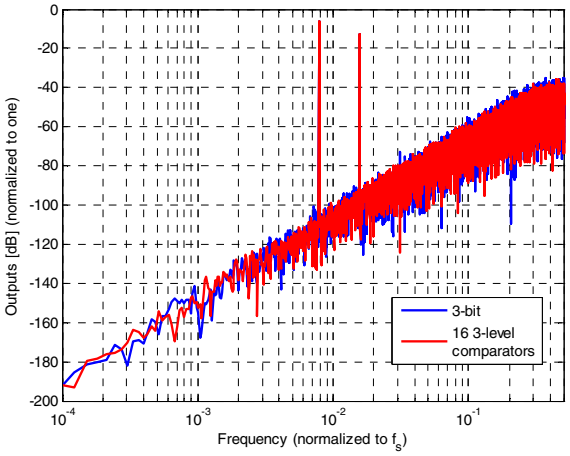
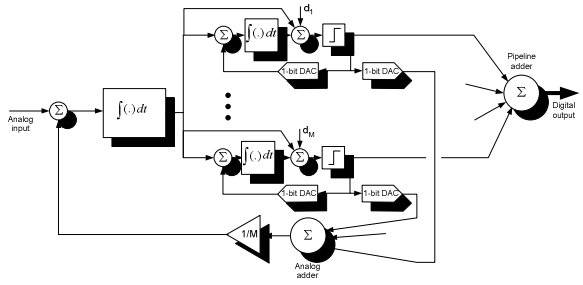


(b)

Figure 2: Delta sigma ADC using spatial averaging. a) Simplified schematic. b) Frequency response for a second order system using a 3-bit conventional quantizer, and using a 16 1.5-bit spatial quantizer. Two tones (-6dB$_{FS}$ and -12dB$_{FS}$) used to observe nonlinear behavior.

into account (9 bit matching for all the components, offset and nonlinear Opamps, etc.). It is noteworthy in this case that because each element has a one-bit first order shaping, the overall response is highly linear (compare with the intermodulation tones in the 3-bit delta sigma modulator, with a 9-bits linear feedback DAC). For comparison purposes, the response of a one bit ADC is also shown. As a conclusion, an improvement in linearity is obtained without the use of DWA or any other mismatch shaping technique in the DAC.

As a corollary, because of the linearity obtained, it is now possible to extend the concepts to a delta sigma DAC structure, as depicted in Fig. 4-a. The first step is to simplify the digital structures; hence, a first delta sigma ($\Delta\Sigma_A$) is used to reduce the digital input word length. The dithering sources can be quantized and easily generated on-chip by means of pseudo random noise generators implemented with linear feedback shift registers (LFSR). The simulated response is shown in Fig. 4-b, together with a 3-bit and a one-bit systems



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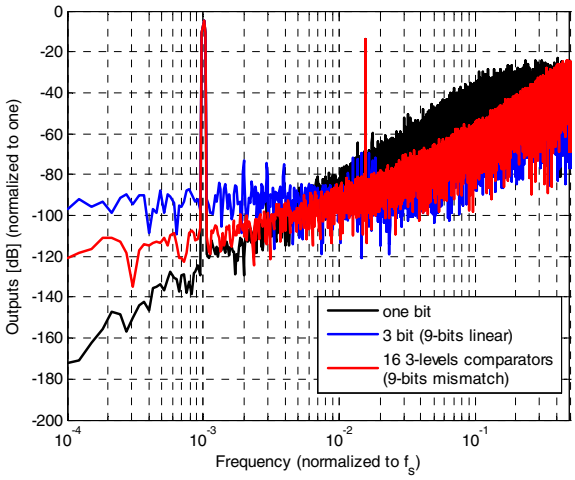

(b)

Figure 3: Delta sigma ADC using spatial averaging with embedded noise shaping. a) Simplified schematic. Two sets of 1-bit DACs are used to simulate a real system. b) Frequency response for a second order system using a 3-bit conventional quantizer, using 16 1.5-bit spatial quantizers, and using a one-bit quantizer delta sigma. Two tones (-4.5dB$_{FS}$ and -14dB$_{FS}$) used to observe nonlinear behavior. All elements are 9 bits linear.

for comparative purposes. Also, the integrated noise powers are plotted for the three different cases. Important points: error feedback can be used (resulting in reduced area and power consumption); no stability problems as long as each equal individual one-bit branch is stable (possibilities of high order noise shaping); current sources can be used (high speed developments)

IV. Conclusions

Analog-to-digital and digital-to-analog converters have been presented, which use coarse quantizers in order to get multibit responses. The idea behind this procedure can be explained as follows: under certain assumptions the quantization noise can be considered as a wide sense stationary stochastic process (generally considered uniformly distributed and with zero mean), with ergodicity in its mean and variance values (i.e., similar time and spatial statistical properties). Based on this fact, assuming zero correlation among all the individual outputs and successive samples, and using the law of the large numbers, we have concluded the previous results for a large number of comparators with large dithering sources.

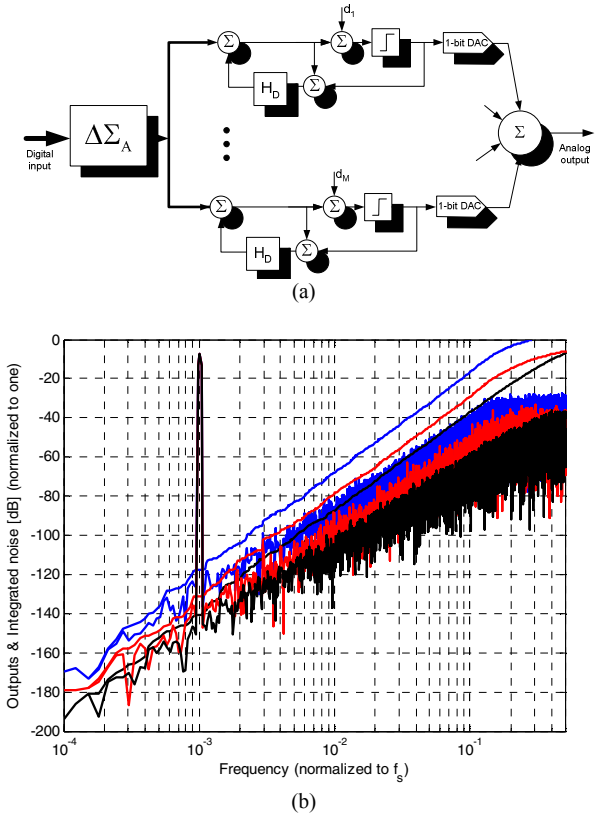

Figure 4: Delta sigma DAC using spatial averaging with embedded noise shaping. a) Simplified schematic. Analog elements have 9 bits matching. Noise sources quantized to 3 levels. b) Frequency response for a second order system using a 3-bit conventional quantizer (black), using 16 1.5-bit spatial quantizers (red), and using a one-bit quantizer delta sigma (blue). Tone at -7dB$_{FS}$. Also shown are the integrated noise powers for the three cases.

Both time and space constrains were taken into account, e.g., for the spatial ADC case, a $\log_2(M)$ bits length word is obtained as the output of the system, but with an equivalent quantization error of $\log_2(M^{1/2})$. The tradeoff is clear: *accuracy vs. time and/or area & power*.

On the other hand, an interesting and promising fact emerged from this research: highly linear devices can be devised using imperfect components.

As it was already mentioned, all the one-bit inputs/outputs must be uncorrelated among themselves. The use of M noise sources at the inputs of the M comparators not only achieves this result, but also dithers the quantization noises, helping the loop filters to shape their power spectral densities (PSD). Generating the noise in digital domain is an easy matter, something that is not so trivial in the analog domain.

As a result, circuit robustness is obtained, which comes from the fact that there is no need of accurate voltage dividers to get the quantizer reference chain. Another extra advantage is that if one comparator (or a reduced amount of them) fails, the system will still be functional, with a little degradation on its characteristics

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