A Digitally Enhanced 1.8-V 15-bit 40-MSample/s CMOS Pipelined ADC

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***Abstract*—A 1.8-V 15-bit 40-MSample/s CMOS pipelined analog-to-digital converter with 90-dB spurious-free dynamic range (SFDR) and 72-dB peak signal-to-noise ratio (SNR) over the full Nyquist band is presented. Its differential and integral nonlinearities are 0.25 LSB and 1.5 LSB, respectively, and its power consumption is 400 mW. This performance is enabled by digital background calibration of internal digital-to-analog converter (DAC) noise and interstage gain errors. The calibration achieves improvements of better than 12 dB in signal-to-noise plus distortion ratio and 20 dB in SFDR relative to the case where calibration is disabled. Other enabling features of the prototype integrated circuit (IC) include a low-latency, segmented, dynamic element-matching DAC, distributed passive input signal sampling, and asymmetric clocking to maximize the time available for the first-stage residue amplifier to settle. The IC is realized in a 0.18-μm mixed-signal CMOS process and has a die size of 4 mm $\times$ 5 mm.**

***Index Terms*—Analog-to-digital conversion, calibration, mixed analog–digital integrated circuits (ICs).**

I. Introduction

THE trends toward increased digital signal processing and tighter integration in communications and imaging systems have created a need for high-resolution low-voltage analog-to-digital converters (ADCs) with sample rates above 20 MHz. Pipelined ADCs (PADCs) are well suited to such applications but are highly sensitive to nonlinearity introduced by their internal digital-to-analog converters (DACs) and interstage gain errors. Without some form of trimming or calibration, these limitations make it difficult to implement conventional PADCs with an effective number of bits greater than 11 in present VLSI technology, especially at low supply voltages.

This paper presents a 1.8-V 15-bit 40-MSample/s CMOS PADC prototype integrated circuit (IC) in which these problems are addressed by two digital background calibration techniques: the DAC noise cancellation (DNC) technique proposed in [1] and the gain error correction (GEC) technique proposed in [2]. Together these techniques enable the prototype PADC to achieve 90-dB spurious-free dynamic range (SFDR) and 72-dB peak signal-to-noise ratio (SNR) over the full Nyquist band, a differential nonlinearity (DNL) of 0.25 LSB, an integral nonlinearity (INL) of 1.5 LSB, and a power consumption of 400 mW [3]. Other features of the PADC that helped facilitate implementation of the calibration techniques and achieve the necessary underlying performance prior to calibration include a low-latency segmented dynamic element-matching DAC, distributed passive input signal sampling, and asymmetric clocking to maximize the time available for the first-stage residue amplifier to settle.

The DNC and GEC techniques are applied to a conventional PADC topology. The DNC technique digitally estimates and corrects for DAC nonlinearity within the PADC. It is completely digital in that it is implemented by adding only digital circuitry to a conventional PADC. The GEC technique digitally estimates and corrects for interstage gain errors. It is mostly digital in that it requires a small amount of noncritical analog circuitry relative to a conventional PADC. Both techniques operate in the background, i.e., they operate continuously during normal operation of the PADC without the need for an auto-calibration cycle. Although the techniques complement each other, they are independent and each can be applied in the absence of the other. In addition to improving performance, the techniques relax circuit and layout requirements, thereby reducing overall design and layout time.

The DNC and GEC techniques compare favorably to other calibration techniques that have been proposed previously. Most such techniques either operate in the foreground, thereby disrupting normal ADC operation [4]–[7], require additional stages [8], [9], require extra clock phases [10]–[12], reduce the usable input bandwidth [4], [13], only improve DNL [14], improve SFDR but not SNDR [15], or increase analog complexity [16]. A slight extension of the DNC technique was recently proposed to correct for both DAC nonlinearity and interstage gain errors simultaneously, but, unlike the GEC technique, it only corrects for interstage gain errors resulting from capacitor mismatches [17]. Various techniques have been presented that are related to the GEC technique. An earlier technique that operates on a similar principle to the GEC technique but requires significantly more analog circuitry is presented in [18]. More recently, three variations of the GEC technique have been proposed [19]–[21]. The technique presented in [19] reduces convergence time at the expense of an increase in analog and digital circuitry. The technique presented in [20], although similar to the GEC technique, increases the required output voltage range of the residue amplifiers and has a much longer convergence time. The technique presented in [21] has the advantage that it is an all-digital technique, but the disadvantage that its convergence relies on the error introduced by the flash ADC within the first pipeline stage resulting from comparator offsets and resistor ladder errors.

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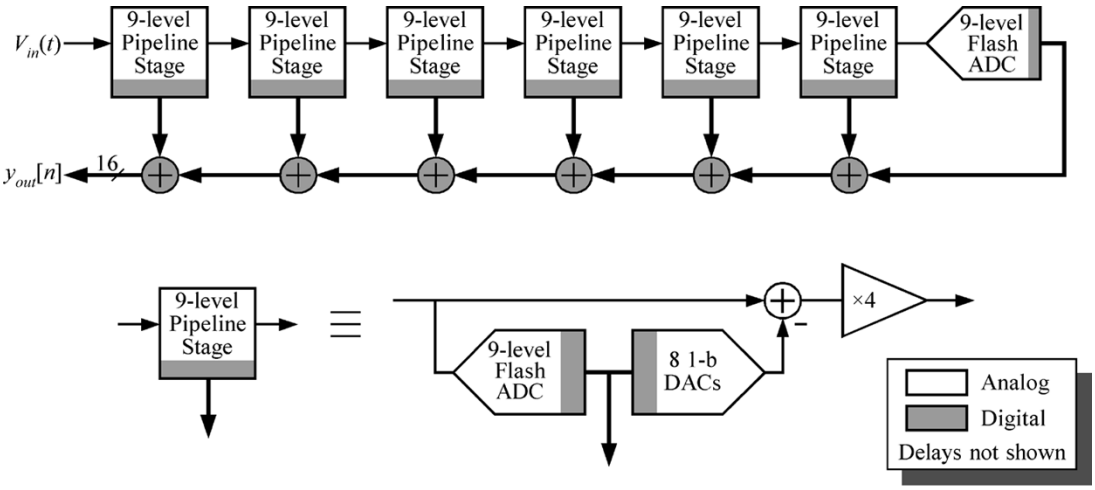

Fig. 1. Conventional PADC example.

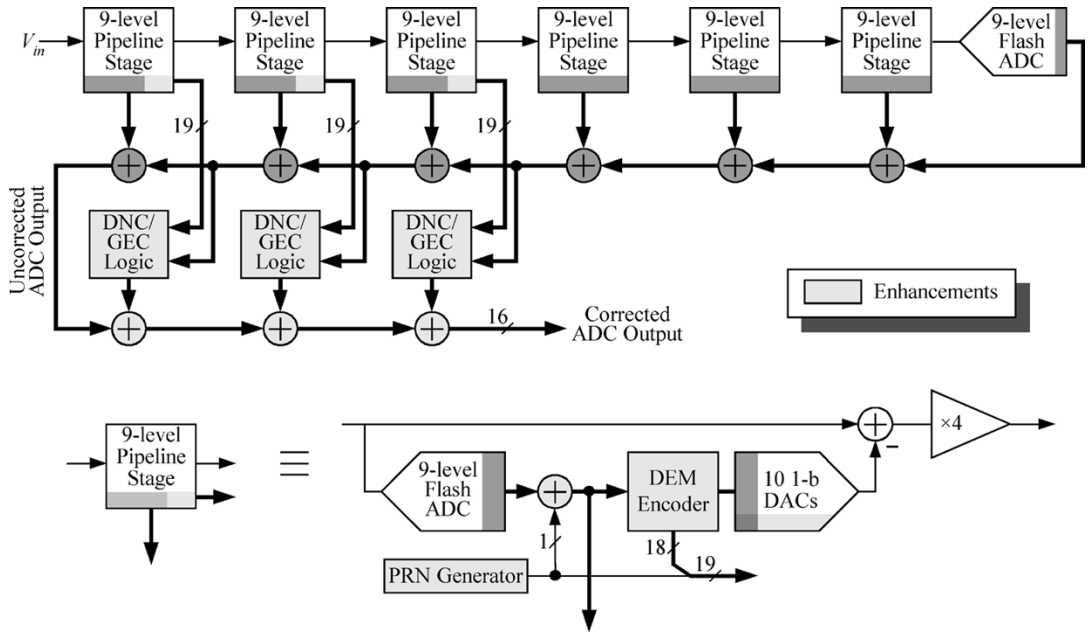

Fig. 2. Digitally enhanced PADC prototype.

II. System-Level Design Details

A. Underlying Conventional Pipelined ADC

The prototype PADC consists of an underlying conventional PADC with additional blocks to implement DNC and GEC. A high-level diagram of the underlying conventional PADC is shown in Fig. 1. It consists of seven stages, each of which resolves slightly more than 3 bits (nine instead of eight levels). As shown in the figure, each stage uses a nine-level flash ADC to digitize its input signal. In all but the last stage, a nine-level DAC, comprised of eight parallel 1-bit DACs, converts the ADC output into a nine-level analog value which is subtracted from the stage's input signal. The result is amplified by a *residue amplifier* with an *interstage gain* of 4 to generate the *residue* which is the input to the subsequent pipeline stage. The nine-level digital outputs of each stage are combined with appropriate weighting factors and delays to generate the overall PADC output. It can be verified that the ideal dynamic range of the PADC is slightly more than 15 bits.

In the absence of nonideal circuit behavior, the quantization step size of the flash ADC in each stage is 1/9th of the maximum allowed input range of the stage, so the voltage range of the corresponding residue is 4/9th of the maximum allowed input range of the stage. Therefore, in the absence of nonideal circuit behavior, 5/9th of the input range in each of the second through seventh stages is never used. However, in practice, comparator offset voltages and resistor ladder deviations cause the flash ADCs to introduce additional errors that use some of the extra range. Fortunately, provided that the error does not cause this extra range to be exceeded, it gets cancelled in the pipeline up to the accuracies of the interstage gains and nine-level DACs [22]. This well-known principle of pipelined ADCs is referred to as *redundancy*, and, as explained below, is exploited by the GEC technique.

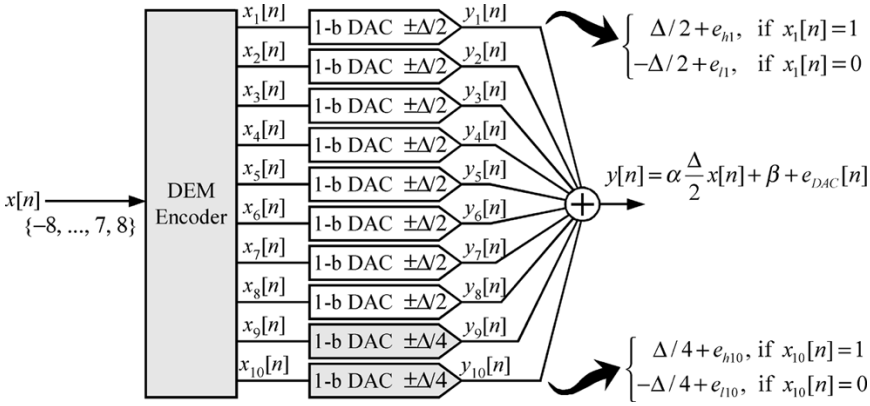

Fig. 3. DEM DAC.

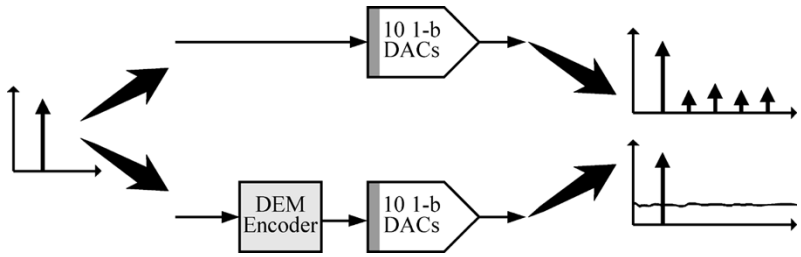

Fig. 4. Effect of DEM on the output spectrum when mismatches are present.

B. Pipelined ADC System Overview

A high-level diagram of the implemented prototype PADC is shown in Fig. 2. Enhancements to the conventional architecture of Fig. 1 are indicated in the figure. The correction algorithms are only applied to the first three stages, because errors in the remaining stages are negligible when referred back to the PADC input. As shown in the figure, each correction stage differs from a conventional PADC stage in three respects: 1) a 1-bit pseudorandom number (PN) sequence is added to the output of the flash ADC; 2) a dynamic element-matching (DEM) encoder precedes the bank of 1-bit DACs; and 3) two extra 1-bit DACs are added to the original bank of eight 1-bit DACs to accommodate the added PN sequence. To minimize latency, the PN sequence adder and DEM encoder are implemented together, as will be described in Section III.

C. Dynamic Element-Matching DAC

A high-level block diagram of each DEM DAC is shown in Fig. 3. The eight 1-bit DAC elements of the underlying conventional PADC have a step size of Δ, and the two additional elements have a step size of $\Delta/2$, where Δ is the step size of the corresponding stage's flash ADC. The outputs of the 1-bit DACs are given by

$$y_i[n] = \begin{cases} \frac{\Delta}{2} + e_{\rm hi}, & \text{if } x_i[n] = 1 \\ \frac{-\Delta}{2} + e_{\rm li}, & \text{if } x_i[n] = 0 \end{cases} \qquad i = 1, 2, \ldots, 8 \quad (1)$$

and

$$y_i[n] = \begin{cases} \frac{\Delta}{4} + e_{\rm hi}, & \text{if } x_i[n] = 1 \\ \frac{-\Delta}{4} + e_{\rm li}, & \text{if } x_i[n] = 0 \end{cases} \qquad i = 9, 10 \quad (2)$$

where $e_{\rm hi}$ and $e_{\rm li}$ are high-level and low-level output errors, respectively, resulting from nonideal circuit behavior. In typical switched-capacitor implementations, mismatches among nominally identical unit capacitors incurred during fabrication are the dominant source nonideal circuit behavior, and such mismatches do not change appreciably over time. Thus, $e_{\rm hi}$ and $e_{\rm li}$ are assumed to be time-invariant and are referred to as *mismatch errors*.

The DEM encoder consists of digital circuitry that sets bits $x_1[n], \ldots, x_{10}[n]$ such that, in the absence of mismatch errors, the output of the DAC would be $y[n] = 1/2\Delta x[n]$. However, mismatch errors cause the output of the DAC to be

$$y[n] = \alpha \frac{\Delta}{2} x[n] + \beta + e_{\rm DAC}[n] \quad (3)$$

where α is a constant gain, β is a constant offset, and $e_{\rm DAC}[n]$ is the DAC noise [1]. Thus, mismatch errors cause α, β, and $e_{\rm DAC}[n]$ to deviate from their ideal values of 1, 0, and 0, respectively.

In a conventional PADC, each 1-bit DAC element is controlled directly by the flash ADC. In the presence of mismatch errors, this deterministic control results in nonlinear distortion, as illustrated in Fig. 4. In this case, the DAC output has the form of (3) where $e_{\rm DAC}[n]$ is a deterministic function of $x[n]$.

The DEM encoder exploits flexibility in choosing its output values to decorrelate $e_{\rm DAC}[n]$ from the DAC's input sequence. For most DAC input values, $x[n]$, there are multiple ways to choose the bits $x_1[n], \ldots, x_{10}[n]$ to achieve the same DAC output value in the absence of mismatch errors. However, mismatch errors cause these nominally identical DAC output values to differ from each other. For example, Fig. 5 shows three

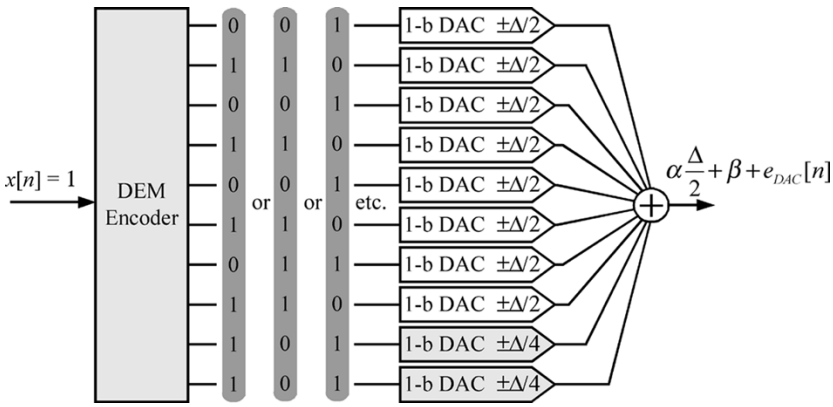

Fig. 5. DEM example.

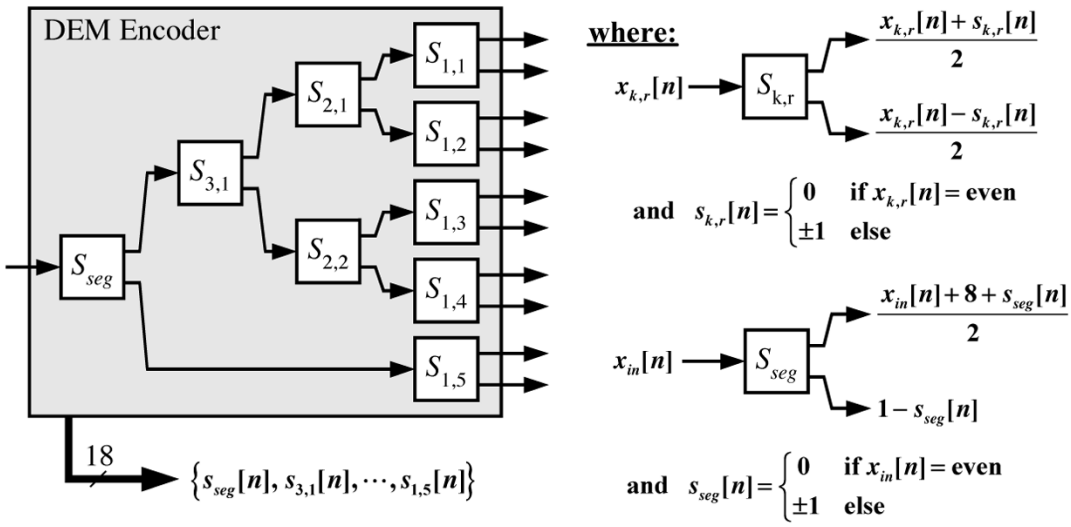

Fig. 6. Details of the DEM encoder.

choices of $x_1[n], \ldots, x_{10}[n]$ (out of a larger valid set) corresponding to $x[n] = 1$ that would each result in the same output, i.e., $y[n] = \Delta/2$, if there were no mismatch errors. However, mismatch errors cause these nominally identical outputs to differ because the different choices of $x_1[n], \ldots, x_{10}[n]$ cause different combinations of the 1-bit DACs to be high or low. Each sample period, the DEM encoder pseudorandomly selects one of the valid choices for $x_1[n], \ldots, x_{10}[n]$ corresponding to the present DAC input, $x[n]$. It can be shown that the resulting DAC noise is white and uncorrelated with $x[n]$ [1].

Therefore, DEM improves the SFDR of a PADC because it converts harmonic distortion into white noise and causes it to be uncorrelated with the other signals in the PADC. However, the DAC noise increases the overall noise floor of the PADC, so SFDR is improved at the expense of SNR [15], [23]. Fortunately, the DEM encoder causes the noise to have a predictable structure. The DNC technique improves the SNR by exploiting this structure to estimate the DAC noise and remove it from the PADC output.

Each of the correction stages in the prototype IC uses the partially segmented tree-structured DEM digital encoder shown in Fig. 6 [24], [25]. The encoder consists of nine *switching blocks*, labeled S_{seg} and $S_{k,r}$, where $k \in \{1, 2, 3\}$ and $r \in \{1, 2, 3, 4, 5\}$. Each switching block generates a corresponding *switching sequence* defined as

$$s_{\text{seg}}[n] = \begin{cases} 0, & \text{if } x_{in}[n] = \text{even} \\ \pm 1, & \text{else} \end{cases}$$
$$s_{k,r}[n] = \begin{cases} 0, & \text{if } x_{k,r}[n] = \text{even} \\ \pm 1, & \text{else} \end{cases} \quad (4)$$

where $x_{in}[n]$ and $x_{k,r}[n]$ are the switching block inputs. The choice of $+1$ or -1 when the switching block input is odd is made by a bit sequence from a pseudorandom number generator. Each pseudorandom sequence is designed to well approximate a white zero-mean random process that is uncorrelated with all other signals in the PADC. These statistical properties are inherited by the switching sequences by virtue of their definition in (4).

The DAC input, $x_{in}[n]$, can be viewed as an integer in the range -8 to 8. At each sample time n, the top and bottom outputs of switching block S_{seg} are set to $(x_{in}[n] + 8 + s_{\text{seg}}[n])/2$ and $1 - s_{\text{seg}}[n]$, respectively, and the top and bottom outputs

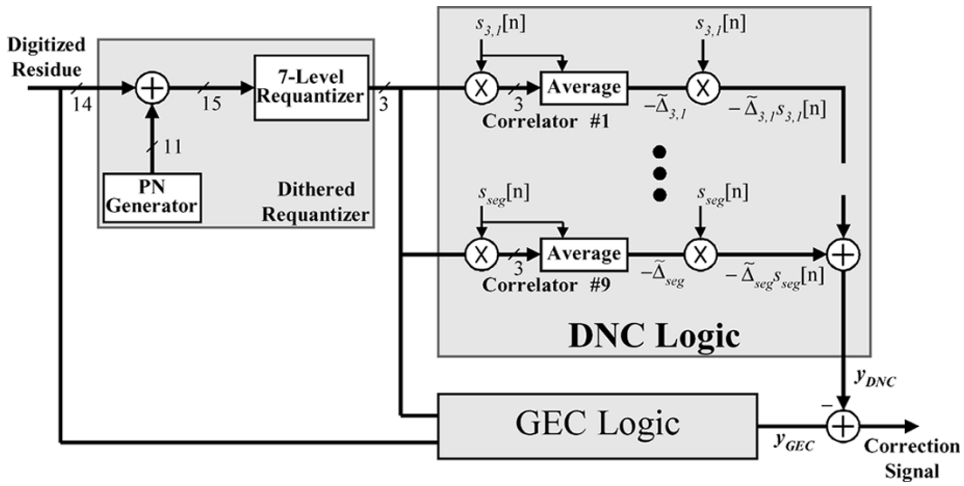

Fig. 7. First-stage correction logic with details of the DNC logic.

of switching block $S_{k,r}$ are set to $(x_{k,r}[n] \pm s_{k,r}[n])/2$, respectively. It can be shown that mismatch errors cause the DAC noise to have the form

$$e_{\mathrm{DAC}}[n] = \sum_k \sum_r \Delta_{k,r} s_{k,r}[n] + \Delta_{\mathrm{seg}} s_{\mathrm{seg}}[n] \qquad (5)$$

where the Δ_{seg} and $\Delta_{k,r}$ terms are constants that depend only on the mismatch errors. Thus, the DAC noise inherits the aforementioned statistical properties of the switching sequences. As discussed below, the DNC technique exploits these statistical properties to estimate and remove the DAC noise from the PADC output.

D. DAC Noise Cancellation

The structure imparted to the DAC noise by the DEM encoder is evident in (5). It is similar to spread spectrum modulation of several dc "message signals": the *unknown* constants Δ_{seg} and $\Delta_{k,r}$ are modulated by the *known* $s_{\mathrm{seg}}[n]$ and $s_{k,r}[n]$ "spreading codes." The DNC logic implements a simple digital spread-spectrum "receiver," or correlator, that estimates the Δ_{seg} and $\Delta_{k,r}$ terms and uses them to cancel the DAC noise in the PADC output.

Fig. 7 shows the top-level diagram of the first-stage correction logic (the DNC/GEC logic block in Fig. 2) and details of the DNC logic. The correction logic in the second and third stages are almost identical (their bus widths could have been scaled down relative to those in the first-stage correction logic, but to save design time this was not done). Both the first stage's *digitized residue* (combined digital outputs of all the remaining stages) and the uncorrected overall PADC output contain the output-referred DAC noise, which is an inverted and scaled version of DAC noise given by (5). Prior to the DNC logic, the digitized residue is converted from 14 bits to 3 bits (seven levels) by the *dithered* requantization block. Requantization is performed to reduce the size of the DNC logic. *Dithered* requantization ensures that the resulting requantization noise is white and uncorrelated with the digitized residue, which is necessary to avoid corrupting the correlations [1]. One drawback is that the requantization noise slows down the correlation process thereby increasing the time required for convergence. Seven-level requantization was found to be a good compromise between logic size and convergence time.

The DNC logic consists of nine *channels*, one for each switching block in the DEM DAC encoder. In each channel the requantized digitized residue is correlated against the switching sequence of the associated switching block to produce an output-referred estimate of one of the Δ_{seg} or $\Delta_{k,r}$ terms. Each channel output is formed by multiplying the estimate by the corresponding switching sequence. The outputs of all of the channels are added together to form the overall output of the DNC logic, $y_{\mathrm{DNC}}[n]$, which is an output-referred estimate of the total DAC noise and is used to cancel the DAC noise at the PADC output. As discussed in [1], the accuracy of the DAC noise estimation and cancellation depends on the number of samples used in the correlations. In this design, 2^{27} samples were used to obtain the desired performance.

E. Gain Error Correction

Fig. 8 illustrates the operation of the PADC with interstage gain error. Shown for a simple input case, interstage gain error, represented by ε in the figure, results in imperfect cancellation of the flash ADC quantization noise at the PADC output. Since the quantization noise is correlated with the input signal, both the SFDR and SNDR of the converter are degraded. The GEC technique adds a pseudorandom two-level signal, $r_{\mathrm{gec}}[n]$, to the output of the nine-level flash ADC as shown in Fig. 9 [2]. The $r_{\mathrm{gec}}[n]$ sequence is chosen to be white, zero mean, and uncorrelated with all other signals in the PADC. It takes on values of $\pm\Delta/4$ referred to the DAC output so as to occupy only a portion of the error headroom created by the redundancy used to cancel flash ADC errors. It travels the same path that the quantization noise travels to the PADC output and thus sees the same gain. To obtain an estimate of the normalized gain $(1+\tilde{\varepsilon})$, where $\tilde{\varepsilon}$ is the gain error estimate, the first stage's digitized residue is correlated against the random signal. The path traveled by the random signal must be sufficiently linear to ensure that the correlation is not corrupted. Given the gain error estimate, correction could be performed by multiplying the digitized residue by $-\tilde{\varepsilon}/(1+\tilde{\varepsilon})$ and adding the resulting correction signal to the overall PADC output. Under the assumption of a small gain error

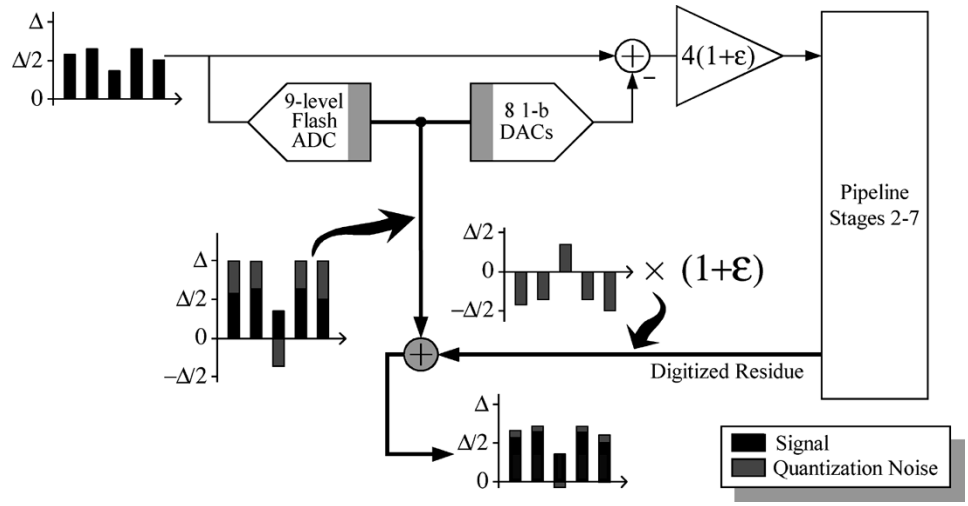

Fig. 8. Imperfect cancellation of quantization noise due to gain error.

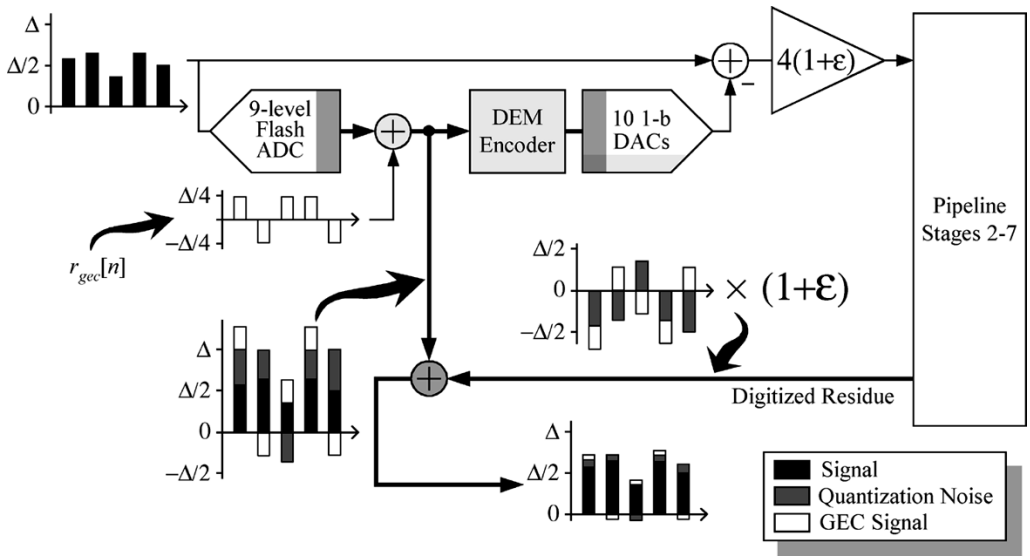

Fig. 9. Insertion of GEC PN sequence.

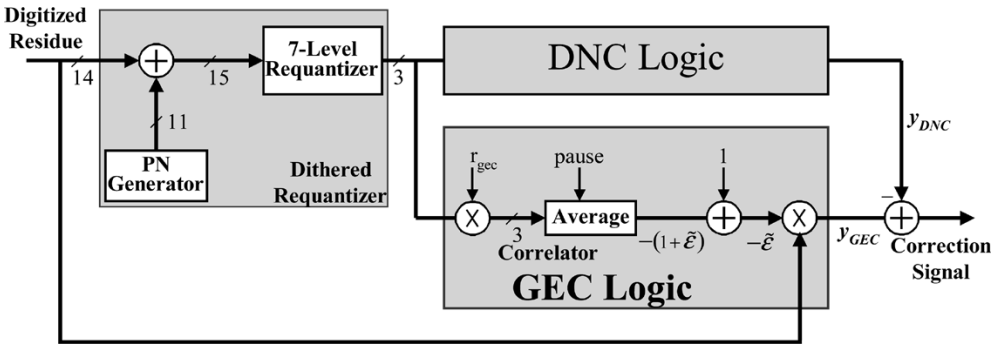

Fig. 10. First-stage correction logic with details of the GEC logic.

$(1+\tilde{\varepsilon}\approx 1)$, an approximation can be achieved by simply multiplying the digitized residue by $-\tilde{\varepsilon}$, thereby avoiding a division. In Fig. 10, a top-level diagram of the first-stage correction logic is shown with details of the GEC logic. The same issues regarding dithered requantization and the DNC logic previously discussed apply to the GEC logic as well. The accuracy of the gain error estimation and correction depends on the number of samples used in the correlations [2]. In this design, 2^{27} samples were used to obtain the desired performance.

The amplitude of $r_{\rm gec}[n]$ must be sufficiently small to prevent overloading the following stages. However, a large signal is desirable for rapid convergence of the estimation. As a compromise, an amplitude of $\Delta/4$ was chosen to leave approximately one-half of the error headroom created by redundancy available

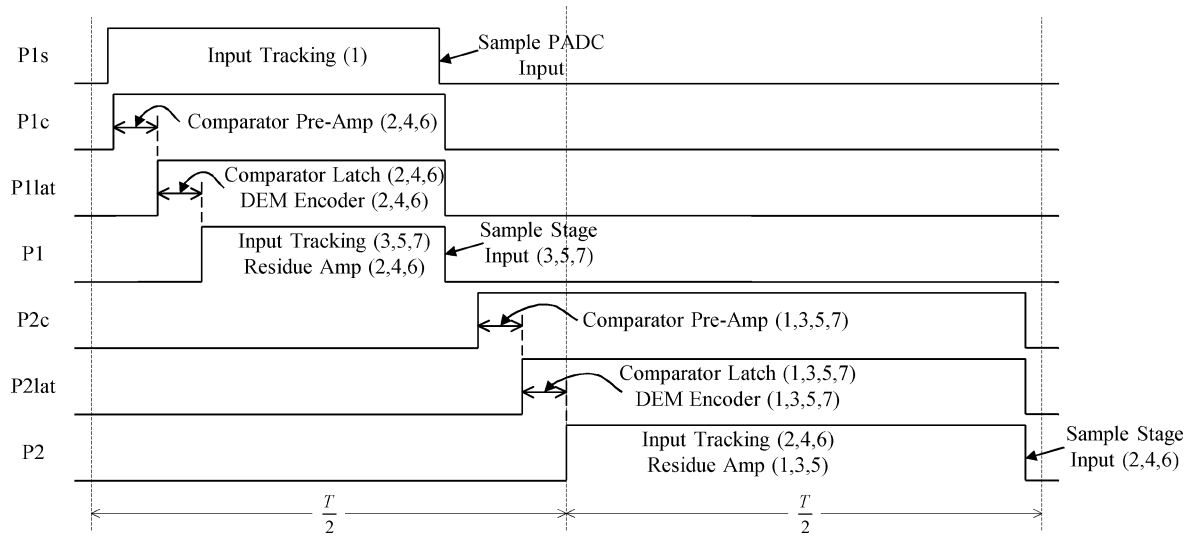

Fig. 11. Simplified timing diagram of the overall ADC (stage numbers in parentheses).

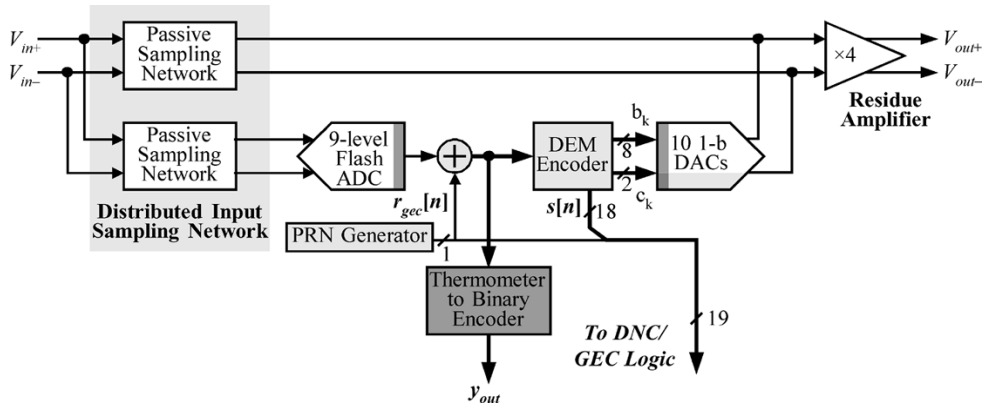

Fig. 12. Correction stage diagram showing distributed passive input sampling.

for flash ADC errors. To create the $\pm\Delta/4$ signal with a minimal amount of complexity, a 1 or 0 signal is added at the flash ADC output (converted to a $\Delta/2$ or 0 signal by the DAC), and a constant offset of $-\Delta/4$ is introduced at the DAC output. When the output of the flash ADC is positive full scale, adding 1 would exceed the input dynamic range of the DAC. To avoid this situation, the GEC operation is suspended each time the flash ADC output is positive full scale.

III. Circuit-Level Design Details

A. Overview of Switched-Capacitor Implementation

The prototype IC was implemented using fully differential switched-capacitor techniques. A simplified timing diagram of the chip is shown in Fig. 11. Delayed bottom-plate switching is used to reduce charge injection and clock feed-through effects. Separate DAC and input-sampling capacitors are used to prevent signal-dependent loading of the references. This benefit comes at the expense of increased kT/C noise resulting from the extra capacitors and increased residue amplifier requirements (because of the reduced feedback factor). The calibration techniques sufficiently relaxed the capacitor matching requirements such that the capacitor sizes in this design were determined by kT/C requirements alone. Moreover, no special attention was paid to capacitor matching, which greatly simplified the layout and reduced layout time.

B. Input Sampling Network

PADCs often include an input sample-and-hold amplifier (SHA). While an SHA relaxes circuit requirements in the remainder of the PADC, an SHA with sufficiently high linearity and low noise to meet the target specifications of this design would consume a large amount of current. To avoid this problem, this design avoids using an SHA by distributing the continuous-time input sampling operation into the main signal path and the flash ADC path as shown in Fig. 12 [26]. As described in [26], mismatches cause the sampled signal in each path to differ, but the difference is corrected along with the flash ADC errors provided the extra range created by redundancy is not exceeded. The input sampling network is comprised of eight of the simplified networks shown in Fig. 13. A single-ended version is shown for simplicity, but the actual circuits are fully differential. Instead of involving the residue amplifier and comparators in sampling the input as was done in [26], two passive switched-capacitor sampling networks are used. Matching is simplified as the time constant in both paths

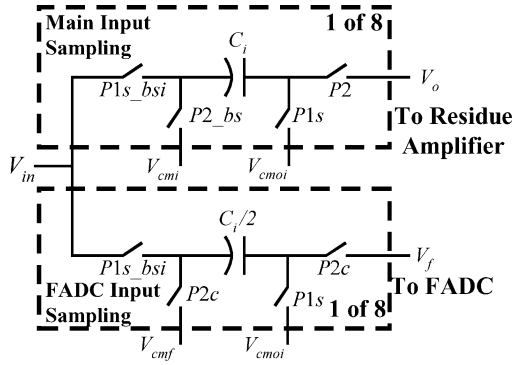

Fig. 13. Circuit diagram of the input sampling network.

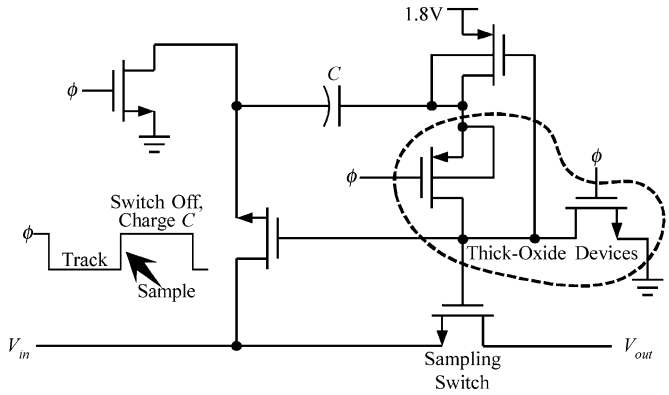

Fig. 14. Bootstrapped switch circuit.

is determined solely by transistors operating in the triode region and capacitors. Isolation between the continuous-time input and the first-stage residue amplifier is also increased. The flash ADC input network has the same nominal time constant as the main input network but uses half-sized elements to reduce area and input loading while still maintaining sufficient matching. The total capacitance in the flash ADC input network is 1 pF compared to 2 pF in the main input sampling network.

C. Bootstrapped Switch

To achieve the necessary linearity, the continuous-time input sampling switch is *bootstrapped* with the circuitry shown in Fig. 14. The circuitry is a modified version of that presented in [27]; process standard thick-oxide devices with 3.3-V voltage limits are used to replace thin-oxide devices wherever 1.8-V technology limits would otherwise be exceeded. Bootstrapping is also used for other critical switches in the PADC, such as those connected to a voltage near mid-supply or those with time-constant matching constraints.

D. DAC

A simplified diagram of the fully differential switched-capacitor DAC used in the first three stages is shown in Fig. 15. The DAC consists of ten 1-bit switched-capacitor DACs, eight with a step size of Δ and two with a step size of $\Delta/2$. The remaining stages use the same DAC architecture but without the two additional 1-bit DAC elements. The references in the DAC capacitor network are double sampled (once each clock phase by each capacitor) to effectively double the reference voltage and allow the use of half-sized capacitors. This has the benefits of decreased kT/C noise and increased residue amplifier feedback factor. Because of DNC and GEC, the increased DAC mismatches and gain error resulting from the smaller capacitors are not problematic.

E. Residue Amplifier

A simplified diagram of the two-stage Miller-compensated opamp used in the residue amplifier is shown in Fig. 16. A folded-cascode input stage was chosen for high gain and a common-source output stage was chosen for wide output swing despite the low supply voltage. The OTA output common-mode voltage is sensed and compared to a common-mode reference by a simple *RC* circuit and a current-mirror amplifier not shown in the figure. The inverted output of the current-mirror amplifier, labeled V_{CMFB} in Fig. 16, is used to control the common-mode voltage.

In a conventional PADC without calibration, more than 100 dB of open-loop dc gain would be required to meet the desired performance, typically requiring amplifier gain-boosting techniques. Gain-boosting circuitry, along with enable/disable functionality, is included on the prototype IC. Simulations indicate more than 125 dB of open-loop dc gain with gain-boosting enabled, but only 85 dB with gain boosting disabled. However, the gain without boosting is sufficient to suppress nonlinearity in the amplifier and switches for the target specifications, and thus the error is mainly linear and can be corrected by GEC. As expected, the measured PADC performance with GEC enabled does not significantly degrade when gain boosting is disabled.

The amplifier is scaled down once and used in all the remaining stages without further scaling. More aggressive scaling would have reduced power consumption without significantly degrading performance, but was not done in the interest of saving design and layout time.

F. Clock Generator

With the distributed input sampling network described previously, proper nonoverlapping timing of the switched capacitors requires the comparators in the flash ADCs and the DEM encoder to wait until the beginning of the amplification phase to process the inputs as the nonoverlapping time can no longer be used [26]. Therefore, in a normal two-phase clocking scheme, the time required for the comparators and the DEM encoder to operate reduces the time available for all the residue amplifiers to settle. The first-stage amplifier is typically the most critical block in the pipeline as it sets limits on converter speed and consumes a significant portion of the overall power. This is especially the case with a multibit first stage, because the requirements on the remaining stages are significantly relaxed. To ensure that the time for the amplification phase of the first-stage amplifier, *P2*, is not reduced by the time required for the comparators and DEM encoder, the standard nonoverlapping clock generator is modified with an extra feedforward path, as shown in Fig. 17. All of the time required for the comparators and DEM encoders in both phases is now taken from the second stage's amplification phase (*P1*), as shown in Fig. 11. Although this asymmetric clocking reduces the available time for the second-stage amplifier to settle and thus reduces allowable

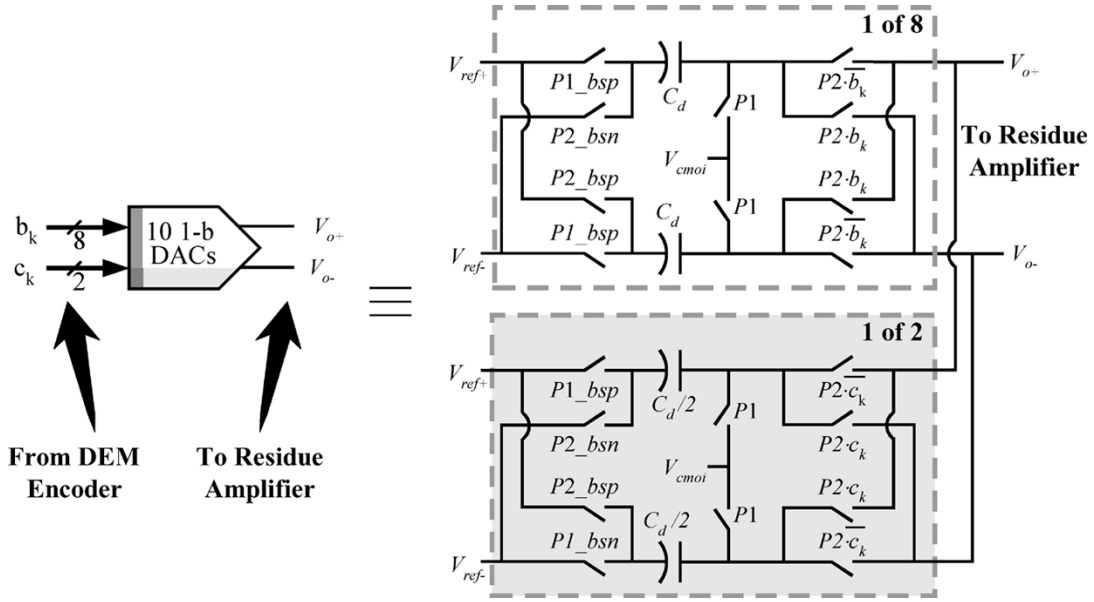

Fig. 15. Circuit-level implementation of the 1-bit DACs.

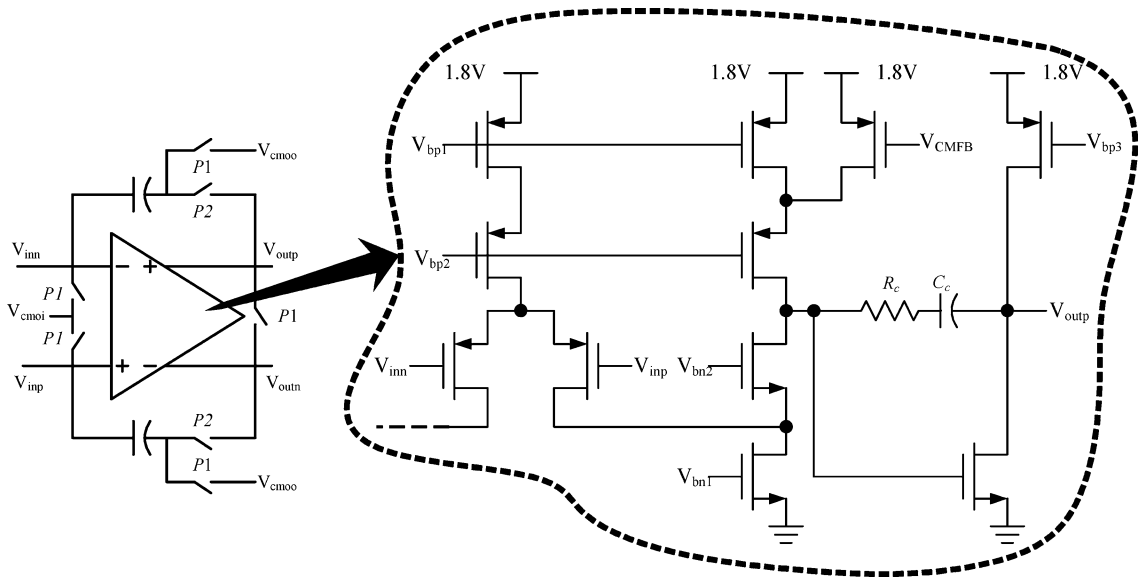

Fig. 16. Residue amplifier architecture.

amplifier scaling, increasing the requirements on the second stage to decrease the requirements on the first stage is a desirable tradeoff. The clock phase used to sample the continuous-time PADC input, *P1s*, is not affected by the modification and is thus reduced by only one set of flash ADC and DEM encoder periods. This pulsewidth reduction may be an issue depending on the application (i.e., depending on the input driving circuitry).

G. DAC Encoder

Previous high-speed (low-latency) implementations of tree-structured DEM DAC encoders optimize the delay of the individual switching blocks shown in Fig. 6 [28]. The resulting encoder circuit, having a tree-like implementation, has a critical path consisting of a series of transmission gates. All of the transmission gates can be preset as the state depends only on the sequences coming from the PN generator in the DEM encoder [28]. Modeling the series transmission gates as a transmission line and assuming an equivalent load on each gate yields an approximate signal delay [29] of

$$t_d \cong 0.35RC(N)(N+1) \tag{6}$$

where R and C are the equivalent resistance and capacitance of each switch, and N is the number of bits in the encoder. Therefore the total propagation delay is proportional to the square of the number of bits in the encoder.

A new high-speed implementation for tree-structured DAC encoders is shown in Fig. 18 for the 4-bit partially segmented tree-structured encoder of Fig. 6. The addition of the GEC PN signal to the DAC input is also done in this block to minimize the total latency. The implementation consists of a control logic

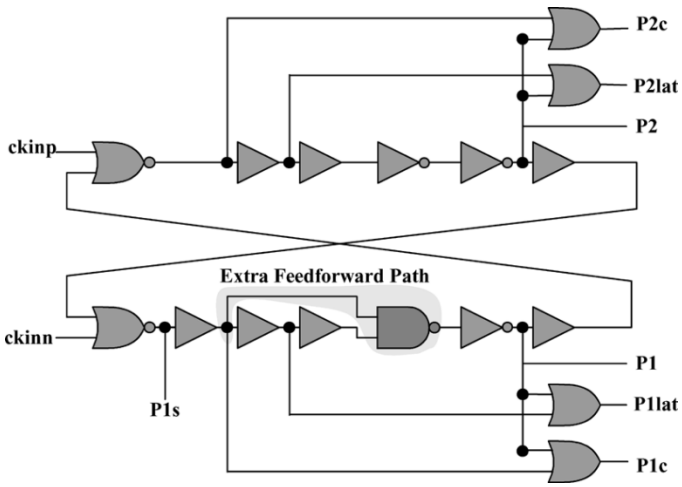

Fig. 17. Simplified diagram of the modified nonoverlapping clock generator.

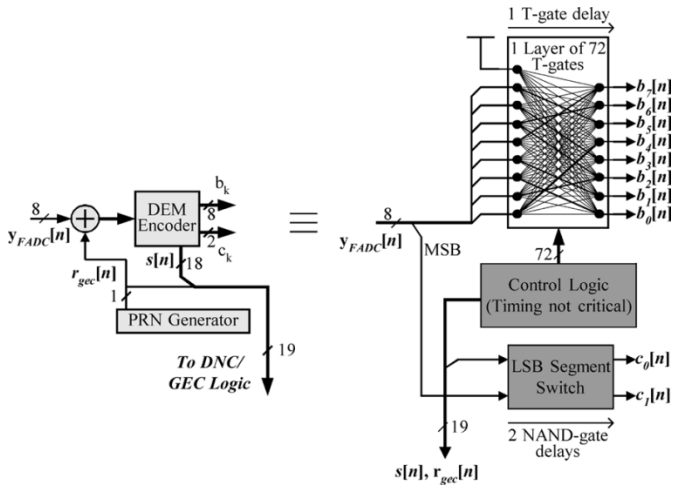

Fig. 18. Low-latency implementation of the DEM encoder and GEC adder.

block that controls a bank of transmission gate switches and a LSB segment switch. The control logic block presets the paths (i.e., the switches) from the flash ADC output to the encoder output using the bits from GEC PN generator and the DEM encoder PN generator. The critical path is reduced to a single transmission gate delay.

Although the critical path has been reduced to a single transmission gate, there is an increase in the number of switches required. For an N-bit unit element tree-structured encoder with $M+1$ levels, where $M=2^N$, the total number of switches is increased to M^2 from $2MN$, but they can be smaller now since they are not in series. Each flash ADC output line has increased parasitic capacitive loading, but it is small since it comes from switches that are off. There is an increase in digital logic over the previous implementation, but it does not reside in the signal path. Latency has been thus reduced mainly at the expense of increased digital complexity which is a desirable tradeoff.

H. Process, Packaging, and Layout Overview

The IC is fabricated in the TSMC 0.18-μm 1P6M mixed-signal CMOS process with MiM capacitors. Separate deep N-wells and multiple voltage supply domains are employed

TABLE I
FABRICATION AND MEASUREMENT SUMMARY

Resolution	15 b
Sample Rate	40 MHz
Input Voltage Range	2.25 Vp-p differential
SFDR	90 dB
THD	88 dB
Peak SNR	72 dB
DNL	0.25 LSB
INL	1.5 LSB
SFDR Improvement With DNC & GEC	> 20 dB
SNDR Improvement With DNC & GEC	> 12 dB
Total Power	400 mW
Analog Power	343 mW
Digital Power	51 mW
Output Drivers	6 mW
Technology	0.18μ 1P6M CMOS
Die Size	4 mm x 5 mm (including pads)
Package	56-Pin QFN with ground downbonding

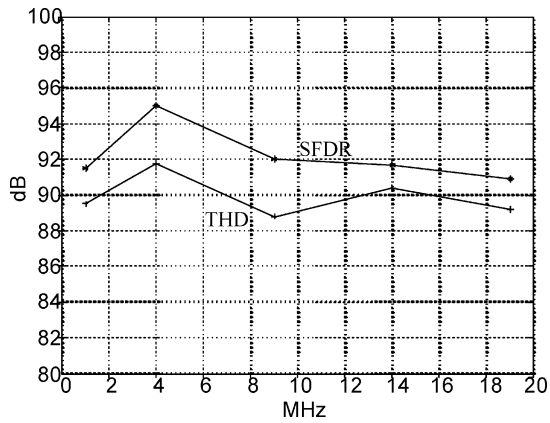

Fig. 19. Measured SFDR and THD versus input frequency.

to reduce undesirable coupling to and from both analog and digital sections, and to improve isolation within and between the PADC stages. A 56-pin QFN package with an exposed die paddle is used for its good electrical performance and grounding capabilities. Down-bonding of all grounds to the exposed paddle, double-bonding of critical supply pins, and on-chip decoupling capacitance help reduce power supply bounce. ESD protection circuitry is contained in all pads.

IV. MEASUREMENT RESULTS

A printed circuit test board was designed, fabricated, and interfaced to a digital data acquisition board to test the PADC. The single-ended output of a low-jitter crystal oscillator mounted on the test board is converted to a differential signal via a transformer and used to clock the PADC IC. A high-purity signal generator was used to generate test signals across the 20-MHz

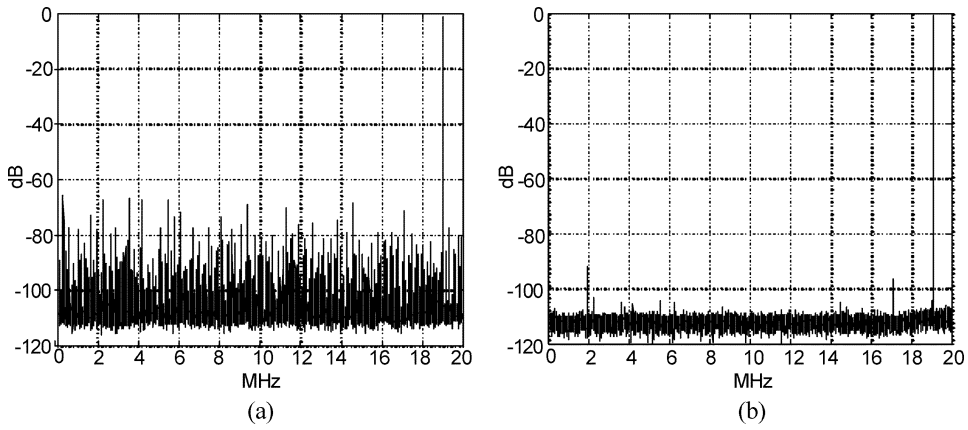

Fig. 20. Measured PSD plots for a 19.03-MHz input signal with calibration (a) disabled and (b) enabled.

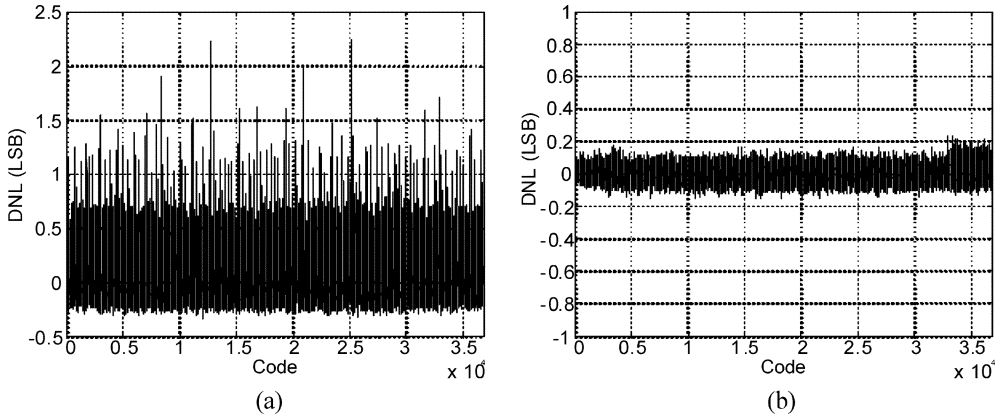

Fig. 21. Measured DNL plots for a 1.01-MHz input signal with calibration (a) disabled and (b) enabled.

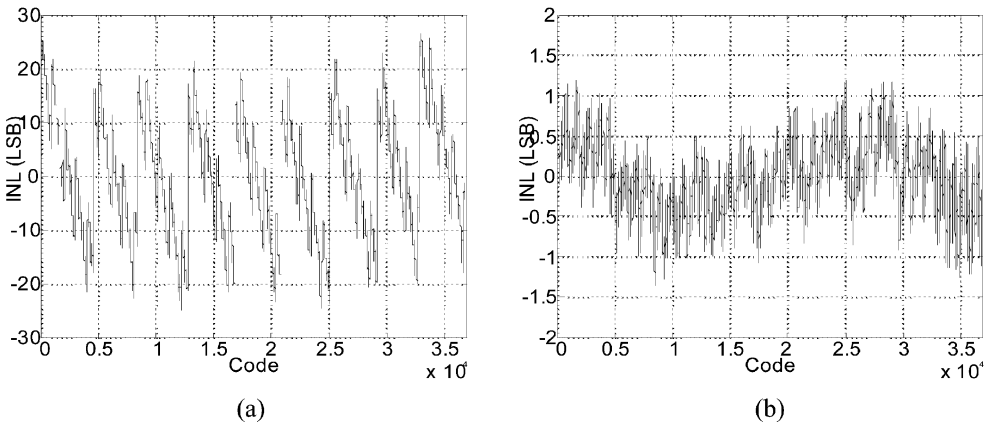

Fig. 22. Measured INL plots for a 1.01-MHz input signal with calibration (a) disabled and (b) enabled.

Nyquist band of the PADC. For each input frequency, one of a set of five high-quality custom discrete-component bandpass filters was used to further purify the input signal just prior to the test board connection. The test board was designed for two different input signal-path component population options: 1) transformer-based single-to-differential input signal conversion and 2) opamp-based single-to-differential input signal conversion. The transformer option works well for frequencies of 9 MHz and higher, but at lower frequencies the distortion performance of the transformer is less than that of the PADC. The opamp option works well for frequencies of 9 MHz and below, but introduces distortion at higher frequencies. Therefore, both options were necessary to measure the performance of the PADC over its full bandwidth.

Table I contains a summary of fabrication and measurement details. The IC operates from a 1.8-V supply, except for the digital logic core that needs to be powered from a 2.1-V supply when the chip is operated at 40 MS/s due to a digital timing error (1.8 V was sufficient at 20 MS/s). Fig. 19 shows SFDR and total harmonic distortion (THD) performance versus input frequency

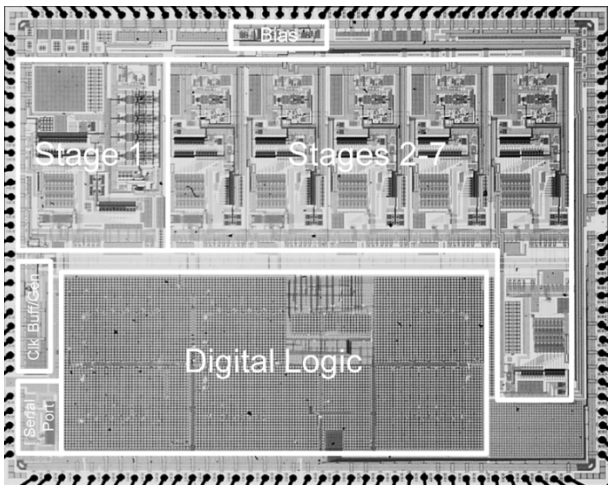

Fig. 23. Die photo.

at −1 dBFS. A representative PSD plot from the ADC with and without the calibration techniques enabled for a −1-dBFS 19.03 MHz input signal is shown in Fig. 20. DNL and INL measurements at 1.01 MHz with calibration disabled and enabled are shown in Figs. 21 and 22, respectively. As can be seen from the figures, the calibration techniques result in significant improvements in SNDR, SFDR, DNL, and INL. The die photo is shown in Fig. 23.

V. Conclusion

The silicon implementation of two digital background calibration techniques has been presented. The DNC technique compensates for DAC mismatch noise, while the GEC technique compensates for interstage gain errors. Both techniques operate in the background, transparent to normal converter use, and perform their error estimation and correction completely in the digital domain. Together they drastically reduce analog circuit requirements required to achieve high performance. They have been shown to be enabling components in a high-resolution PADC.

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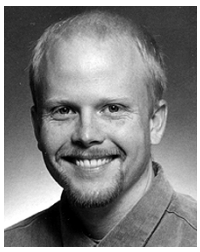

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