25.1 A Digitally Enhanced 1.8V 15b 40MS/s CMOS Pipelined ADC

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The trends toward increased digital signal processing and tighter integration in communications and imaging systems have created a need for high-resolution, low-voltage ADCs with sample-rates above 20MHz. Pipelined ADCs are well-suited to such applications, but are sensitive to component mismatches and interstage gain errors, especially at low supply voltages. This paper demonstrates two digital background calibration techniques that address these problems in the context of a 1.8V CMOS pipelined ADC. Together, they enable the ADC to achieve 90dB SFDR and 72dB peak SNR over the full 20MHz Nyquist band. The INL and DNL are 1.5LSB and 0.25LSB, respectively.

As shown in Fig. 25.1.1, the ADC consists of 7 pipeline stages. Each stage resolves 9 levels with a gain of 4, so the ideal resolution of the ADC is slightly above 15 bits. The calibration techniques, referred to as DAC noise cancellation (DNC) and gain error correction (GEC), respectively, are applied to the first three pipeline stages [1,2]. These stages, which are shown in Fig. 25.1.2, differ from a conventional pipeline stage in 3 respects: 1) a dynamic element matching (DEM) DAC is used in place of a thermometer-encoded DAC, 2) a 1-bit pseudo-random number (PN) sequence, $r_{GEC}[n]$, which takes on values of $\pm\Delta/4$ referred to the DAC output is added to the input of the DAC, where Δ is the step-size of the flash ADC, and 3) the resolution of the DAC is increased to accommodate $r_{GEC}[n]$. These modifications allow the DNC/GEC logic blocks to estimate and largely cancel the error sequences in the uncorrected ADC output resulting from DAC noise and non-ideal interstage gains. The estimation and cancellation are performed digitally in the background, transparent to normal ADC use.

The DEM DAC consists of a DEM encoder followed by a segmented bank of 10 1-bit switched-capacitor DACs, 8 with a step-size of Δ and 2 with a step-size of $\Delta/2$. For each input sample, the DEM encoder selects its 10 output bits such that the sum of the 1-bit DAC outputs would equal the input value if there were no capacitor mismatches. For most input values, there are several different 10 bit combinations with this outcome. The choice of which such combination to use is made pseudo-randomly.

The details of the DEM encoder are best described in terms of its 9 switching blocks labeled S_{seg} and $S_{k,r}$. Ignoring the $\Delta/2$ LSB factor, the DAC input, $x_{in}[n]$, can be viewed as an integer in the range -8 to 8. At each sample time n, the top and bottom outputs of switching block S_{seg} are set to $(x_{in}[n]+s_{seg}[n])/2$ and $-s_{seg}[n]$, respectively, where $s_{seg}[n]$ is zero if $x_{in}[n]$ is even, and chosen pseudo-randomly to be ±1 otherwise. Similarly, the top and bottom outputs of switching block $S_{k,r}$ are set to $(x_{k,r}[n]\pm s_{k,r}[n])/2$, respectively, where $s_{k,r}[n]$ is zero if $x_{k,r}[n]$ is even, and chosen pseudo-randomly to be ±1 otherwise. Each pseudo-random choice is driven by one of the 9 PN sequences which are designed to well approximate white, uncorrelated random processes. Thus, the $s_{k,r}[n]$ sequences are also white and uncorrelated. The PN sequences along with the parity of each switching block input are passed to the corresponding DNC/GEC logic block, thereby giving it access to the $s_{seg}[n]$ and $s_{k,r}[n]$ sequences.

It can be shown that capacitor mismatches cause the DEM DAC to introduce additive DAC noise of the form

$$e_{DAC}[n] = \Delta_{seg} s_{seg}[n] + \sum_{k,r} \Delta_{k,r} s_{k,r}[n],$$

where the Δ_{seg} and $\Delta_{k,r}$ terms are constants that depend only on the capacitor mismatches. The objective of the DNC logic is to digitally estimate and cancel the DAC noise component from the uncorrected ADC output. This is possible because the $s_{seg}[n]$ and $s_{k,r}[n]$ sequences are white and uncorrelated, are restricted to values of 0 and ±1, and are known to the DNC logic. A simple correlation algorithm, similar to that of a digital spread spectrum receiver, is used to estimate $e_{DAC}[n]$ in the background as described in [1].

As described in [2], GEC operates on a related principle. Capacitor mismatches, finite open-loop op-amp gain, incomplete settling, charge injection, and clock feed-through all give rise to interstage gain error, which causes coarse quantization error from the individual stages to appear in the uncorrected ADC output. Each GEC logic block estimates the non-ideal interstage gains by correlating the digitized residue against the $r_{GEC}[n]$ sequence added in the corresponding pipeline stage, and uses the estimate to scale the digitized residue so as to generate a sequence with which to cancel the associated error term in the uncorrected ADC output.

To minimize latency, the $r_{GEC}[n]$ adder and DEM encoder are implemented together as shown in Fig. 25.1.3. The input-output functionality is as described above, but the logic has been flattened so the critical path is a single layer of transmission gates preset by 40MHz clocked logic.

Standard switched-capacitor circuits are used in all stages. The continuous-time input is sampled separately for the main signal path and the flash ADC [3]. Critical switches are implemented with the bootstrapped switch shown in Fig. 25.1.4, which is a modification of that presented in [4]. Separate DAC and input capacitors are used to avoid signal dependent loading of the references at the expense of increased residue amplifier requirements and kT/C noise. The DAC capacitors sample the reference voltages on both clock phases, thereby allowing half-size capacitors. The first stage capacitor sizes were chosen just large enough to meet kT/C noise requirements, and matching issues were not considered critical during layout with the view that DNC and GEC would compensate for capacitor mismatches. Indeed, simulations suggest that to achieve the reported performance without DNC and GEC using this design and circuit technology would have required 25 times larger first-stage capacitors.

A two-stage Miller-compensated OTA with a PMOS folded-cascode input stage is used in each residue amplifier. Without GEC, better than 100dB of open-loop gain would be required, which would necessitate gain boosting. However, GEC relaxes the gain requirement to the point that gain boosting is not necessary. To demonstrate this point, gain boosting circuitry that can be disabled digitally is included in the first stage. The reported experimental results are with gain boosting disabled.

The ADC was tested at input signal frequencies across the 20 MHz Nyquist band, and no significant performance degradation was observed as a function of frequency. A representative PSD plot from the ADC with a 19.03MHz input signal is shown in Fig. 25.1.5. Additional fabrication and measurement details are provided in Fig. 25.1.6, and a die photo is shown in Fig. 25.1.7.

References:

[1] I. Galton, "Digital Cancellation of D/A Converter Noise in Pipelined A/D Converters," *IEEE Trans. Circ. Syst. II*, pp. 185-196, Mar. 2000.

[2] E. J. Siragusa and I. Galton, "Gain Error Correction Technique for Pipelined Analogue-to-Digital Converters," *Elect. Let.*, pp. 617-618, Mar. 2000.

[3] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE J. Solid-State Circuits*., no. 3, pp. 318-325, Mar. 2000.

[4] M. Dessouky and A. Kaiser, "Input Switch Configuration Suitable for Rail-to-Rail Operation of Switched Opamp Circuits," *Elect. Let.*, pp. 8-10, Jan. 1999.

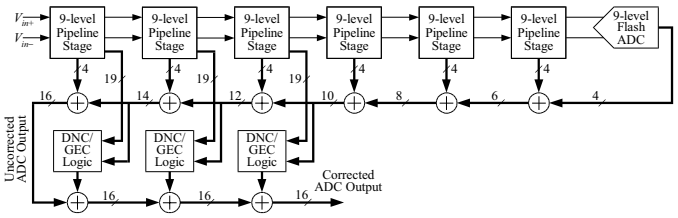

Figure 25.1.1: Block diagram of the implemented pipelined ADC.

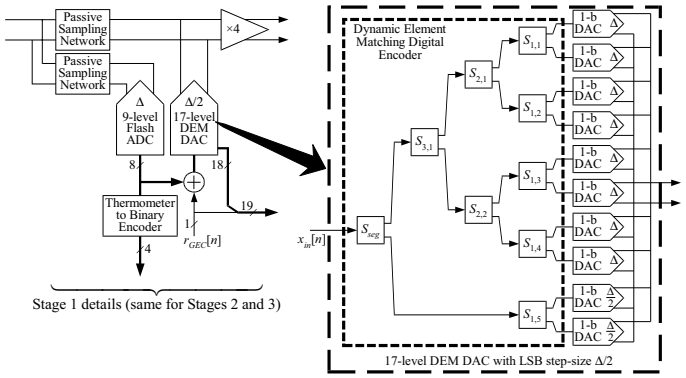

Figure 25.1.2: Behavioral details of the first three pipeline stages.

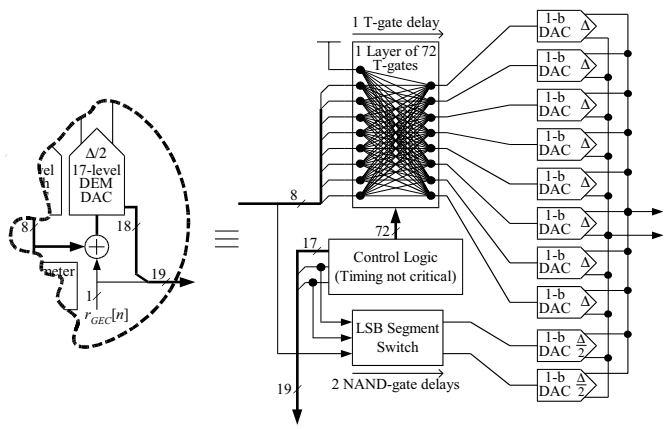

Figure 25.1.3: Implementation of the GEC adder and DEM digital encoder.

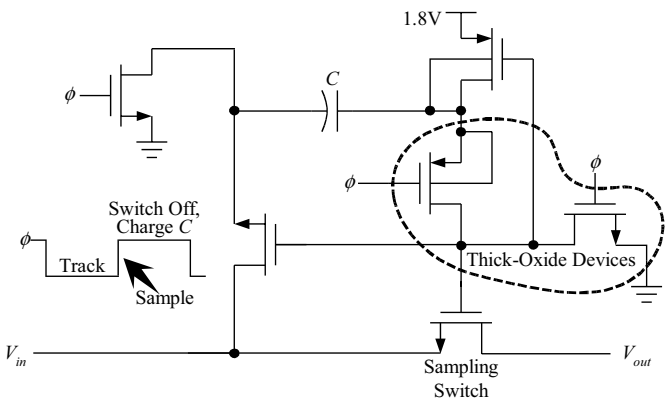

Figure 25.1.4: Bootstrapped switch details.

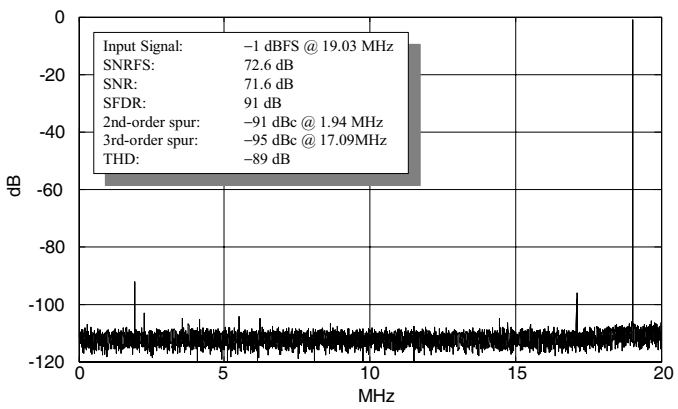

Figure 25.1.5: Representative measured PSD plot with DNC and GEC enabled.

Resolution	15 bits
Sample Rate	40 MHz
Input Voltage Range	2.25 Vp-p differential
SFDR	90 dB
THD	88 dB
Peak SNR	72 dB
DNL	0.25 LSB
INL	1.5 LSB
SFDR Improvement with DNC & GEC	> 20 dB
Peak SNDR Improvement with DNC & GEC	> 12 dB
Power Consumption:	
Analog:	343 mW
Digital:	51 mW
Output Drivers:	6 mW
Total:	400 mW
Die Size	4 mm × 5 mm (including pads and ESD circuitry)
Technology	0.18 µm 1P6M CMOS
Package	56 Pin QFN with ground down-bonding

Figure 25.1.6: Performance summary.

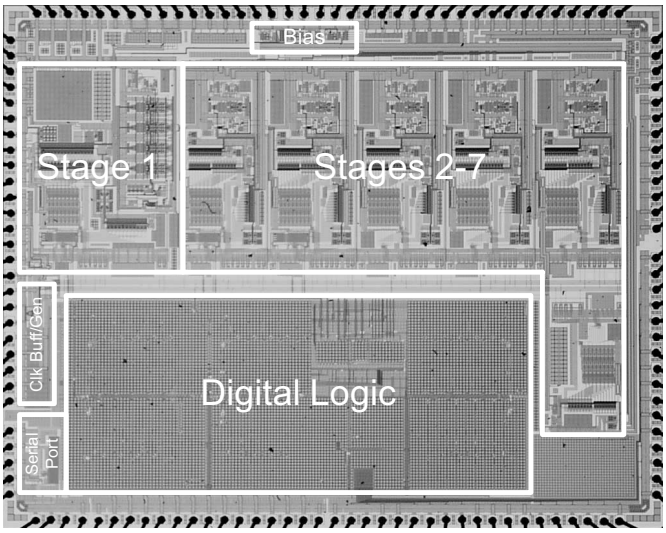

Figure 25.1.7: Die micrograph.

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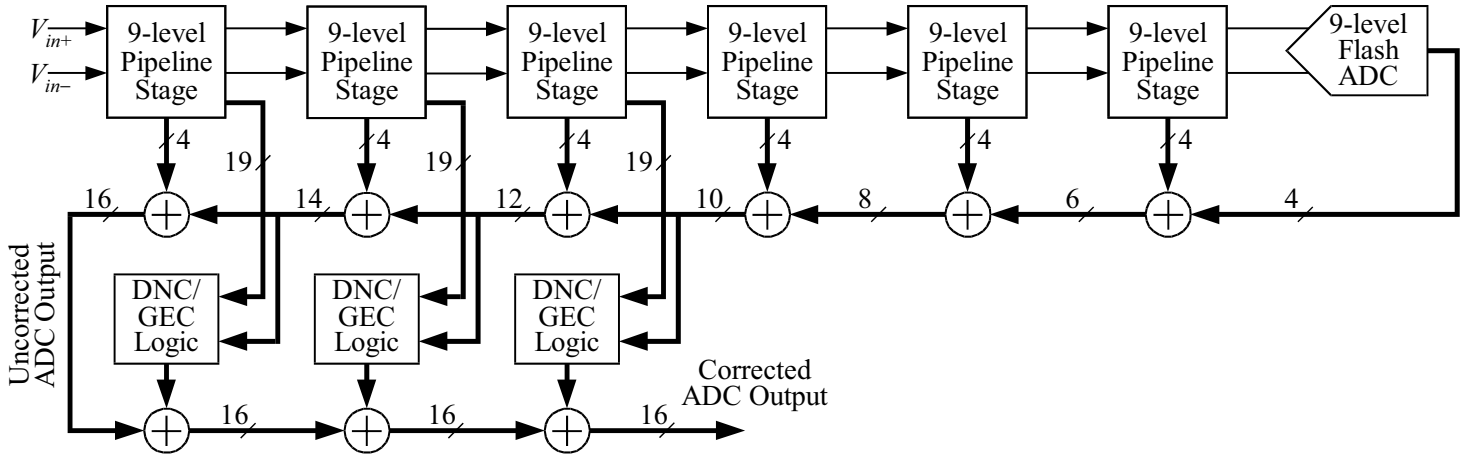

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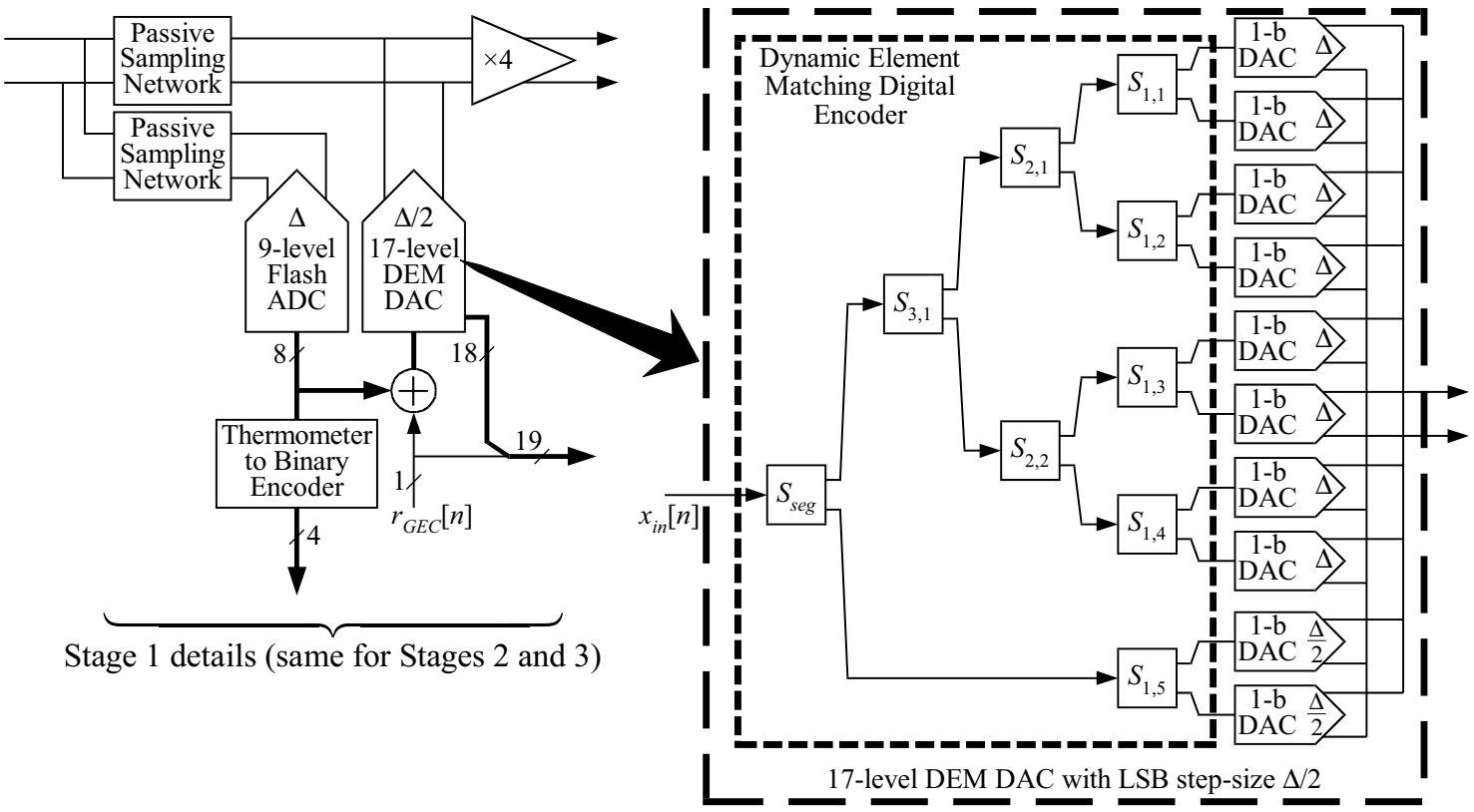

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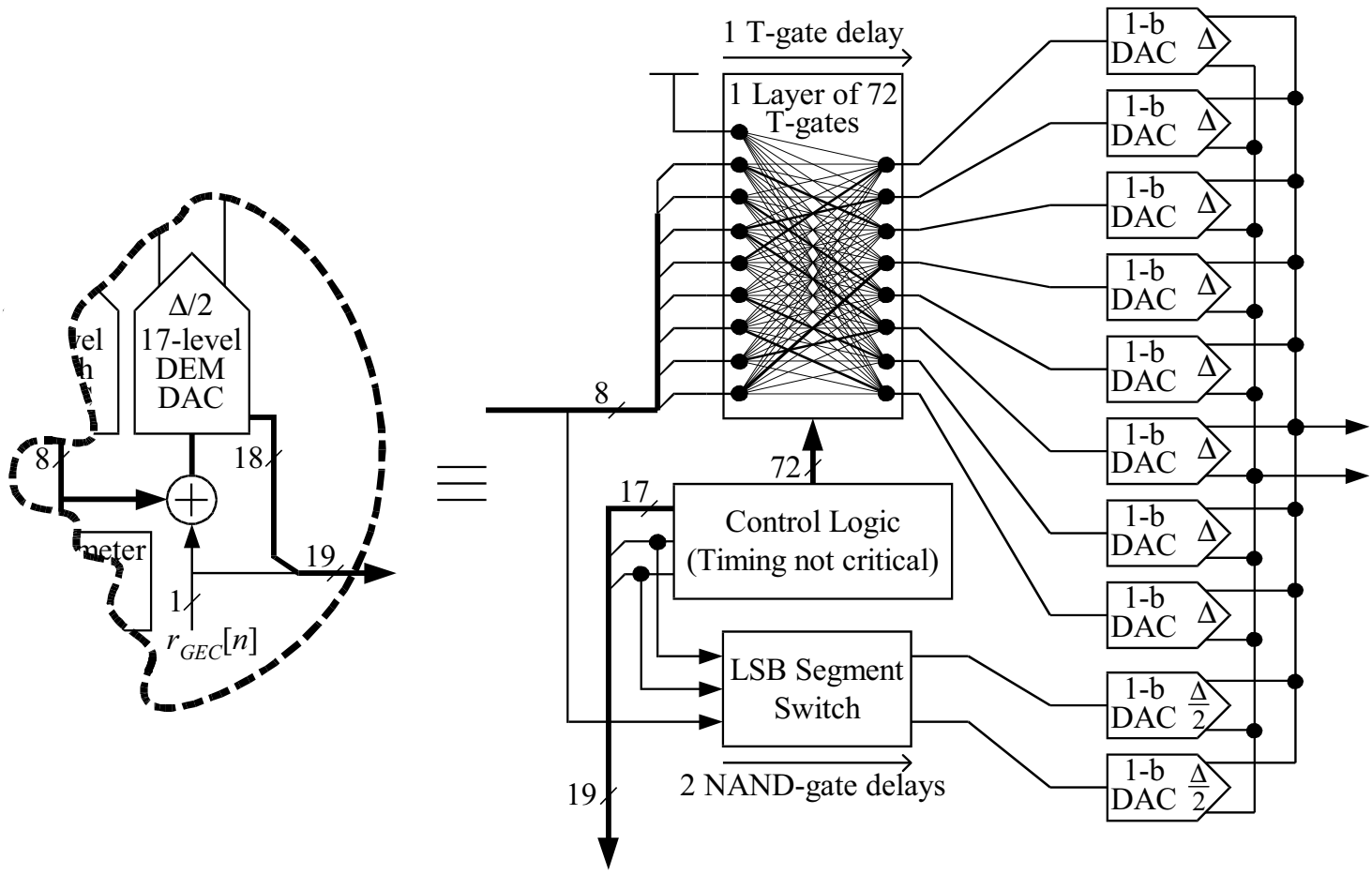

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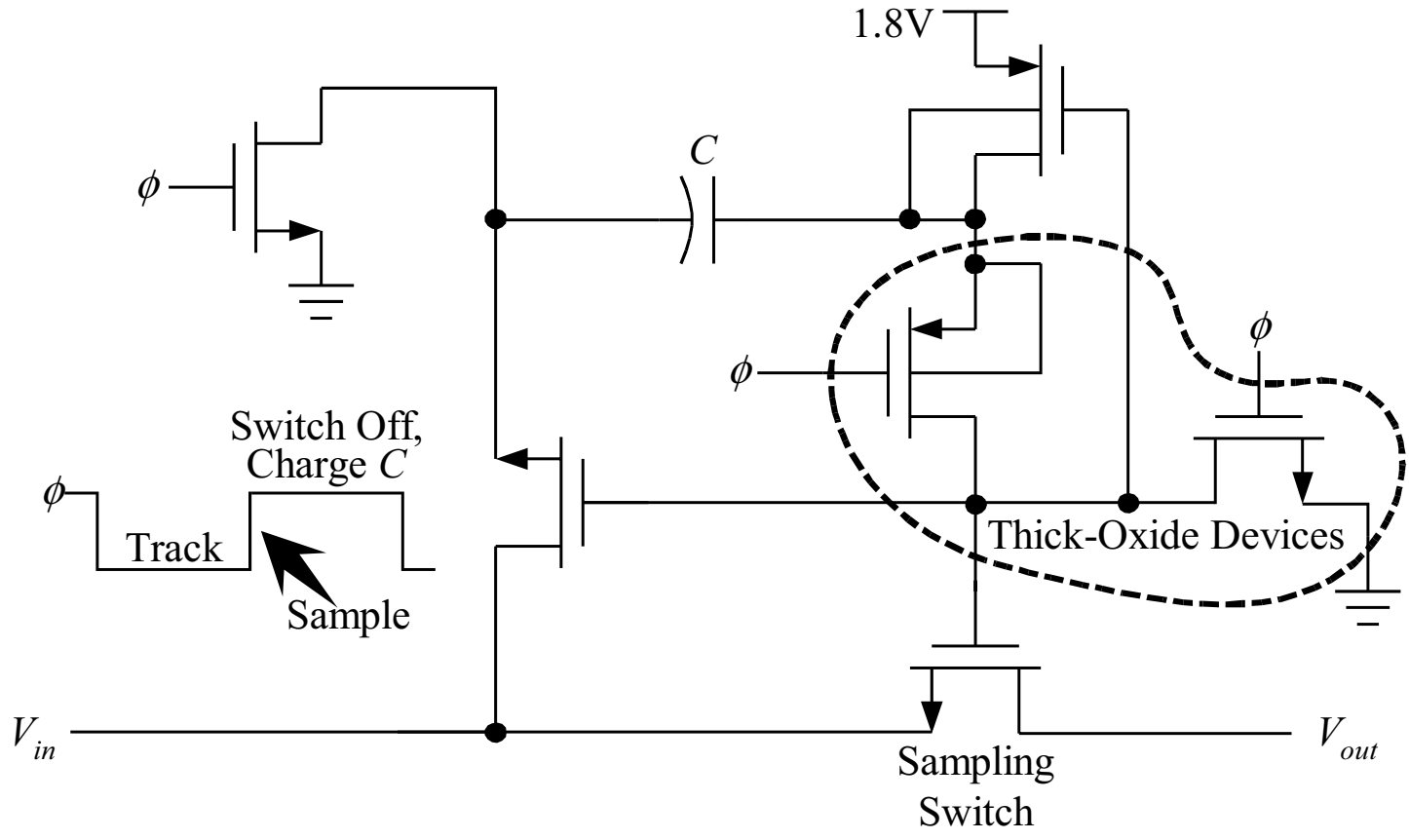

Figure 25.1.4: Bootstrapped switch details.

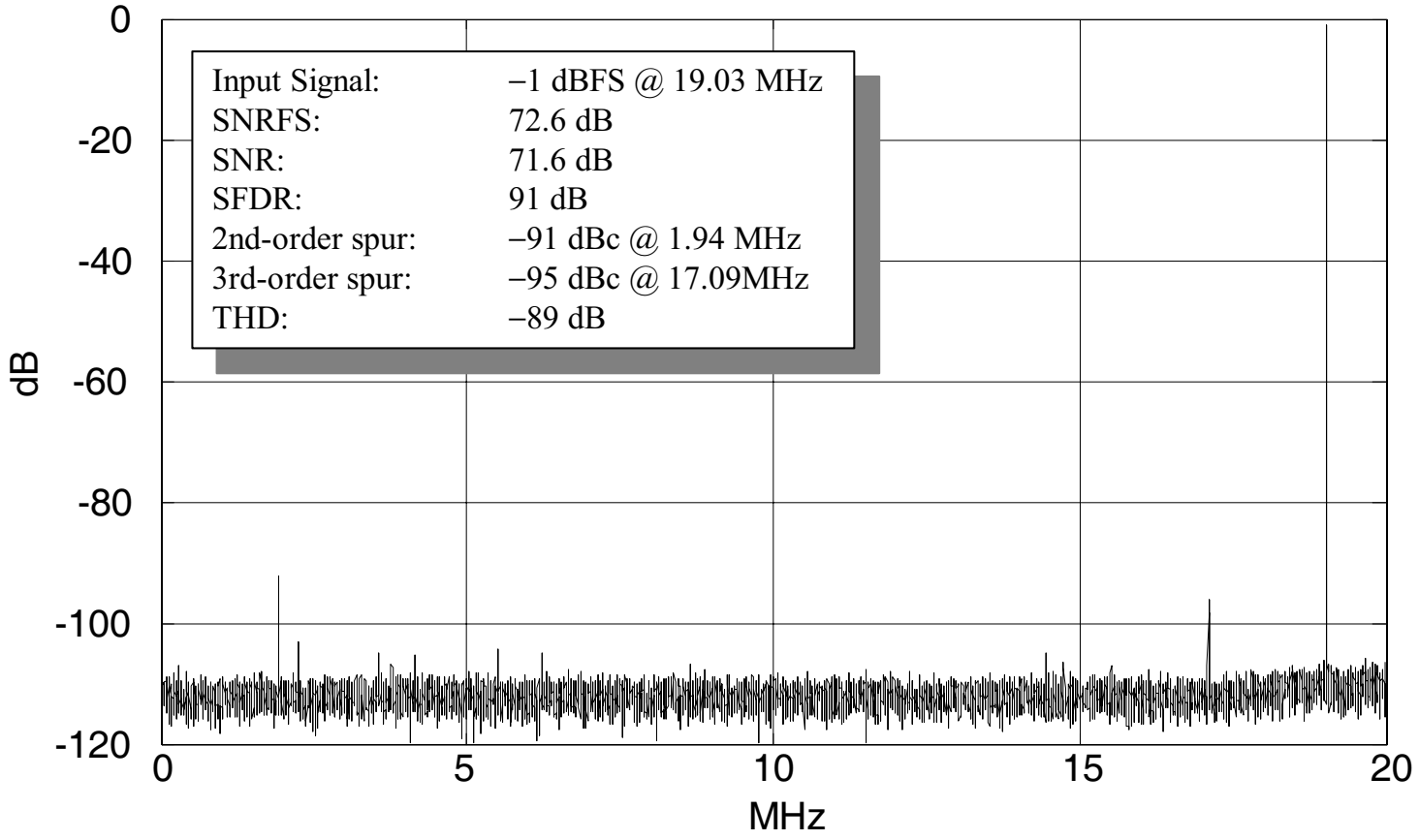

Figure 25.1.5: Representative measured PSD plot with DNC and GEC enabled.

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SFDR Improvement with DNC & GEC	> 20 dB
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Power Consumption: Analog: Digital: Output Drivers: Total:	 343 mW 51 mW 6 mW 400 mW
Die Size	4 mm × 5 mm (including pads and ESD circuitry)
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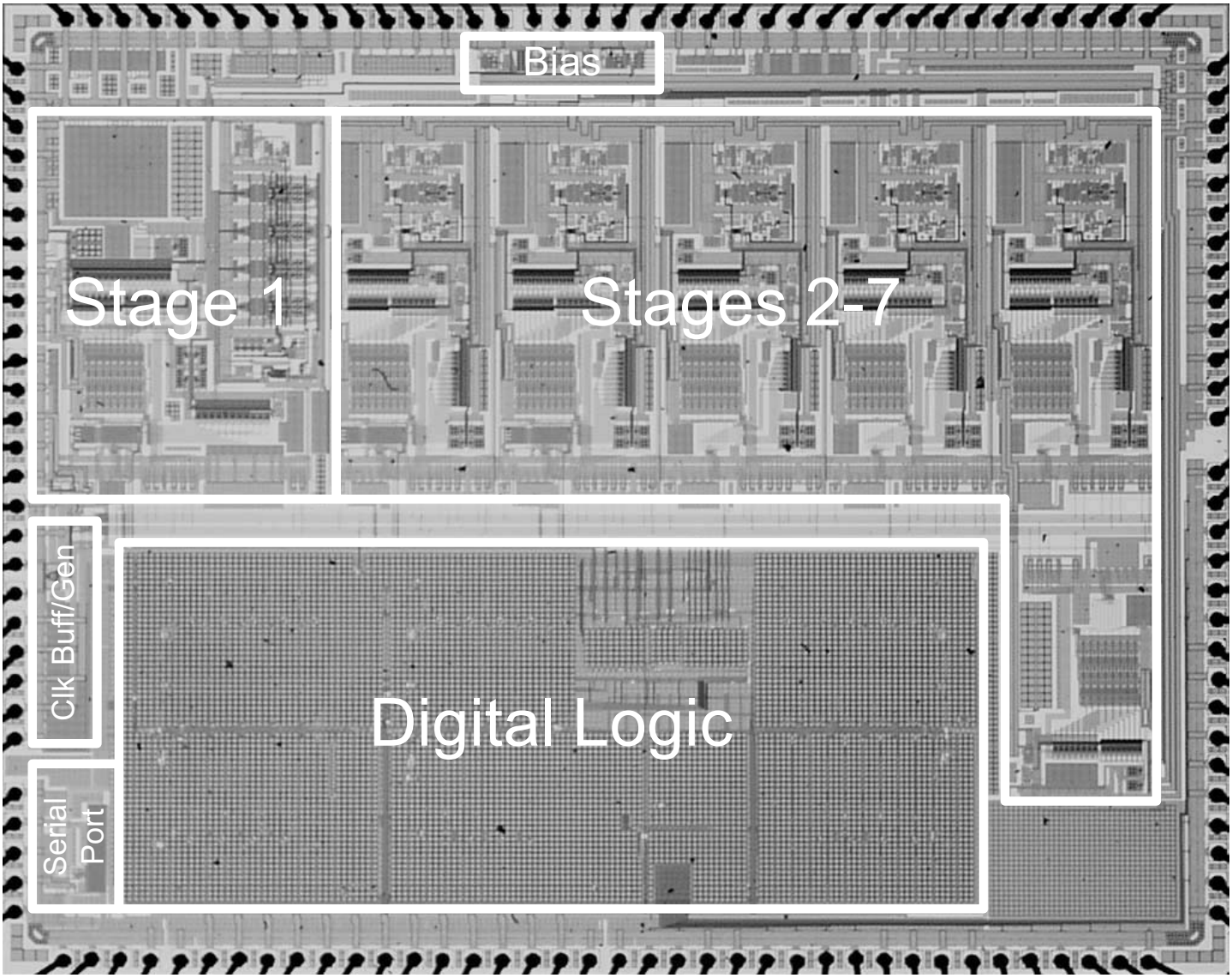

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